Design of an Input-Parallel Output-Parallel Multi-Module DC-DC Converter Using a Ring Communication Structure

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Abstract

The design feasibility of a micro unidirectional DC transmission system based on an input-parallel output-parallel (IPOP) converter is analyzed in this paper. The system consists of two subsystems: an input-parallel output-series (IPOS) subsystem to step up the DC link voltage, and an input-series output-parallel (ISOP) subsystem to step down the output voltage. The two systems are connected through a transmission line. The challenge of the delay caused by the communication in the control system is addressed by introducing a ring communication structure, and its influence on the control system is analyzed to ensure the feasibility and required performance of the converter system under practical circumstances. Simulation and experiment results are presented to verify the effectiveness of the proposed design.

I. INTRODUCTION

Input-parallel output-parallel (IPOP) connected DC/DC conversion systems provide scalability as well as reliability for high power rating requirements. Since the system components can be distributed, this allows the size of the magnetic components to be reduced by operating the individual converters at a high switching frequency [1]-[3]. The design of such a portable system has been discussed here. The proposed application of this system is in emergency situations, where power transmission for short distances of a few kilometers is required.

Conventionally, there are two main issues that need to be addressed in a multiple DC/DC conversion systems. The first

challenge is the voltage and current balance problem of each module in the presence of substantial differences in the various module parameters of real applications [1]-[4]. This issue has received a great deal of research coverage [1]-[10]. The second challenge is the physical realization of the control structure for the control of the system. Since a DC/DC conversion system consists of a number of modules, the control structure is usually categorized as either a centralized control structure or as a distributed control structure. When compared to the centralized control structure, the distributed structure is more flexible, and provides a higher scalability. Moreover, the communication overhead in such a system is lower [11]-[15]. The control structure is greatly influenced by the communication topology. Some examples of different communication topologies are the single bus communication architecture, the master-slave distributed architecture, and the ring architecture. For low galvanic isolation in parallel connected systems, the single bus architecture has been widely used in parallel connected DC/DC or AC/DC systems [13]-[16], [17]. The single-bus architecture can easily share data between each module with a very simple construction that is easy to

implement. However, the simultaneous transmission and reception between the master module and slave modules cannot be accessed through a single line, thereby reducing the communication speed. The master-slave distributed topology with bidirectional communication is usually used in cascaded DC/AC inverter systems [18], [19]. Since the control structure of the cascaded system is usually centralized, each module is relatively independent. The master-slave architecture shows a great advantage in terms of its clear division of the control function and the small communication delay from a master controller to a slave controller. However, the cost of such a communication system is quite high. Moreover, the number of communication ports on the master module increases with the number of the modules, thus increasing communication burden and cost of the master module [14]. The ring architecture proposed in [18] can solve the problem of galvanic isolation. All of the modules are connected to form a ring, thus reducing the voltage level between two adjacent modules.

Different communication protocols have been proposed for these systems. The EtherCAT protocol applied in MMC (Multi Module Converter) systems has been analyzed in [15] and [21]. Three potential control networks for the monitoring and control of power electronics converters, MACRO, PROFINETIRT and EtherCAT have been compared in [22]. By applying the ring communication architecture, the three protocols work under the master-slave mode. As a result, there is still no communication between the slave modules. As a result, there is not reduction in the communication burden of the master module. Adding communication between salve modules improves the communication structure [14].

All of the references discussed so far for the ring topology have considered the application of different communication modes for multi-pulse topologies such as cascaded H-bridge converters while studies on multi-module DC/DC converters are almost nonexistent. With the advent of new switching devices and the augmentation of switching frequencies, the footprint of low voltage (less than 1kV) transformer based DC/DC converters have been reduced dramatically when compared to high voltage systems. Hence, they can provide practical means for designing high voltage high power multi-module DC/DC conversion systems with a more compact size than single high voltage converter systems. In this paper the design feasibility of a micro unidirectional DC transmission system under the ring communication topology has been analyzed. The design objective of this study is to achieve the required DC transmission system with the smallest possible size at the lowest possible component cost. Such a system can be used to deliver power in the range of tens to hundreds of kilowatts across a few kilometers with a compact portable converter system connected through the smallest possible diameter wire to minimize the weight.

In this paper, taking a ring communication structure based on inter-module communication as an example, the
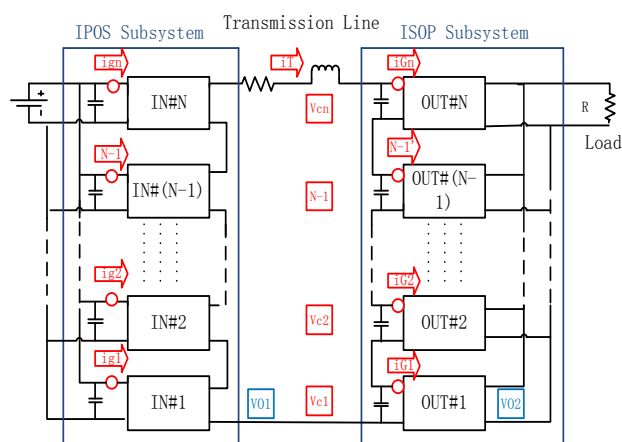

Fig. 1. IPOP conversion system.

communication structure applied to the design of a DC transmission system based on a IPOP converter consisting of several modules is analyzed. In addition, the influence of the communication delay is kept in focus while designing the control system to ensure a good bandwidth. Moreover, for a given limited baud rate of the microcontrollers in real applications, the largest number of connected modules in series communication is calculated to ensure the feasibility of the design.

This paper is organized as follows. In Section II, the characteristics of the IPOP conversion system are described including the topology and the communication structure. In Section III, the control of the IPOP converter system is designed using a linear model. In Section IV, the controller designed in Section III is applied to a nonlinear system, and simulation results are presented to validate the feasibility of the IPOP system adopting the ring communication structure. In Section V, the results of experiments are given to prove the feasibility of the design. Finally, Section VI concludes this paper.

II. SYSTEMATIC DESCRIPTION

The proposed IPOP system, shown in Fig. 1, consists of two subsystems: an IPOS DC/DC converter consisting of modules IN#x (x=1, 2… N) to step up the DC voltage, and an ISOP DC/DC converter system consisting of modules OUT#x to step down the output voltage to its original value. Both the step up and step down converter modules are identical systems and composed of transformer isolated full bridge forward converters.

The blue and red circles and squares in Fig. 1 depict the current and voltage measurement points, respectively. The red color represents the measurement point for each full bridge converter, while the blue color represents the measurement point for each subsystem. In order to minimize the space occupied by the high isolation voltage sensors, only the bottom
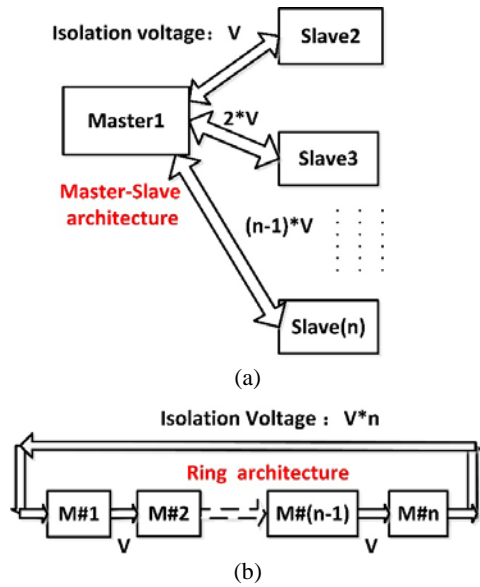
Fig. 2. (a) Master-Slave Structure. (b) Ring communication architecture.

modules IN#1 and OUT#1 measure the output voltage of each subsystem and the measured values are transmitted to other converter systems through the inter-module communication system. To select an inter-module communication architecture, once again the complexity, size and cost has been taken into account.

To further emphasize this point, Fig. 2(a) and 2(b) show the master-slave and ring communication architectures. In the master slave communication architecture, the galvanic isolation requirement for the communication interface from each module to the master module is equal to V*(n-1), where V is the output voltage of each module, and 'n' is module number. When compared to the master-slave architecture, the advantage of the ring architecture is the low requirement of the galvanic isolation since the galvanic isolation level from module to module is equal to V except for the first and last module where it is V*n. This characteristic can greatly help in reducing the size and cost of the ring based communication architecture. In addition, the expensive optical isolator with its optical cable can be replaced by a transformer based isolator.

Another aspect of ring based communication is its scalability. Ideally, if the communication rates are unlimited then adding more modules to a ring structure does not require any modification in the system hardware. Meanwhile, master-slave based systems are limited by the number of communication ports available in the master controller. This makes the system more compact as the number of modules increases.

In this paper, the case where each subsystem is made up of four full-bridge modules is considered, and each module delivers 10A at 300V nominal. With this setup, the high voltage DC link operates at 1200V as shown in Fig. 3. The two subsystems are connected through a 1Km transmission line, for which the inductance and resistance cannot be neglected.
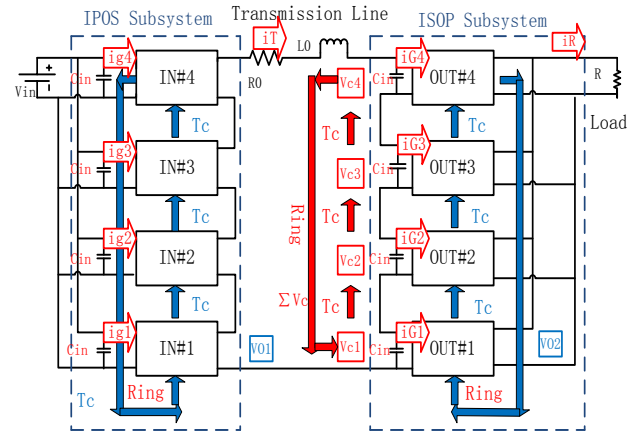

Fig. 3. IPOP conversion system adopting Ring communication structure

For each full bridge module, shown in Fig. 4(a), to make sure that the current is continuous under 10% of a nominal load and a switching frequency of 40 kHz, the inductance is designed as follows:

$$\mathrm{L} \geq \frac{(a*Vin - V_o)\mathrm{D}}{0.2 I_{on} f_s} = 1.25 mH \qquad (1)$$

The output capacitor is used as a filter combined with an inductance. On the one hand, considering the ESR and the size of the capacitor, normally a capacitor C_o of about 400$\mathbf{\mu}$F which has an ESR of about 1$\mathbf{\Omega}$ can keep the voltage ripple under 2V, with an acceptable size. On the other hand, the output capacitor influences the resonant frequency of the system. The inductance together with the output capacitor of the IPOS subsystem, the line inductance and the input capacitor of the ISOP subsystem form an LCLC circuit. The resonant frequencies should not be very high since this would influence the inner current loop. In addition, they should not be very low since this would increase the size of the RC compensation circuit used to damp the resonance which will be described in detail in Part D of Section 3. A better design is to control the resonant frequencies to be in the range of 100Hz to 1 kHz. Symmetrically, an identical input capacitor C_{in} of 400$\mathbf{\mu}$F together with C_o can meet these requirements, and the two resonant frequencies are 154Hz and 668 Hz.

The parameters for each converter module and the whole system are presented in Table I and Table II.

III. CONTROL DESIGN

The communication mode of the ring architecture greatly influences the design of the system controller. The ring architecture can adopt a master-slave communication mode. However, the communication rate requirement in such a case for the whole system will be quite high. To reduce the bandwidth requirement, inter-module communication and distributed implementation of the control algorithm are considered. For example, M#2 receives a message from M#1,

TABLE I
PARAMETERS OF A FULL-BRIDGE MODULAR CONVERTER

Input voltage (V_{in})	300 V
Rated output current (I)	10 A
Switching frequency (f_s)	40 kHz
Duty cycle (D)	1/3
Inductance (L)	1.25 mH
Output capacitor (C_o)	400 µF
Input capacitor (C_{in})	400 µF
Turn ratio (a)	N2/N1=1.5
Output voltage (V_o)	300 V

TABLE II
PARAMETERS OF THE WHOLE SYSTEM

Input voltage (V_{in})	300 V
Rated output current (4*I)	40 A
Line inductance (L_o)	1.2 mH
Line resistance (R_o)	0.1 **Ω**
IPOS Output voltage (V_{o1})	1200 V
Output voltage (V_{o2})	300 V
Load (R)	30/4 **Ω**
Load Current (i_R)	40 A

processes it and modifies a portion of it and then sends it to M#3. Each module executes on the message in a similar manner and finally the message loops back to M#1. For the conversion system, the whole control algorithm consists of three kinds of control loops, fast local control loops, fast global control loops, and slow global control loops. In such a design, the communication burden of each module is equalized in the ring architecture so that the communication requirement for the module communication controller is low. In comparison, in the master-slave architecture, the communication burden of the master module increases as the number of modules increases. However, in the ring architecture, the communication delay increases as the number of module increases. If the communication delay for two adjacent modules is Tc, then the delay from M#1 to M#K will be (k-1)*Tc (2≤k≤N). In this communication mode, with a limited communication rate, the influence of the communication delay on the control performance is quite significant.

Referring to Fig. 3, the communication delay is distributed in three control loops. For the output voltage control loop in the IPOS subsystem, only module IN#1 measures the output voltage. As a result, there is a communication delay from module IN#1 to the other three modules. For the output voltage control loop in the IPOS subsystem, there is communication delay from OUT#1 to the other three modules for the same reason. Moreover, in the voltage sharing loop of the ISOP subsystem, the input voltage is obtained by adding the input voltages of the four modules. As a result, there is also a communication delay when each module transmits the input voltage to OUT#1.

The overall design of the controller system has been conducted in five steps.

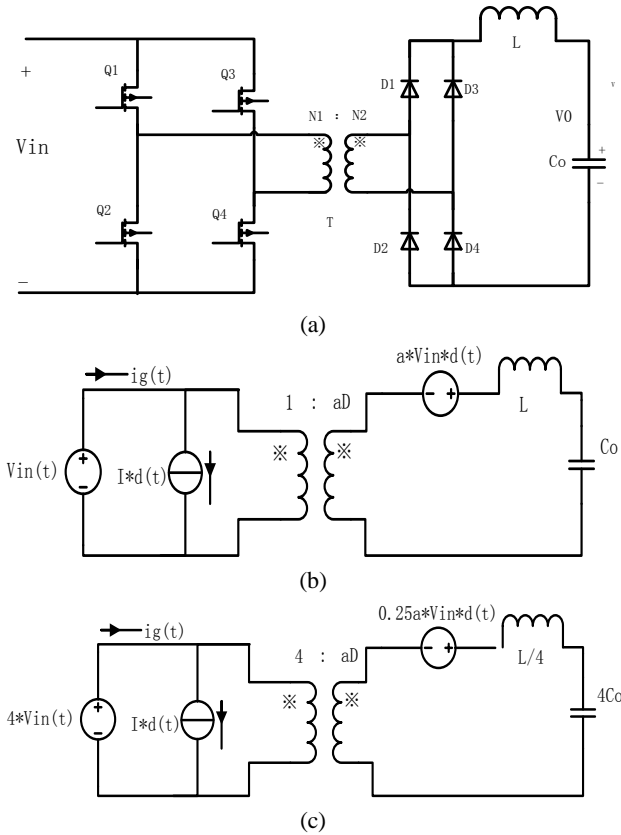1) Obtaining a small signal steady state model for the whole

Fig. 4. (a) Topology of a full-bridge converter. (b) Small signal model of the full-bridge converter. (c) Equivalent small signal model of the ISOP subsystem under stable operation.

system.

2) Designing the controller for the ISOP while considering a nominal load at its output and its input constant voltage.

3) Reducing the ISOP with a nominal load as a first order system.

4) Designing a passive network to convert the reduced ISOP + the transmission line + the output filter of the IPOS to a stable network.

5) Designing the controller for the IPOS while considering the rest of system as a load.

A. Small Signal Model of the ISOP Module

The small signal model has been discussed a lot due to its advantages in linearized analysis. One of these advantages is its ability to get the frequency response of the controller. For the sake of simplicity, the leakage inductance of the transformer of each module in the IPOP system is ignored. In real applications high frequency transformers are designed with an extremely small leakage inductance. Fig. 4(b) shows a small signal model of the full-bridge converter in Fig. 4(a) [23]. The signal with the script (t) represents the small signal variables. By replacing the small signal model with an actual circuit, an equivalent small signal model of the ISOP subsystem under stable operation is presented in Fig. 4(c).

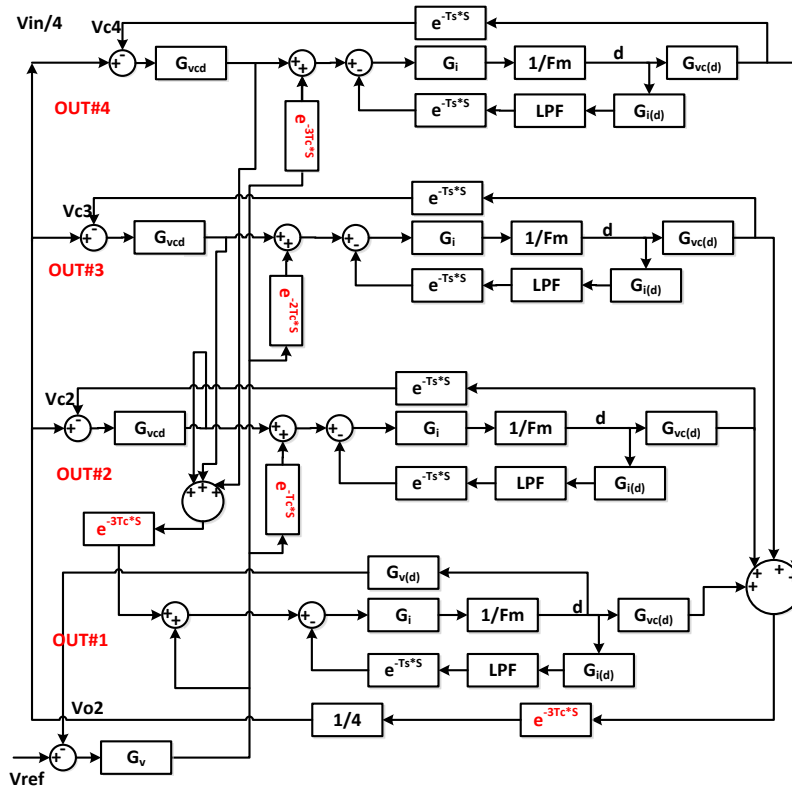As for the full-bridge converter small signal model in Fig.

Fig. 5. Control principle diagram of the ISOP subsystem.

4(b), there are three input signals (d(t), Vin(t), and io(t)); and two output signals (ig(t) and Vo(t)). It is a second-order system. The transfer functions from the input signals to the output signals are derived as follows:

$$(s^2 + \frac{1}{LC})i_g(s) = (Is^2 + \frac{aDV_{in}}{L}s + \frac{1}{LC})d(s)$$
$$+ \frac{a^2D^2}{L}sV_{in}(s) + \frac{aD}{LC}i_o(s) \quad (2)$$

$$CsV_o(s) = \frac{i_g(s) - Id(s)}{aD} - i_o(s) \quad (3)$$

$$G_{i(d)} = \frac{i_g(s)}{d(s)} = \frac{Is^2 + \frac{aDV_{in}}{L}s + \frac{I}{LC}}{s^2 + \frac{1}{LC}} \quad (4)$$

$$G_v = \frac{V_o(s)}{d(s)} = \frac{V_{in}}{LCs^2 + 1} \quad (5)$$

B. Control Strategy of the ISOP Subsystem

The control system of the ISOP subsystem consists of an input voltage sharing loop and an output voltage loop which are decoupled outside the inner current loop [6]. First the inner current tracking loop using the average current control strategy is designed to obtain as large a bandwidth as possible. This improves the bandwidth requirement for the output voltage loop. The output voltage loop is then designed based on the inner current loop to get the largest control bandwidth while ensuring stability. Finally, the balance control of the input

voltage of each module is designed. Fig. 5 is a control principle diagram which shows the control loops. Here Gi(d), Gvc(d) and Gv(d) represent the transfer functions from the duty cycle to the input current, input voltage and output voltage, respectively, for each module in the ISOP subsystem. Gi, Gvc and Gv represent the corresponding controllers. Fm presents the magnitude of the modulation wave, and a LPF (Low Pass Filter) is used to filter out the high frequency components in the sampling current.

For each measurement point, the sampling delay is the same, based on the common sampling frequency. It can be ignored when there is a communication delay related to the measured value because it is very small when compared to the communication delay. Ts and Tc represent the sampling time and the transmission time between two modules. For the output voltage loop, taking the first converter as the main converter which measures the output voltage and sending the obtained value to the next converter, the output voltage communication delay from the main module to other modules is $e^{-(k-1)Tc*s}$ ($2 \le k \le 4$). For the voltage sharing loop, the input voltage of the subsystem is first obtained by adding the voltage of the four modules. As a result, the average communication delay for each module getting voltage is e^{-3Tc*s}. Then, the control signal of the voltage sharing loop of OUT#1 is obtained by adding the output of the voltage sharing loop of the other three modules. The communication delay is also e^{-3Tc*s}.

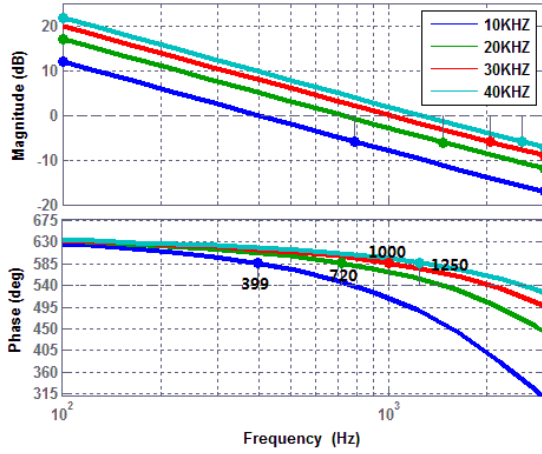*1) Inner Current Loop*: Since the inner current loop has the

Fig. 6. Open Bode plot of voltage loop of ISOP subsystem.

TABLE III
BANDWIDTH OF VOLTAGE LOOP OF ISOP SUBSYSTEM WHEN USING PI CONTROLLER

Communication frequency (Delay)	PI parameters (Kp, Ki)	Voltage control Bandwidth
10kHz (0.1ms)	Kp=1, Ki=2	0.801kHz
20kHz (0.05ms)	Kp=1.8, Ki=2	1.46kHz
30kHz (0.033ms)	Kp=2.5, Ki=2	2.05kHz
40kHz (0.025ms)	Ki=3.1, Ki=2	2.59kHz

Fig. 7. Equivalent Small signal model of the IPOS module.

largest bandwidth requirements, it is designed first. In the digital control system, the average current control shows that it has the advantages of reduced conducted noise and less harmonics. Therefore, the average current control is adopted. By regulating the P controller of the current loop, when Kp is 0.15, the phase margin is 48°, and the bandwidth of the current loop is 10kHz.

2) Output Voltage Loop: To ensure the load regulation of the output voltage loop, a PI controller is applied to the output voltage loop. The influence of the communication delay is analyzed. Fig. 6 gives an open loop bode plot of the voltage loop without loop compensation when considering the largest communication delay e^{-3Tc*s} under different communication frequencies. Take the communication frequency of each module as fs, Tc=1/fs. For linearization, the communication delay is simplified to a third order Pade approximation as:

$$e^{-\tau s} \approx pade(\tau,3) = \frac{1 - \frac{\tau s}{2} + \frac{(\tau s)^2}{8} - \frac{(\tau s^3)}{48}}{1 + \frac{\tau s}{2} + \frac{(\tau s)^2}{8} + \frac{(\tau s^3)}{48}} \qquad (6)$$

After the approximation, the phase of the voltage open loop begins at 720° at 0Hz. Phase margin from 540° to 720° is used to analyze the bandwidth.

To ensure at least a 45° phase margin, which means that the phase is at least 585° (540° + 45°), when the communication delay is 0.1ms, 0.05ms, 0.03ms, and 0.025ms, the crossing frequency needs to be 0.399kHz, 0.72kHz, 1.0 kHz, and 1.25kHz, respectively. Using a PI controller, the bandwidth results are presented in Table III. It can be concluded that as the communication delay increases, the bandwidth of the voltage control loop decreases significantly.

3) Input Voltage Sharing Loop Controller: If the input voltage of a converter changes, then the input voltage of the ISOP subsystem will change instantaneously. Therefore, the bandwidth of the sharing loop is kept much smaller than that of the voltage loop. Otherwise, it will interact with the voltage loop and make the control system unstable. By regulating the

PI controller, when the communication frequency is 20kHz, the output sharing loop controller is set to Kp=0.25, Ki=1, and the bandwidth is nearly 100Hz, which is less than 1/10 of that of the voltage loop.

C. Model Reduction of the ISOP Subsystem

Based on the previously mentioned system design structure, the ISOP subsystem is regarded as the load of the IPOS module. It is convenient to reduce the ISOP subsystem to a low order system in order to design the IPOS controller.

A method of balance realization [24] to simplify the ISOP subsystem is used to get an equivalent realization for which the controllability and observability where Grammians are equal and diagonal. The small entries of the diagonal elements indicate the states that can be removed to simplify the model. It is determined that for the ISOP subsystem, the diagonal entries are very small except for the first one. Therefore, the ISOP subsystem is reduced to a first order system. Finally, the first-order reduction of the ISOP subsystem under a nominal load is given as follows:

$$\frac{i(s)}{v(s)} = \frac{24.95s - 1334}{s + 2.457 \times 10^5} \qquad (7)$$

D. Design of the RC Branch to Damp the Resonance Point

Taking the reduced ISOP module as the load, an equivalent small signal model of the IPOS module under stable operation is shown in Fig. 7. The ISOP subsystem is reduced under a nominal load. In Fig. 8(a), the model contains a LCL resonance filter and a load which changes with the frequency, giving two resonance points. Since the voltage control loop bandwidth is not very large, to damp the resonance points, a passive damping method using a series connected RC branch, as shown in Fig. 8(b), is applied to avoid destabilization due to the aforementioned resonant points.

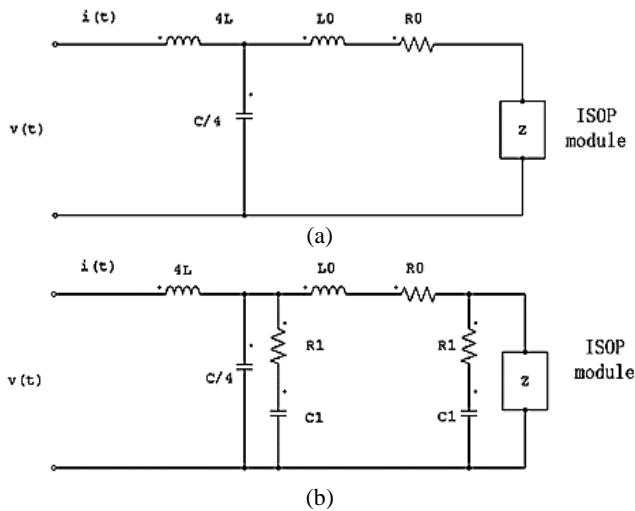A comparison of the resonance points before and after

(a)

(b)

Fig. 8. (a) LC resonance circuit of the system. (b) RC branches added to the system.
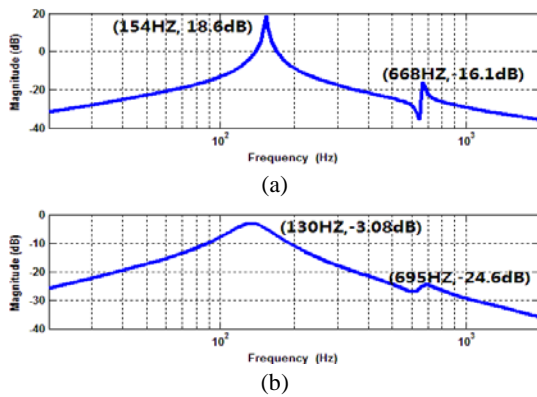

(a)

(b)

Fig. 9. (a) Resonance points of the original system. (b) Damping of resonance points by adding RC branches.

compensation is shown in Fig. 9. The original system has two resonance points, f1=154Hz and f2=670Hz as shown in Fig. 9(a). After adding the RC branches to the system (R1=20Ω, C1=100uF), the two resonance points are damped to a great extent which can be concluded from Fig. 9(b).

E. Control Design of the IPOS Subsystem

After applying the common ratio control method to the IPOS subsystem [2], a small signal diagram of the complete IPOS subsystem is shown in Fig. 10. The implication of each block is the same as that in the ISOP control principle diagram. Since the DC link voltage is only sampled by the first module IN#1, the influence of this delay is significant in the voltage loop and it is represented by the red colored exponential terms.

1) Inner current loop of the IPOS subsystem

Using the same method as the current control of the ISOP module, the P controller is designed as P=0.04. The phase margin is 46.6°, and the bandwidth is 8.97 kHz.

2) Outer voltage loop of the IPOS subsystem

Using the same method as the voltage loop control of the ISOP subsystem, the communication delay of the control
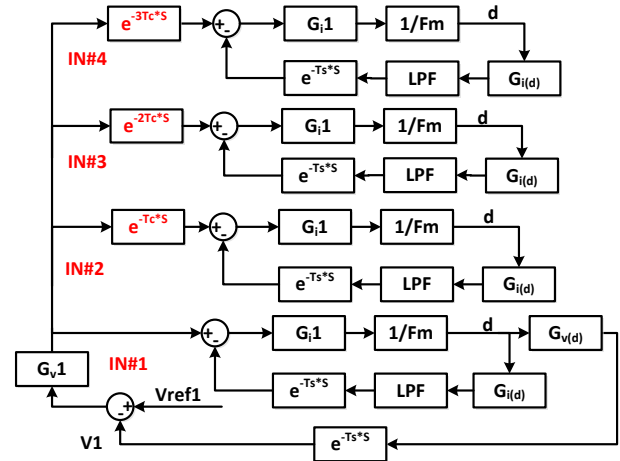

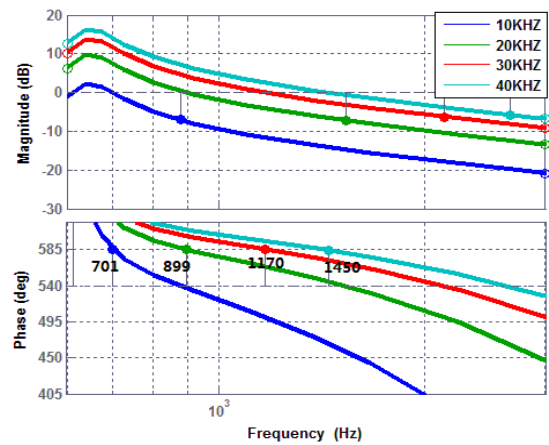Fig. 10. Control diagram of the IPOS subsystem.

Fig. 11. Open Bode plot of voltage loop of IPOS subsystem without compensation.

TABLE IV
BANDWIDTH OF VOLTAGE LOOP OF IPOS SUBSYSTEM WHEN USING PI CONTROLLER

Communication frequency (Delay)	PI parameters (Kp, Ki)	Voltage control Bandwidth
10kHz (0.1ms)	Kp=0.63,Ki=2	0.836kHz
20kHz (0.05ms)	Kp=1.5, Ki=2	1.35kHz
30kHz (0.033ms)	Kp=2.4, Ki=2	2.07kHz
40kHz (0.025ms)	Ki=3.2, Ki=2	2.66kHz

system is analyzed. To ensure at least a 45° phase margin and a 6dB gain margin, when the communication delay is 0.1ms, 0.05ms, 0.033ms, and 0.025ms, the crossing frequency is 0.701kHz, 0.899kHz, 1.17kHz, and 1.45kHz, as shown in Fig. 11. Using a PI controller, the bandwidth results are presented in Table IV.

The analysis presented in this section can be extended to a higher number of modules. Considering a practical situation, if a microcontroller with a baud rate of 4Mbits/s is used in each module, and the data length is within 10 bytes in the data frame shown in Fig. 12, in which the reserved data area contains the necessary control signals for the module itself, while the public data area contains signals which contribute
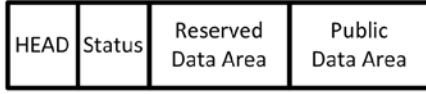
Fig. 12. Data frame used in the ring communication structure .

TABLE V
THE CONTROL BANDWIDTH UNDER DIFFERENT BAUD RATE OF
MCU AND NUMBER OF MODULES

Baud rate of MCUS (fc) Number of Modules	2M (25K)	4M (50K)	8M (100K)
	Voltage control bandwidth		
4	1.79kHz	3.23kHz	5.18kHz
8	0.84kHz	1.54kHz	2.77kHz
12	0.56kHz	1.04kHz	1.96kHz

to the control of the whole system, the transmission frequency of each module can reach as much as fs=4*106/ (10*8) =50 kHz. According to Table V, this kind of microcontroller can achieve bandwidth as high as 1 kHz even when 12 modules are connected in the IPOP DC transmission system. The control speed is ensured when the transmission power grows 12 times that of a single module. For this baud rate, multiple low-cost microcontrollers can be used to realize it, increasing its feasibility and utility.

IV. SIMULATION RESULTS OF THE NONLINEAR SYSTEM

The simulation of the nonlinear system is conducted in SIMULINK in three steps. First, the ISOP subsystem is simulated separately with input and output disturbances, and the voltage balance control is verified by giving a current disturbance to the input capacitance of OUT#1. Second, the reduction of the ISOP subsystem is taken as the load of the IPOS subsystem to conduct a simulation of the IPOS converter to verify the validity of the method of model reduction for the ISOP subsystem. Finally the two subsystem are connected to verify the effectiveness of the design method of the IPOP system and the stability of the control system. The parameters for the converter are given in Table I and Table II. Referring to the design of the linear system under a communication frequency of 20 kHz in section II, the PI controller parameters are given in Table VI.

A. Simulation of the ISOP Subsystem (Input Voltage: 1200V, Output Voltage: 300V)

According to the ISOP subsystem in Fig. 1, the red circles (iG1, iG2, …, iG4) and red squares (Vc1, Vc2, …,Vc3) represent the input current and input voltage of each module, respectively. Meanwhile, the blue squares (Vo1, Vo2) represent the output voltage of the subsystem. Three independent disturbances are given to the ISOP subsystem to verify the stability of the control system, namely an input

TABLE VI
CONTROL PARAMETERS OF THE NONLINEAR SIMULATION

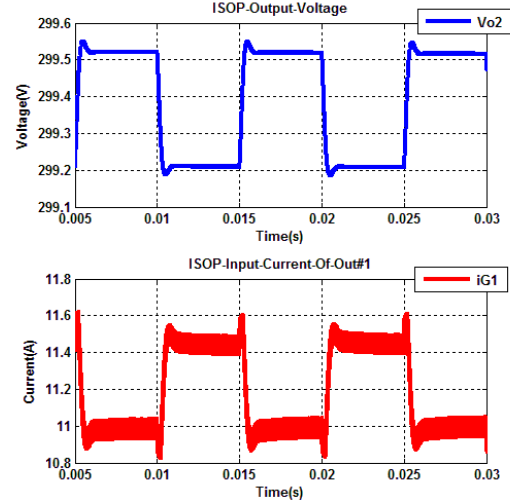| Control loop	ISOP subsystem	IPOS subsystem
Current loop	Kp=0.015	Kp=0.04
Voltage loop	Kp=1.8,Ki=2	Kp=1.5,Ki=2
Voltage sharing loop	Kp=0.25,Ki=1	None

Fig. 13. ISOP output voltage and input current under input voltage disturbance.

voltage disturbance to the DC link, an input current disturbance to OUT#1, and an output current disturbance.

1) Simulation results of the ISOP subsystem with ±10% (±120V) input voltage disturbances of 100Hz are given in Fig. 13. From the simulation results, the response time of the output voltage of the ISOP subsystem is within 1ms. The DC regulation under the disturbances is quite low (within 0.5%). The input current of IN#1 is a little higher than the nominal current mainly due to the fact that the transformer is not ideal, and given an exciting current of approximately 0.3A, the simulation results will be more similar to real applications.

2) Simulation results of the ISOP subsystem are given in Fig. 14 with an input current disturbance of 1A at t=2s to module OUT#1. To present substantial differences with various module parameters, the parallel parasitic resistance of the input capacitance of each module is kept different: 500Ω for OUT#1, 400Ω for OUT#2, 300Ω for OUT#3, and 200Ω for OUT#4. From the simulation results, the input voltage of each module of the ISOP subsystem fluctuates within 3V which is less than 1% of the nominal input voltage. Finally they become equal to each other to keep the balance. This proves the effectiveness of the voltage sharing control loop of the ISOP subsystem.

3) Simulation results of the ISOP subsystem with ±10% (±1A) output current disturbances of 100Hz are given in Fig. 15. From the simulation results, the response time of the output voltage of the ISOP subsystem is within 1ms. The load regulation under the disturbances is quite low (within 0.5%).
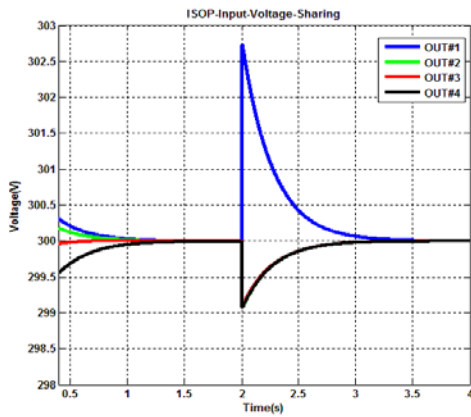
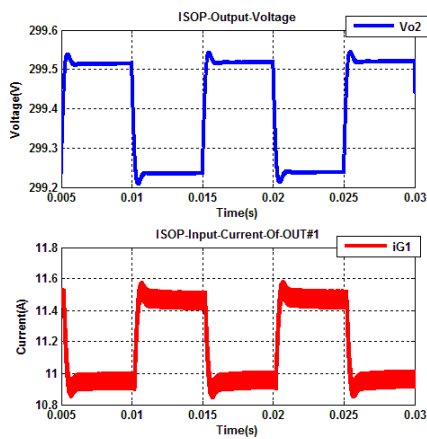Fig. 14. ISOP input voltage sharing under input current disturbance.

Fig. 15. ISOP output voltage and input current under output current disturbance.

B. Simulation of the IPOS Subsystem (Input Voltage: 300V, Output Voltage: 1200V)

The reduction of the ISOP subsystem is taken as the load of the IPOS subsystem. When a $\pm 10\%$ ($\pm 30V$) input voltage disturbance is given to the IPOS subsystem, the simulation results are shown in Fig. 16. The response time of the IPOS output voltage is within 1ms, and the DC regulation is quite low (within 0.5%).

C. Simulation of the Whole IPOP Subsystem (Input Voltage: 300V, Output Voltage: 300V)

Referring to Fig. 1, the ISOP subsystem is connected to the IPOS system to constitute the entire IPOP system. An input voltage disturbance and output current disturbance are given to the IPOP converter to verify the stability of the control system of the whole system.

1) Simulation results of the initial start-up of each module are shown in Fig. 17. For the two step conversion system in real applications, first the IPOS subsystem starts up after the input capacitor is charged to its nominal input voltage. The ISOP subsystem cannot start up until the input voltage reaches a voltage level around the nominal input voltage. As
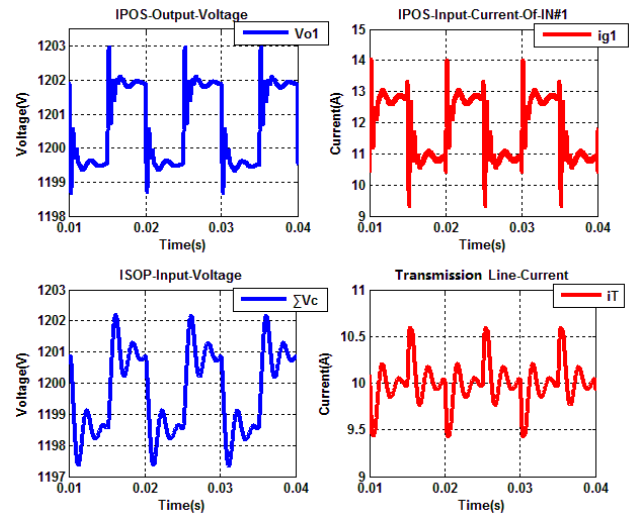

Fig. 16. Simulation results of IPOS subsystem under input voltage disturbance.
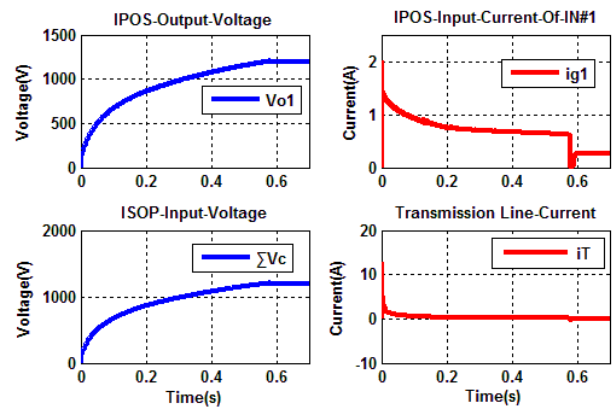

Fig. 17. Simulation results of initial start-up of IPOP system.

can be seen from Fig. 17(a), to avoid over current protection, first the constant current control is applied for the initial start-up of the IPOS subsystem, and when the output voltage reaches its nominal value (1200V), the voltage control takes over the current control to keep the input voltage of the ISOP subsystem stable. Then the control of the whole system begins by setting a slow ramp reference output voltage. The initial voltage balancing of the ISOP subsystem is ensured by balancing the resistances which can be disconnected afterwards.

2) Simulation results of the IPOP system with $\pm 10\%$ ($\pm 30V$) input voltage disturbances of 100Hz are shown in Fig. 18. As can be observed from the simulation results, the voltage and current in the first four plots of Fig. 18 are very similar to those in Fig. 16. This validates the method of model reduction used for the ISOP subsystem. Moreover, from the last two plots of Fig. 18, the DC regulation is within 1/3000, which is much less than that in the ISOP subsystem. As for the IPOP system, input disturbances are damped twice through the IPOS and ISOP subsystems. In this way, high DC regulation is ensured.
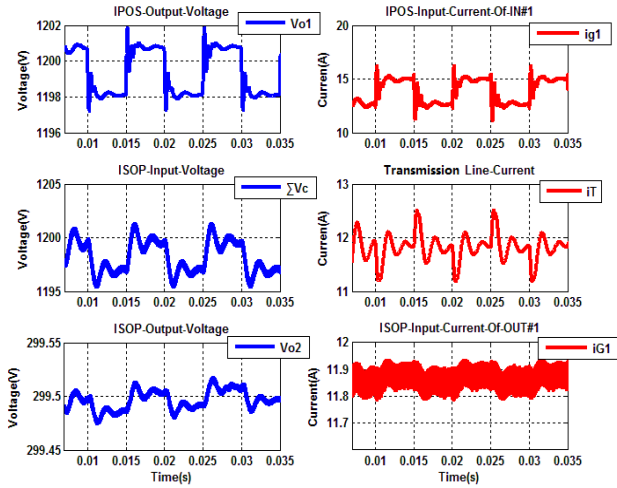
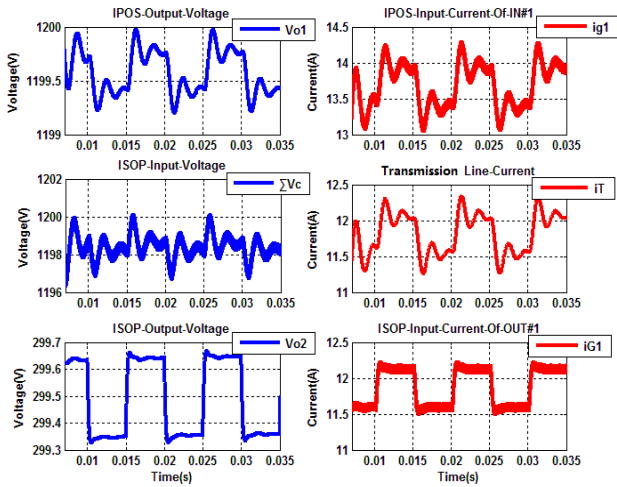Fig. 18. Simulation results of IPOP system under input voltage disturbance.

Fig. 19. Simulation results of IPOP system under output current disturbance.
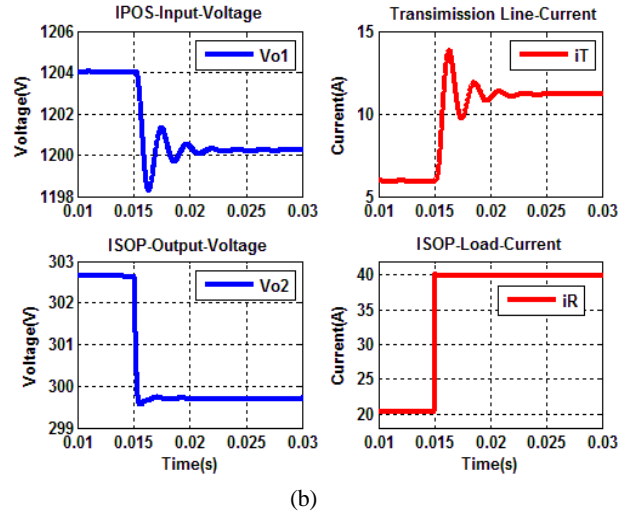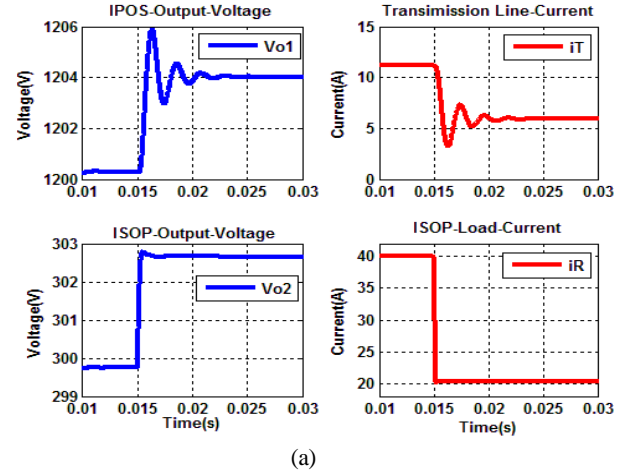

(a)

(b)

Fig. 20. (a) Simulation results of IPOP system with high load change from nominal load to half load. (b) Simulation results of IPOP system with high load change from half load to nominal load.

3) Simulation results of the IPOP system with ±10% (± 1A) output current disturbances of 100Hz are shown in Fig. 19. From the simulation results, it can be seen that the load regulation is small (within 1/1000) and the response time of the ISOP output voltage is within 1ms.

4) Simulation results of the IPOP system with large sudden load changes of about half the nominal load are shown in Fig. 20. The load changes from a nominal load (40A) to half a load (20A) and vice versa. After a very short transient with very little overshooting, the ISOP output voltage and load current go into a new stable state. The response time is less than 1ms, and the load regulation is within 1%.

The simulation results show the stability and rapid response of the control system designed for a linear system. A PI controller is applied to ensure the DC regulation and load regulation. The bandwidth analysis in the linear system is related to the response time of the current and voltage in the nonlinear system. This proves the feasibility of using the ring communication structure to design an IPOP DC/DC conversion system in practical applications.

V. EXPERIMENT RESULTS

To verify the operation and performance of the proposed control system of the IPOP converter, a 4.8 kW system was built consisting 8 modules as previously described with a hundred volts in the DC link for safe operation. The proposed design has been tested in a laboratory prototype as shown in Fig. 21. The specifications of each converter are nearly the same as the proposed design.

In terms of implementation, the common mode disturbance voltage increases as the number of connected modules increases. Therefore, the common mode inductor should be added separately. The power supply of each controller board comes from the input capacitor of each module, so that a small power switching power supply module is needed. For the ISOP subsystem, the balancing resistance of each module is
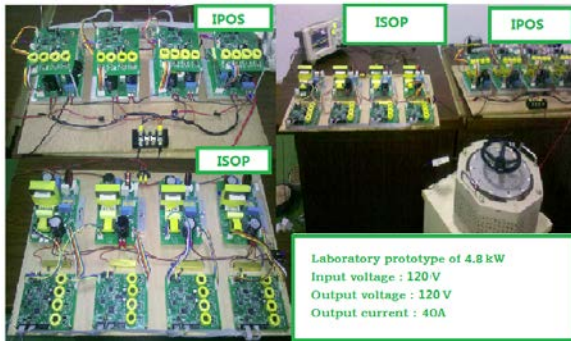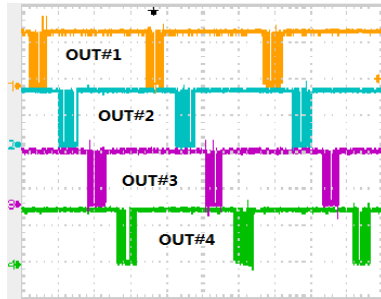
Fig. 21. The 4.8 kW IPOP converter laboratory prototype.

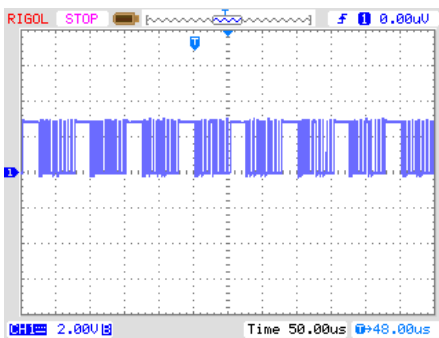Fig. 22. Four-Module Single-Frame mode Ring communication waveform

Fig. 23. Continuous mode Ring communication waveform.

indispensable for input voltage sharing when starting up. However, it can be disconnected afterwards.

The inner communication module of the DSPIC with a baud rate of 1.86 MHz is applied to the ring communication structure, and the data length is 8 bytes. Therefore, the theoretical transmission frequency is about 30 kHz. To better illustrate the characteristics of ring communication, the waveform of a single data frame transmitted during a cycle is shown in Fig. 22. Since the data transmission is triggered by DSP interrupts, the interval between the transmissions of two nearby modules is spent on data processing and calculation before a transmission interrupt occurs. Therefore, the real transmission frequency is less than the calculated value in real applications. However, with MUCS of high performance computing, the interval can be ignored. In this experiment, the transmission frequency is finally about 15 kHz, which can be deduced from Fig. 23. This shows the continuous data frame transmission. A new data frame is generated and transmitted about every 70us.
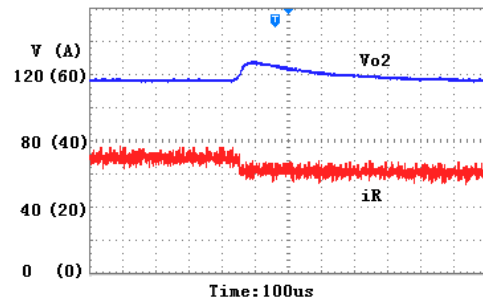
(a)
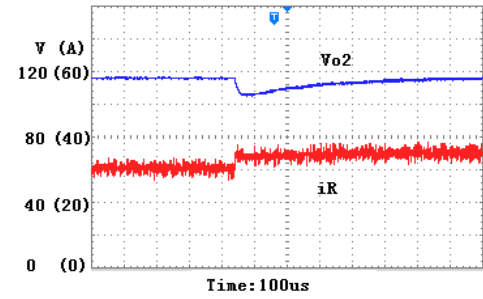
(b)

Fig. 24. (a) Step responses of output voltage and load current of IPOP converter with 12.5% fall step load change. (b) Step responses of output voltage and load current of IPOP converter with 12.5% rise step load change.
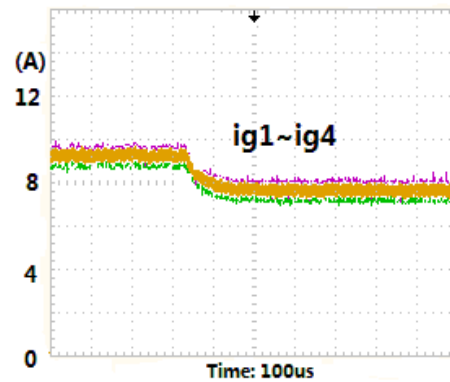
(a)
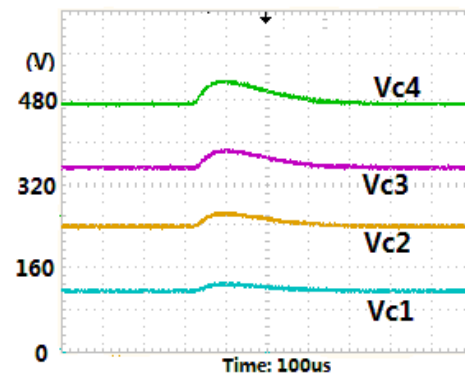
(b)

Fig. 25. (a) Step responses of input current of each converter of IPOS subsystem with12.5% fall step load change. (b) Step responses of input voltage of each converter of ISOP subsystem with 12.5% fall step load change.

The response waveforms of the output voltage and current when a sudden load disturbance with $\pm 12.5\%$ of a nominal load (between 30A and 35A) is applied are shown in Fig. 24. The load regulation is quite small, within about 1%, and the response time is within 1ms.

To show the current and voltage balance of the IPOS and ISOP subsystems, when the load is reduced by 12.5%, the current waves of each converter of the IPOS subsystem and the input voltage waves of the ISOP subsystem with respect to the low voltage ground are shown in Fig. 25. As can be seen in Fig. 25(a), the input current of each converter comes to a new steady state within 1ms. The magnitude of the ripple of the input voltage of OUT#4 in Fig. 25(b) is about four times that of OUT#1 because four converters are connected in input-series.

From the experiments results above, it can be seen that the proposed idea of applying the ring communication structure to a multi-module DC-DC converter is of great feasibility. Multiple low cost microcontrollers like the DSPIC can easily achieve the requirements of ring communication. The current and voltage balance problems can be solved by a control system designed based on the communication structure. The DC-DC converter system shows great expandability by increasing the number of converters connected in the IPOS and ISOP subsystems to increase the transmission power at a low cost.

VI. CONCLUSION

Simulation and experiment results indicate that the ring communication architecture is an attractive solution for IPOP DC/DC conversion systems. It solves the problem of galvanic isolation in centralized master-slave communication. In addition, communication between modules directly reduces the communication overhead.

One of the challenges in using the ring communication structure for the control of DC/DC conversion systems is the limit on the control bandwidth. The analysis of the influence of the communication delay on the stability and performance of the control system is of great importance. An effective methodology has been presented here in which the largest control bandwidth ensuring a phase margin and gain margin is analyzed using a small signal model. Then the baud rate of the MCU is chosen based on the number of connected modules and the expected control speed. Since readily available off-the-shelf MCUs with low baud rates can be used to realize such systems, practicality and cost effectiveness make these systems feasible. The performance of these systems in simulation and experiment results further supports their feasibility.

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