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A Wide Frequency Range LLC Resonant Controller IC with a Phase-Domain Resonance Deviation Prevention Circuit for LED Backlight Units

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Abstract

This paper presents a wide frequency range LLC resonant controller IC for LED backlight units. In this paper a new phase-domain resonance deviation prevention circuit (RDPC), which covers a wide frequency and input voltage range, is proposed. In addition, a wide range gate clock generator and an automatic dead time generator are proposed. The chip is fabricated using 0.35 μm BCD technology. The die size is 2 x 2 mm2. The frequency of the clock generator ranges from 38 kHz to 400 kHz, and the dead time ranges from 300 ns to 2 μs. The current consumption of the LLC resonant controller IC is 4 mA for a 100 kHz operation frequency using a supply voltage of 15 V.

Key words: Backlight unit, Clock generator, Dead time, LED driver, LLC resonant controller, Prevention Circuit (RDPC), Resonance Deviation, Wide range

I. INTRODUCTION

In recent years, Liquid Crystal Display (LCD) flat panels have become one of the fastest growing markets in large screen displays due to their various advantages, such as a low power consumption, long lifespan, low profile and high contrast ratio [1], [2]. Since LCDs are non-emissive display devices, they usually require a Back Light Unit (BLU) for monitor or TV applications. Recently, Light-Emitting Diodes (LEDs) have become one of the most promising candidates for BLUs and other lighting applications [3]. Since power consumption is directly related to the screen size in an LCD backlighting system, the demand for large screen LCDs and high power density is gradually increasing. As a result, a variety of higher-power topologies have been considered in order to achieve high efficiency in a compact space with low-EMI generation. LLC resonant converters are popularly adapted to consumer and industrial electronics due to their inherent advantages over contending topologies [4]-[7]. Such advantages enable highly efficient operation over a wide input voltage range as a consequence of the very low switching losses found in zero voltage switching (ZVS) conditions. In addition, these converters are suitable for integration, since the two inductors required to form an LLC tank can be integrated into one magnetic core without the need for extra components [10]-[13].

The architecture of the proposed wide range LLC resonant controller IC is discussed in Section II, and the building blocks are described in Section III. Sections IV and V present the simulation and measurement results and the conclusion, respectively.

II. THE PROPOSED LLC RESONANT CONVERTER SYSTEM ARCHITECTURE

Fig. 1 shows the proposed half-bridge LLC resonant LED driving circuit. The LLC resonant controller IC is located on the primary side.

Fig. 2 shows the DC gain characteristics of the LLC converter. When the switching frequency is higher than the resonant frequency (f_O), the voltage gain of the LLC resonant converter is always less than one. Thus, the Zero Voltage

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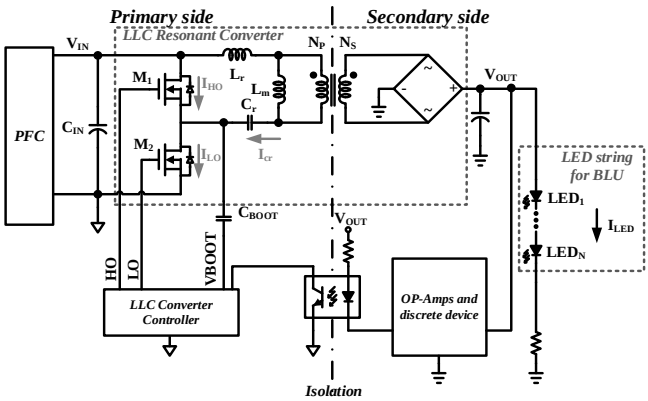

Fig. 1. The proposed half-bridge LLC resonant converter.

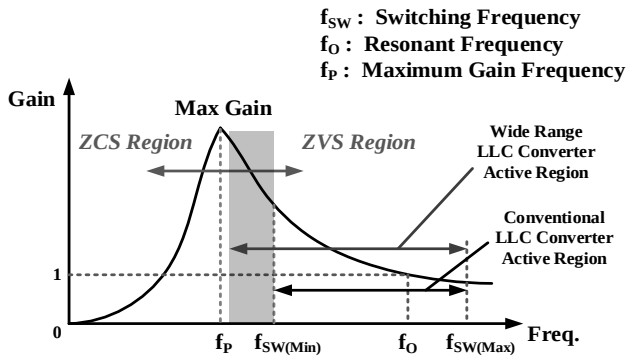

Fig. 2. The DC gain characteristics of the LLC resonant converter.

Switching (ZVS) mode can be achieved. When the switching frequency is lower than the resonant frequency (f_O), either the ZVS or Zero Current Switching (ZCS) modes can be achieved [5].

As a result, the converter must be operated at a frequency higher than f_P, which depends on the value of Q, so that it can always work in the ZVS region.

Eq. (1)-(3) represent the resonant frequency (f_O) and the minimum frequency (f_P) needed to achieve the ZVS mode for different load conditions and quality factors (Q), respectively. f_{sw} is the operating frequency of the converter.

$$f_O = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1}$$

$$f_P = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{2}$$

$$Q = \frac{\sqrt{L_r/C_r}}{R_{LOAD}} \tag{3}$$

The operating frequency of the LLC resonant converter must operate in the ZVS region. When the operating region enters the ZCS region, the external Power FET can break down because of the inrush peak current which flows into the back gate diode. To compensate for this defect, previously proposed LLC resonant converters were limited to a minimum frequency to limit the maximum gain.

Fig. 3(a) and 3(b) show a timing diagram during the resonance deviation region operation and the normal region operation, respectively. Fig. 3(a) and 3(b) show a timing diagram in the resonance deviation region operation and the normal region operation, respectively. Fig. 3(a) shows the operation in the resonance deviation region. During the high duration of the HO signal, the I_{HO} current decreases after reaching its maximum value. The resonant current, I_{Cr}, changes from positive to negative. In this state, if HO is at a low level, the current goes through the parasitic diode of M_1 in Fig. 1 because of the forward bias. If the LO signal is at a high level, the parasitic diode of M_1 in Fig. 1 goes in to the reverse recovery mode because of the reverse bias. In the reverse recovery mode, the impedance of the M_1 parasitic diode momentarily becomes very low and a peak current occurs. Therefore, M_1 is damaged, as shown in Fig. 1.

During a high level state of LO, the I_{LO} current decreases after reaching its maximum value. As shown in Fig. 3 (a), the

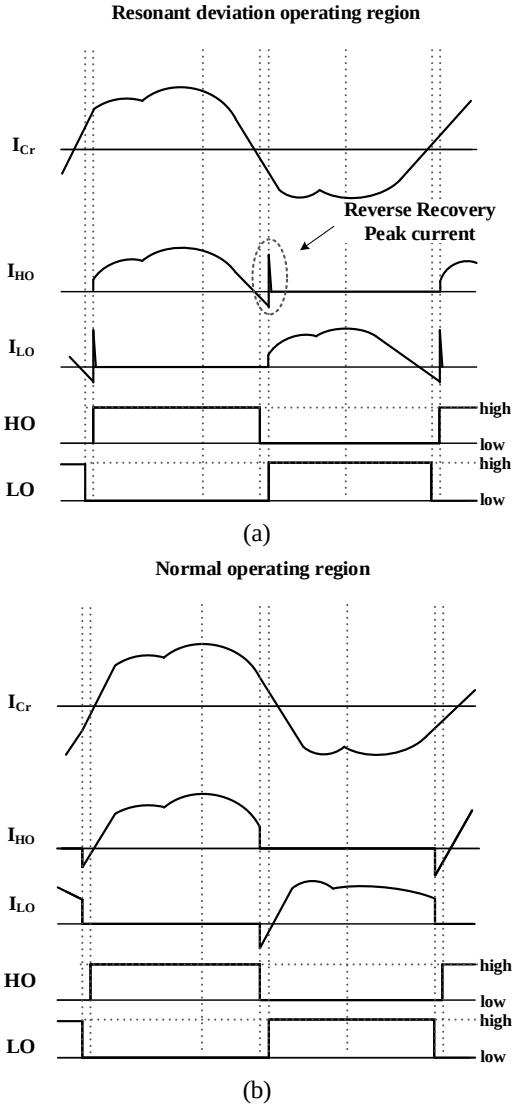

Fig. 3. Timing diagrams of LLC converter operating region. (a) Resonance deviation operating region. (b) Normal operating region.

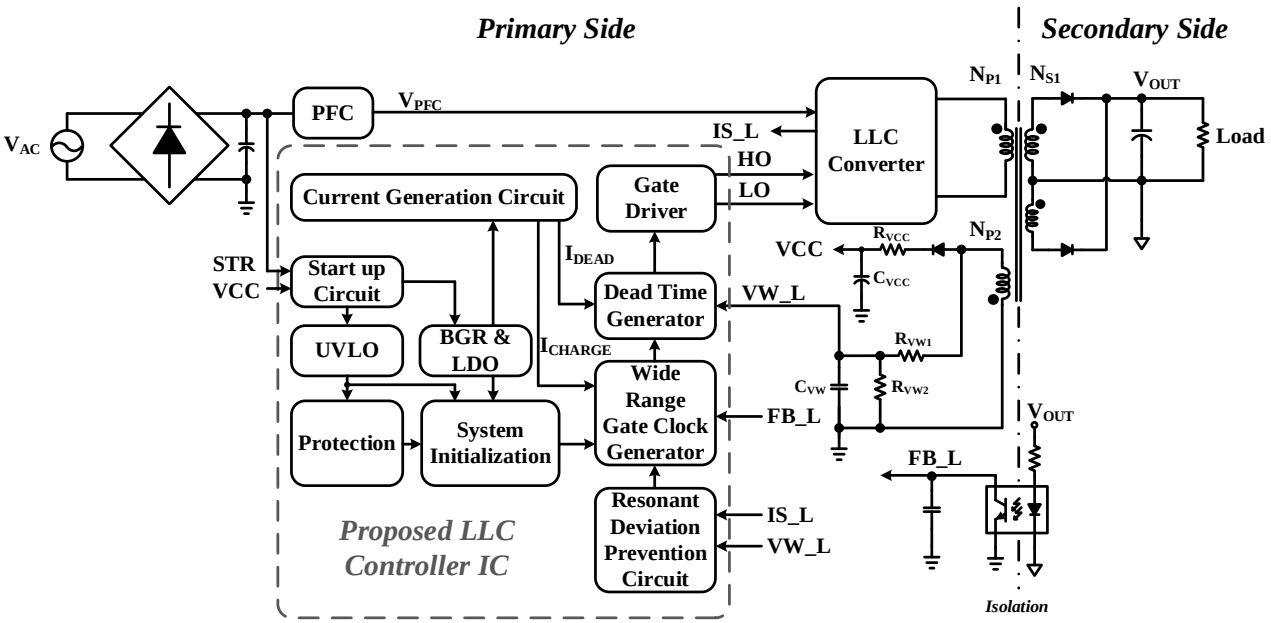

Fig. 4. The architecture of proposed half-bridge LLC resonant converter system.

resonant current, I_{Cr}, changes from negative to positive. In this state, if the LO signal is low, the current goes through the parasitic diode of M_2 in Fig. 1 because of the forward bias. If HO is at a high level, the parasitic diode of M_2 in Fig. 1 is put in the reverse recovery mode because it meets the reverse bias condition. In the reverse recovery mode, the impedance of the M_2 parasitic diode momentarily becomes very low and a peak current occurs. Therefore, M_2 can be damaged, as shown in Fig. 1.

Fig. 3(b) shows the operation in the normal region. During a high level state of HO, the I_{HO} current decreases after reaching its maximum value. If I_{HO} is positive and turns off the HO signal, the current goes through the parasitic diode in M_1 in Fig. 1 because the parasitic diode of M_1 is in the forward bias condition.

If the HO signal is at a high level, the resonant current, I_{Cr}, changes continuously. During a high level state of LO, the I_{LO} current decreases after reaching its maximum value. If I_{LO} is positive with a low level LO, the current goes through the parasitic diode of M_2 in Fig. 1 because of the forward bias. If HO is at a high level, the resonant current, I_{Cr}, changes continuously. As a result, if the I_{Cr} signal is positive, the HO signal is high. However, LO signal is high and the LLC converter operates in the ZVS region, if the I_{Cr} signal is negative. The maximum gain of the LLC converter can be achieved by adding a circuit that senses the I_{Cr} signal to limit the minimum switching frequency. The proposed LLC resonant controller IC protects the circuit by limiting the switching frequency at which it receives feedback from the resonant state of the LLC converter. Therefore, the proposed LLC resonant converter can achieve a much higher gain when compared to previous designs.

Fig. 4 shows the detailed architecture of the proposed LLC controller IC. The proposed LLC controller IC is composed of a Resonance Deviation Prevention Circuit (RDPC), a wide range gate clock generator, a dead time generator, a startup circuit, a gate driver, a protection circuit, a current generation circuit, a system initialization circuit, a BandGap Reference (BGR), a Low Drop Out (LDO) and an Under Voltage Lock Out (UVLO). When the VCC voltage is higher than the Under Voltage Lock Out (UVLO) level and the operating condition is normal, the system initialization is operated by the internal LDO. The cross conduction problem is critical in the design of the SMPS (Switched-Mode Power Supply), because many switching circuits fail to meet the necessary performance requirements due to this problem.

Cross conduction results in premature transistor failure, excessive output noise, low efficiency and excessive heat [8]. The most common method used to prevent cross conduction is to provide a dead time between the complementary driving pulses, HO and LO, in order to turn off both of the transistors at the same time. The duration of this dead time is designed to be long enough to assure that the conduction states of the power MOSFETs, M_1 and M_2 from Fig. 1, do not overlap under any circumstances. In addition, the minimum duty ratio of the complementary driving pulses needs to be guaranteed for each switching cycle due to the body diode conduction time of the power MOSFETs [9]. Therefore, a typical dead time is several percent of the driving time in order to insure a safe operating margin. This limits the range of the PFM control. In this paper, a new dead time generator based on a mono-stable structure is proposed for robust operation with respect to variations.

Accordingly, the proposed LLC controller IC is based on a frequency feedback control system in order to regulate its output.

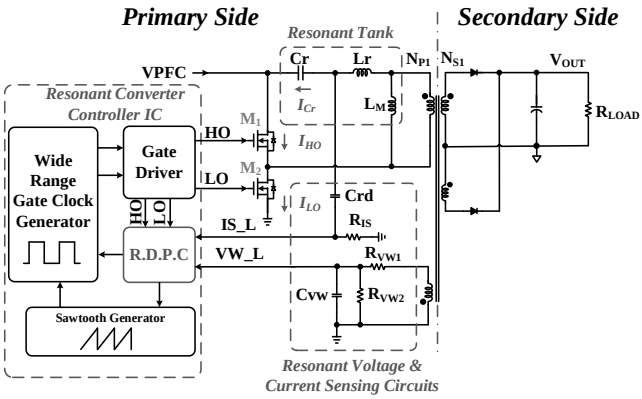

Fig. 5. Detailed block diagram of the LLC resonant converter system including RDPC.

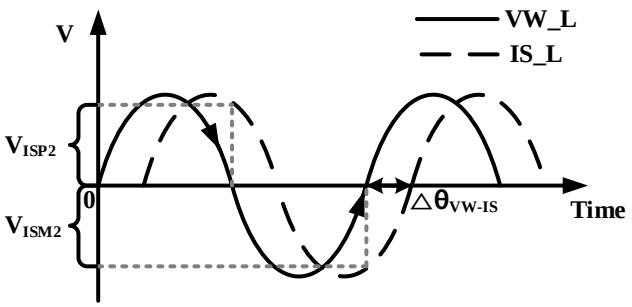

Fig. 6. The conceptual diagram of RDPC function.

III. THE BUILDING BLOCKS

A. The Resonance Deviation Prevention Circuit

The LLC resonant converter uses a Resonance Deviation Prevention Circuit (RDPC) to achieve the minimum switching frequency and to guarantee operation in the ZVS region.

Fig. 5 is a block diagram of the RDPC that is applied to the LLC Resonant Converter. The RDPC can maximize the operating frequency range of the LLC resonant converter. If the inductance and capacitor in the LLC resonant tank are varied, the RDPC controls the operating frequency adaptively. Because the frequency range of the LLC converter is widened, the corresponding voltage ranges of the input and output are also increased. Thus, the LLC converter can be applied to various applications. The operation of the RDPC is explained below. Fig. 6 shows a conceptual diagram of the RDPC. Since the LCC resonant converter should operate in the ZVS region, the phase of the IS_L voltage lags the VW_L voltage. θ_{VW-IS} represents the phase difference between the VW_L voltage and the IS_L voltage.

When the VW_L voltage crosses 0 V, the RDPC circuit detects the level of the IS_L voltage. The IS_L voltage should be positive when the VW_L voltage changes from positive to negative.

On the other hand, the IS_L voltage should be negative when the VW_L voltage changes from negative to positive. In the RDPC circuit, the voltage levels of V_{ISP2} and V_{ISM2} are pre-defined so that θ_{VW-IS} cannot be less than the pre-defined levels. This guarantees that the LLC resonant converter operates in the ZVS region.

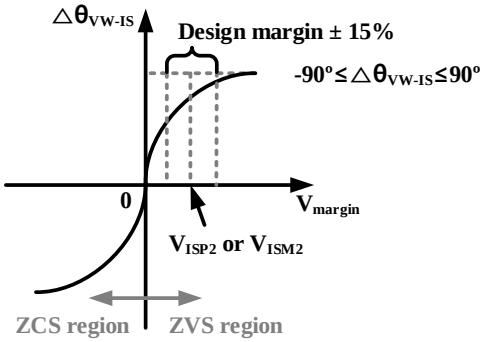

Fig. 7. The phase θ_{VW-IS} vs the level of V_{ISP2} or V_{ISM2}.

Fig 7 shows the phase difference between VW_L and IS_L with respect to the design margin factors for V_{ISP2} or V_{ISM2}. When the phase difference θ_{VW-IS} is positive, the LLC resonant converter operates in the ZVS region.

The margin levels of V_{ISP2} and V_{ISM2} were pre-defined and verified through a post layout simulation. The LLC resonant converter was operated in the ZVS region with respect to Process, Voltage, Temperature (PVT) variations of ±15 %. The resonant frequency (f_p) of the LLC resonant converter is determined by L and C in the resonant tank, whose variations can be covered by the design margin in the LLC resonant controller IC.

The RDPC detects the resonant current with the capacitor, C_{rd}, of the LLC resonant converter at the IS_L terminal. In addition, it detects the resonant voltage of the transformer at the VW_L terminal using the voltage division between R_{VW1} and R_{VW2}. The voltage of VW_L is the resonant voltage signal and voltage of IS_L is the resonant current signal of the LLC converter. If the LLC converter operates in the ZVS region, the characteristic of the resonant tank of the LLC converter is inductive. From this, the slope of the voltage of IS_L can be determined using the voltage of VW_L. In other words, if the voltage of VW_L is positive, the voltage of IS_L increases; and if the voltage of VW_L is negative, the voltage of IS_L decreases.

When HO is turned on, the voltage of IS_L turns-off HO before it becomes negative. LO turns-on when the voltage of IS_L is positive. On the other hand, when LO is turned on, the voltage of IS_L turns-off LO before it becomes positive. LO turns-off when the voltage of IS_L is positive. After the voltage of IS_L becomes negative, HO turns-on and it limits the minimum switching frequency.

Fig. 8 is a block diagram of the proposed RDPC. It consists of a level shifter, a phase detector, a delay cell and a counter. The negative voltages of the VW_L signal and IS_L signal are shifted to positive voltages by the level shifter since they need to be detected by the following blocks. The inputs of the high

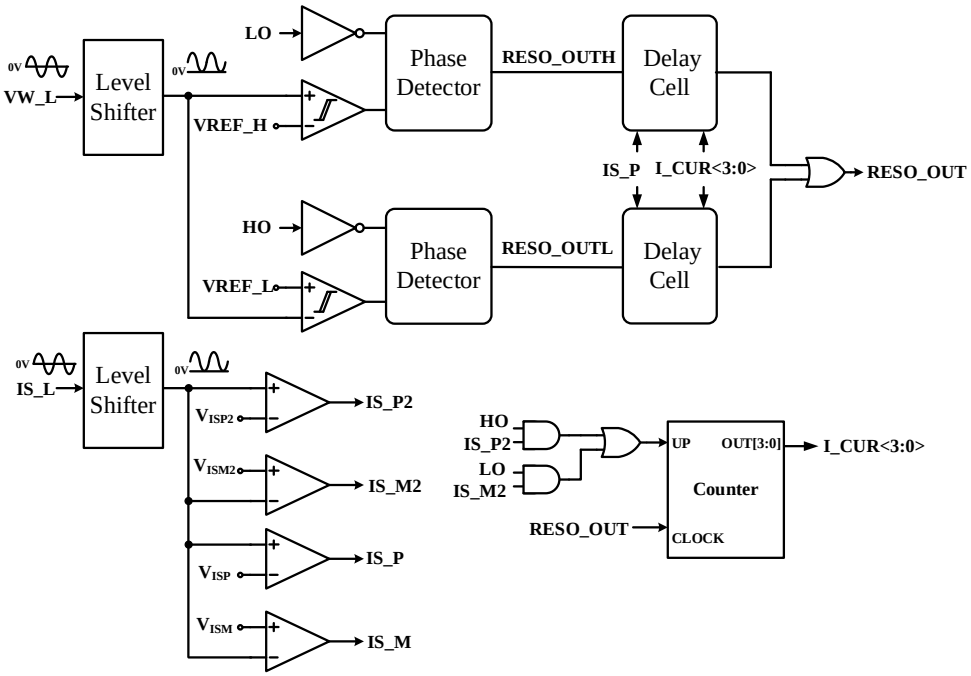

Fig. 8. Block diagram of the proposed RDPC.

side phase detector are the VW_L signal and the HO signal. If HO becomes high and the voltage of VW_L is negative, the RESO_OUTH signal becomes high, and the voltage of IS_L decreases. Similarly, the inputs of the low side phase detector are the voltage of VW_L and the LO signal. If LO becomes high and the voltage of VW_L is positive, the RESO_OUTL signal becomes high, and the voltage of IS_L increases. Thus, the high side phase detector and low side phase detector indicate the increment and decrement of the voltage of IS_L, respectively. The high side delay cell and low side delay cell generate a delay time based on the voltage of IS_L and the outputs of the high side phase detector and low side phase detector. In addition, their delay times are controlled by the outputs (I_CUR<3:0>) of the counter. The outputs of the high side delay cell and low side delay cell are merged by the OR gate to generate the RESO_OUT signal. If RESO_OUT is high, the HO or LO signal becomes low in order to stop the gate switching before it goes to a lower frequency. The counter is used to control the delay time of the high side delay cell and low side delay cell. If HO is high when the RDPC is active and the voltage of IS_L is smaller than V_{ISM2}, I_CUR<3:0> is shifted by one step from the LSB to the MSB and one bit is added to the LSB.

On the other hand, if the voltage of IS_L is larger than V_{ISM2}, I_CUR<3:0> keeps its previous value. In addition, when LO becomes high and the voltage of IS_L is smaller than V_{ISP2}, I_CUR<3:0> is shifted by one step from the LSB to the MSB and one bit is added to the LSB. On the other hand, if the voltage of IS_L is larger than V_{ISP2}, I_CUR<3:0> keeps its previous value. The switching frequency of the LLC converter is limited to the minimum switching frequency, step-by-step,

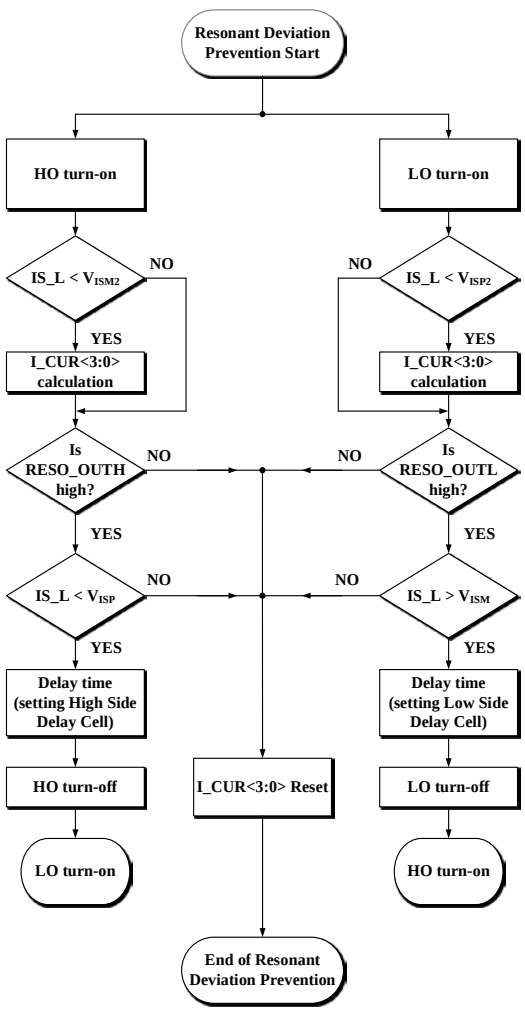

Fig. 9. Flowchart of the proposed RDPC.

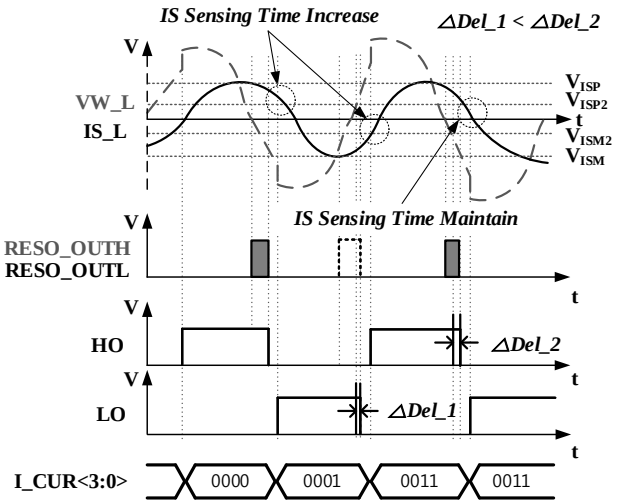

Fig. 10. Timing diagram of the proposed RDPC.

based on the operation explained above. As a result, the LLC converter approaches the minimum switching frequency smoothly.

Fig. 9 is a flowchart of the proposed RDPC. If the RDPC is active and HO becomes high, I_CUR<3:0> is increased or keeps its previous value by comparing the voltages of IS_L and V_{ISM2} with the comparator. If RESO_OUTH is low and the voltage of IS_L is larger than V_{ISP}, I_CUR<3:0> is reset to "0000" and the RDPC operation is terminated. On the other hand, if LO starts to operate, I_CUR<3:0> is increased or keeps its previous value by comparing the voltages of IS_L and V_{ISP2} with the comparator. If RESO_OUTL is low and the voltage of IS_L is smaller than V_{ISM}, I_CUR<3:0> is reset to "0000" and the RDPC operation is terminated.

Fig. 10 is a timing diagram of the proposed RDPC. While the HO signal is high, IS_L decreases after reaching its maximum value. The resonant tank of the LLC converter is located at the boundary between the capacitive and inductive regions. The polarity of VW_L is positive when IS_L increases, and the polarity of VW_L is negative when IS_L decreases.

If the HO signal is high, RESO_OUTH becomes high when VW_L is low. If IS_L is lower than V_{ISP}, the HO signal becomes low after the delay time of the high side delay cell.

When the LO signal is high and IS_L is larger than V_{ISP2}, I_CUR<3:0> is increased from "0000" to "0001". If IS_L is larger than V_{ISM}, the LO signal becomes low after the delay time of the low side delay cell. The delay time of the low side delay cell is determined by an I_CUR<3:0> of "0001". If the HO signal becomes high and IS_L is smaller than V_{ISM2}, I_CUR<3:0> is changed from "0001" to "0011". Thus, the delay time of the high side delay cell is determined by an I_CUR<3:0> of "0011".

B. The Wide Range Gate Clock Generator

The LLC resonant converter consists of a frequency feedback loop. The clock generator from the conventional LLC resonant converter uses a linear switching frequency with respect to the feedback voltage. On the other hand, the on time of the gate pulse in the proposed wide range gate clock generator was designed to have a linear relationship with the feedback voltage.

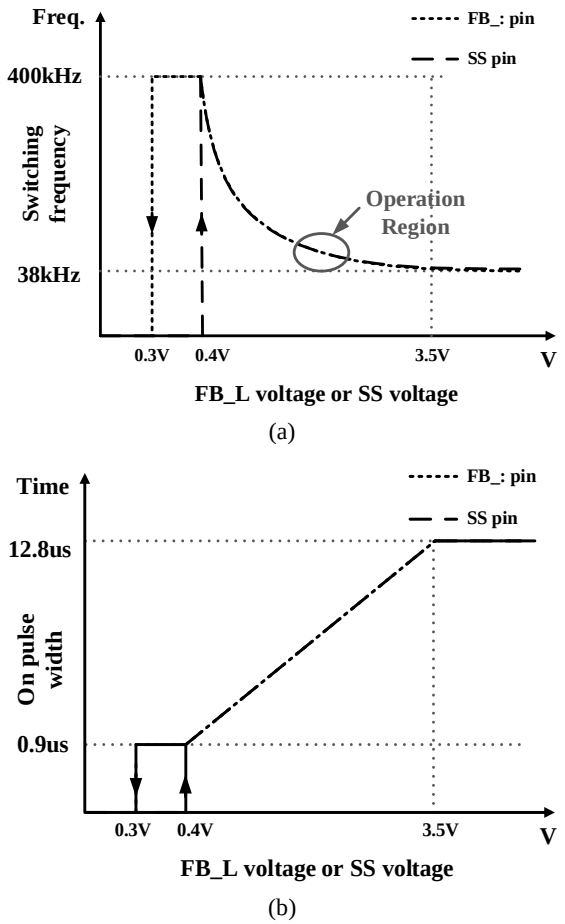

Fig. 11. (a) The switching frequency characteristics. (b) On pulse width characteristics of the proposed wide range gate clock generator.

By using the proposed linear on time scheme, the switching frequency of the LLC resonant converter changes quickly until it reaches the target frequency so that power loss can be minimized at the initial start-up operation. The feedback accuracy is also enhanced by changing the switching frequency slowly after reaching the target operation frequency.

As shown in Fig. 11(a), the switching frequency is determined by the lowest voltage level among the FB_L and SS voltages. The frequency of the gate clock generator is fixed at 400 kHz until the FB_L or SS voltage reaches 0.4 V. The gate clock generator stops operating when the FB_L or SS voltage reaches 0.3 V with a hysteresis of 0.1 V. Fig. 11(b) is the on pulse width graph with respect to the FB_L or SS voltage. The regulation characteristics are improved by controlling the pulse width linearly. This lowers the frequency variation at the operating frequency of the LLC resonant converter.

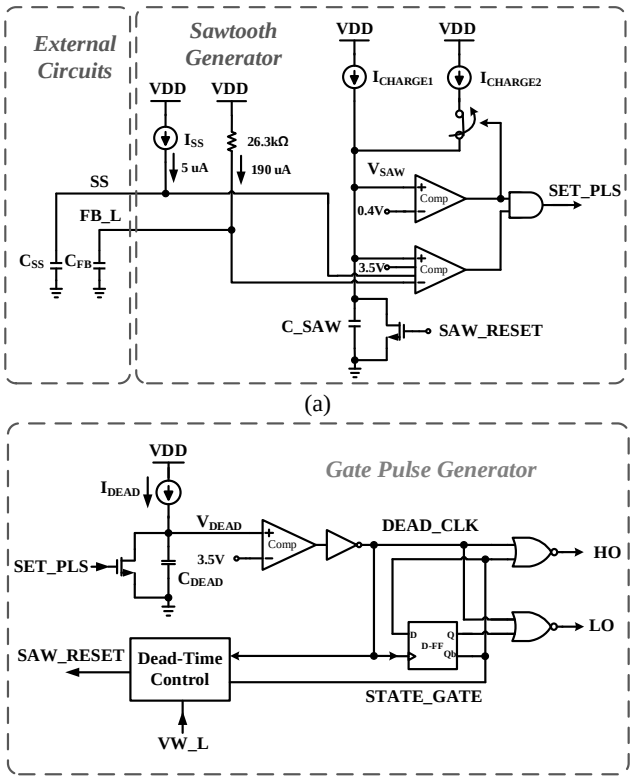

Fig. 12. The block diagram of (a) Sawtooth Generator. (b) Gate Pulse Generator used in the Wide Range Gate Clock Generator.

In addition, the feedback accuracy can be improved by minimizing the frequency variation, which is controlled by the operation of the RDPC.

Fig. 12(a) is a block diagram of the sawtooth generator used in the wide range gate clock generator. The capacitors (C_{SS} and C_{FB}) from the external circuits are charged by the current sources in the sawtooth generator. Furthermore, the switching frequency is determined by the lowest voltage among the FB_L or SS voltages. C_SAW is charged by the current sources $I_{CHARGE1}$ and $I_{CHARGE2}$. If the voltage across C_SAW is over 0.4 V, it is charged by $I_{CHARGE1}$. A dual slope sawtooth generator is implemented so that the on-pulsewidth is controlled linearly with respect to the voltage of SS and FB_L. In this design, the frequency range is from 38 kHz to 400 kHz. Another block in the wide range gate clock generator is the gate pulse generator as shown in Fig. 12(b). The voltage from C_{DEAD} is discharged when the SET_PLS signal becomes high. If the voltage of V_{DEAD} becomes 0 V, DEAD_CLK becomes high. If DEAD_CLK becomes high, HO and LO become low because they are connected to a NOR gate.

SET_PLS becomes low when the SET_RESET signal is active. This is generated by the VW_L and dead-time control block. After that, I_{DEAD} recharges C_{DEAD} until V_{DEAD} goes over 3.5 V. Then DEAD_CLK becomes lower by the comparator.

Fig. 13 is a timing diagram of the wide range gate clock generator. In the T_1 region, C_SAW is charged by two current sources, $I_{CHARGE1}$ and $I_{CHARGE2}$.

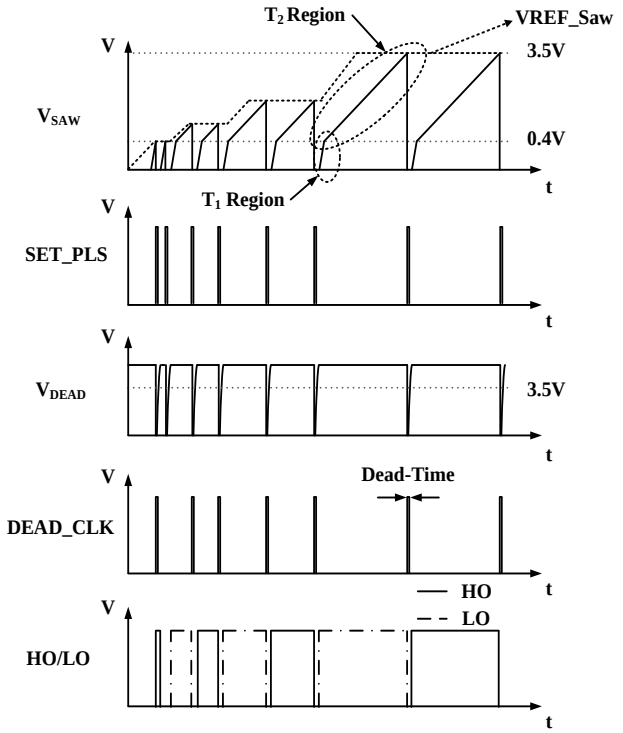

Fig. 13. The timing diagram of the proposed Wide Range Gate Clock Generator.

At this time, the output frequency is determined by Eq. (4).

$$f_{out.\max} = \frac{1}{2T_1} = \frac{I_{CHARGE1} + I_{CHARGE2}}{2 \cdot C\_SAW \times (0.4)} \quad (4)$$

During the T_2 region, C_SAW is charged by only one current source, $I_{CHARGE1}$. The output frequency of the wide range gate clock generator is determined by Eq. (5).

$$f_{out} = f_{out.\max} + \frac{I_{CHARGE1}}{2 \cdot C\_SAW \times (VREF\_Saw - 0.4)} \quad (5)$$

When V_{SAW} reaches VREF_Saw, the SET_PLS signal goes high. Then, the V_{DEAD} node is discharged and the DEAD_CLK signal goes high. The HO and LO signals become low to turn off the corresponding power MOSFETs when DEAD_CLK is high.

C. Automatic Dead Time Generator

In the design of the LLC resonant converter, the dead time needs to be carefully determined because the minimum duty cycle of the gate driving output is related to the conduction time of the body diode of the power MOSFET. The minimum dead time is related to the output capacitance of the power MOSFET. Since the LLC resonant converter is inherently a variable frequency topology, dead-time control is occasionally not essential and may influence the available frequency range.

The automatic dead time generator generates the dead time actively with respect to the switching frequency information and the values of Lr and Cr of the resonant tank.

Even if the switching frequency is changed, an optimized dead-time is generated for the proper operation of the LLC resonant converter.

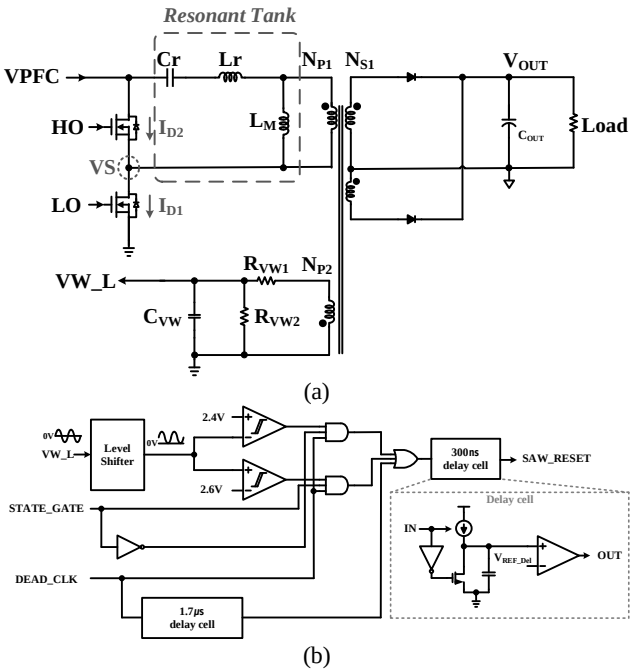

Fig. 14. (a) The external LLC resonant circuits. (b) Detailed block diagram of the proposed Automatic Dead Time Generator.

As the switching frequency reaches the maximum available frequency, hard switching can occur. In order to prevent the LLC resonant converter from hard switching, the automatic dead time generator automatically controls the dead-time from 300 ns to 2 μs.

Fig. 14(a) shows the external LLC resonant circuits. The VW_L voltage follows the variation of the VS voltage. The VW_L voltage can be described by Eq. (6) when the HO signal is high.

$$\frac{N_{P1}}{N_{P2}} \times VW\_L = VS + Vcr + V_{Lr} - VPFC \tag{6}$$

Eq. (7) and (8) can be derived from Eq. (6) by differentiating both sides.

$$\frac{dVW\_L}{dt} = \frac{N_{S1}}{N_{P1}}\left(\frac{dVS}{dt} + \frac{dV_{CR}}{dt}\right) \tag{7}$$

$$\frac{dVW\_L}{dt} = \frac{N_{S1}}{N_{P1}}\left(\frac{I_{CR}}{C_{VS}} + \frac{I_{CR}}{Cr}\right) \tag{8}$$

Assuming that Cr >> C_{VS}, Eq. (8) can be rewritten as Eq. (9).

$$\frac{dVW\_L}{dt} \approx \frac{N_{S1}}{N_{P1}} \times \frac{dVS}{dt} \tag{9}$$

Fig. 14(b) shows a detailed block diagram of the automatic dead time generator. The output signals of wide range gate clock generator, STAGE_GATE, DEAD_CLK, and VW_L are applied to the inputs of the automatic dead time generator. When STATE_GATE is low, HO is turned on. On the other hand, LO is turned on when STATE_GATE is high. When STATE_GATE is low, the VW_L voltage changes from positive to negative, and STATE_GATE becomes high when

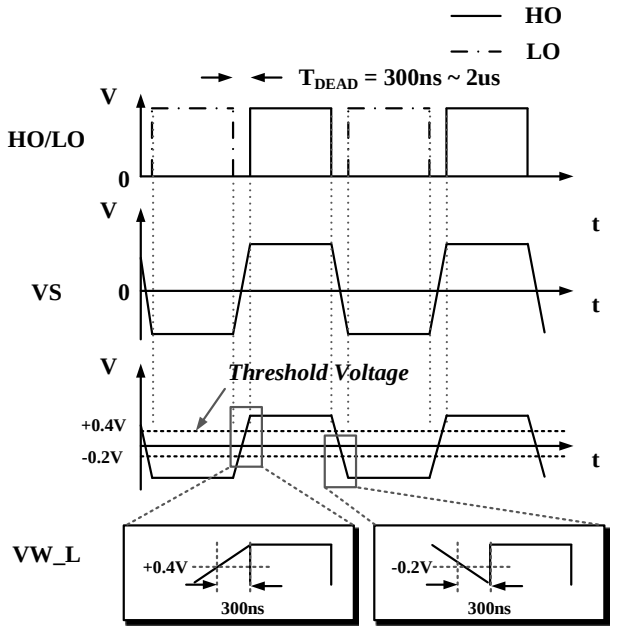

Fig. 15. The timing diagram of the automatic dead time generator.

the VW_L voltage changes from negative to positive. The automatic dead time generator block is triggered by the DEAD_CLK signal. When VW_L is not detected during 1.7 μs, the output of the OR gate becomes high. After the delay time of 300 ns, the SAW_RESET signal becomes high and the gate of the next block is turned on. Delay times of 1.7 μs and 300 ns are generated by the delay cell consisting of a comparator, a current source, and a capacitor.

Fig. 15 is a timing diagram of the automatic dead time generator. During the dead time, the VS signal crosses 0 V.

As shown in Eq. (9), the change rate of the VS signal can be represented by the change rate of VW_L. When the LO signal becomes low and VW_L is larger than 0.4 V, the HO signal becomes low after 300 ns. When the HO signal becomes low and VW_L is smaller than -0.2 V, the LO signal becomes high after 300 ns.

D. The System Initialization Block

The proposed LLC resonant converter controller IC can support the operation of standby mode regardless of the existence of an external PFC IC before the system starts.

Fig. 16 is a block diagram of the system initialization. When the VCC voltage is over 12 V, the LLC resonant controller IC monitors the MODE voltage that is integrated through C_{MODE} and R_{MODE} for 40 ms. It also selects the operation mode between the standby mode (SM) and the quiet mode (QM).

AC_H and AC_L are selected by comparing the external STR voltage level with the reference using the comparator. The low power standby or quiet modes are selected depending on the R_{MODE} resistor value, as summarized in Table I.

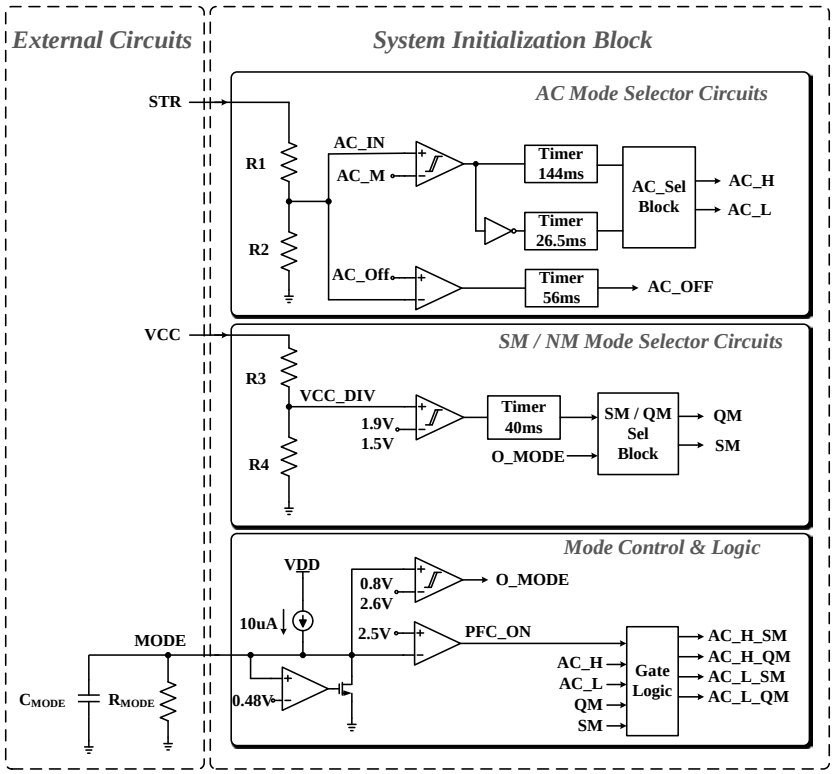

Fig. 16. The block diagram of System Initialization.

TABLE I
MODE SELECTION DEPENDING ON R_{MODE} RESISTOR VALUE

Mode	R_{MODE}
Anti-Noise with PFC	56 kΩ
Low-Power Standby with PFC	100 kΩ
Anti-Noise without PFC	200 kΩ
Low-Power Standby without PFC	300 kΩ

The quiet mode is the preferred mode since it reduces the noise of the transformer by slowing down the variations of the switching frequency. The purpose of the low-power standby mode is to achieve a high gain for the LLC converter by rapidly changing the switching frequency.

Fig. 17 is a timing diagram of the system initialization and mode selection unit of the proposed LLC resonant converter. When an AC input voltage is applied, the startup circuit operates and the VCC voltage increases. When the VCC voltage reaches 11.5 V, the operation of the startup circuit is stopped and the external voltage is sensed to select the operation mode for 40ms. If the VCC voltage is lower than 11 V, the startup circuit is enabled.

E. Standby Mode

When there is no load at the secondary side, the minimum necessary blocks operate in a burst way and the proposed LLC resonant converter controller IC enters the standby mode where it consumes minimum power until the load current increases. In the standby mode, the LLC

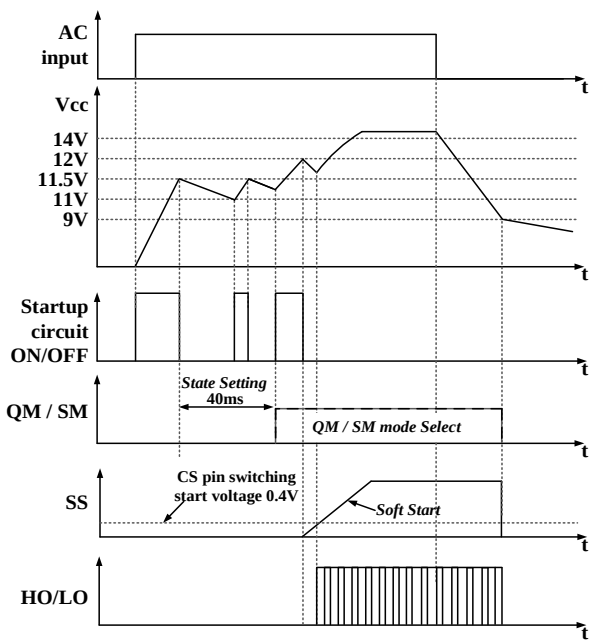

Fig. 17. The timing diagram of System Initialization block.

resonant converter operates to maintain the internal VDD voltage. By using the SS voltage, the soft start function is enabled and the LLC resonant converter is stabilized.

Fig. 18 is a system block diagram in the stand-by mode. The LLC controller IC receives the STB signal using an opto-coupler. The LLC controller IC turns off the PFC and normal circuit operation when the STB signal is high. The LLC converter senses the VCC voltage and operates in the

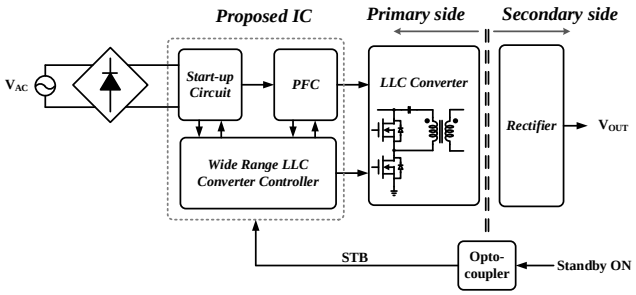

Fig. 18. The system block diagram in Stand-By mode.

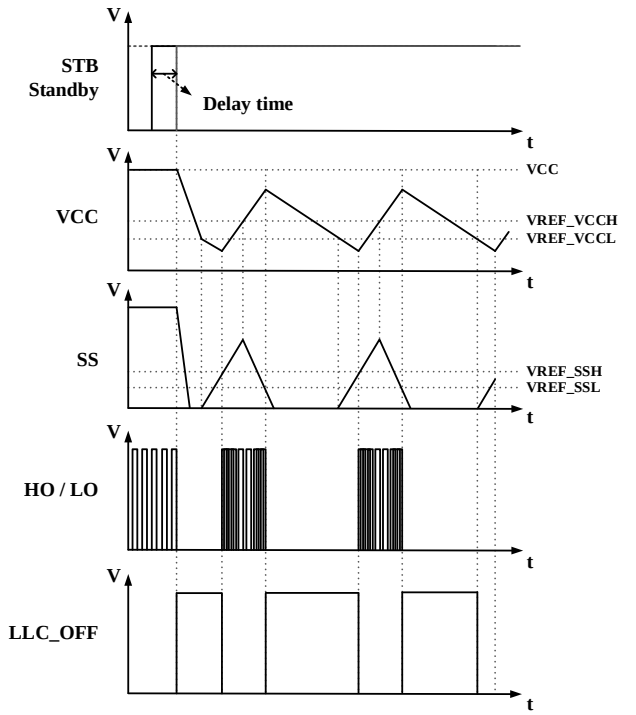

Fig. 19. The timing diagram in Standby Mode.

burst mode.

Fig. 19 is a timing diagram in stand-by mode. When the STB signal becomes high, the HO and LO signals become low, and discharge the SS and VCC voltages.

The VCC voltage is discharged until it reaches VREF_VCCL. Then, the SS voltage starts to charge until it reaches VREF_SSL. Then, the HO and LO signals start switching and the VCC voltage is recharged.

When the VCC voltage reaches VREF_VCCH, the SS voltage starts to be discharged. If the SS voltage is lower than VREF_SSL, then HO and LO become low and turn off the power MOSFETs. The switching frequency is determined by the SS voltage level and the soft burst mode is implemented by alternating between high and low frequencies.

F. Protection Circuit

As shown in Fig. 20, the LLC resonant controller IC includes a protection circuit for over voltage, brown out, and over load conditions. The brown out block turns off the LLC controller IC if the external AC supply voltage is lower than

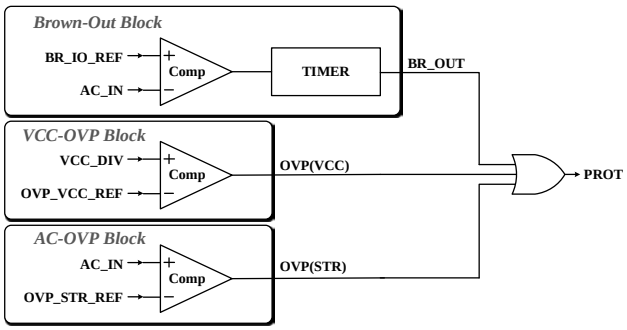

Fig. 20. The protection circuit.

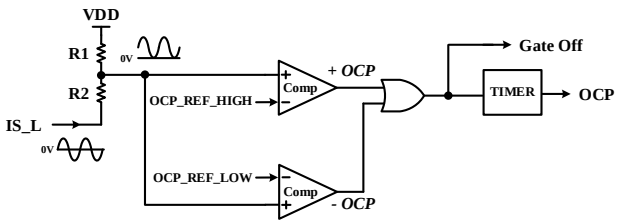

Fig. 21. The Over Current Protection circuit.

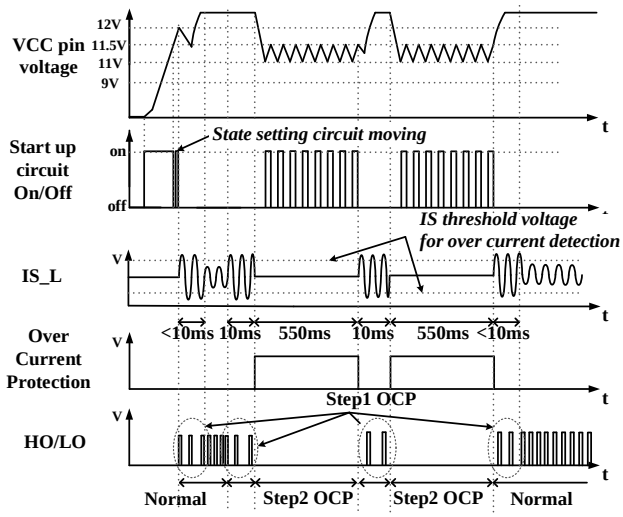

Fig. 22. The timing diagram of the OCP circuit.

the reference voltage (BR_LO_REF).

The Over Voltage Protection (OVP) turns off the LLC controller IC when the VCC and external AC supply voltages are higher than the reference voltages OVP_VCC_REF and OVP_STR_REF.

Fig. 21 shows the Over Current Protection (OCP) circuit. The OCP is activated when the IS_L voltage is higher than the OCP_REF_HIGH signal or lower than the OCP_REF_LOW signal. There are two steps in the OCP. The first step is to turn off the gate that has sensed the +OCP or –OCP. After that, the next side gate is turned on to operate the LLC converter. If the first step lasts more than 10 ms, the OCP signal turns off the LLC controller IC for 55 ms. The LLC controller IC enables soft-start operation because of the auto recovery of the OCP circuit.

Fig. 22 shows a timing diagram of the OCP operation. The resonant current signal of the external LLC converter is

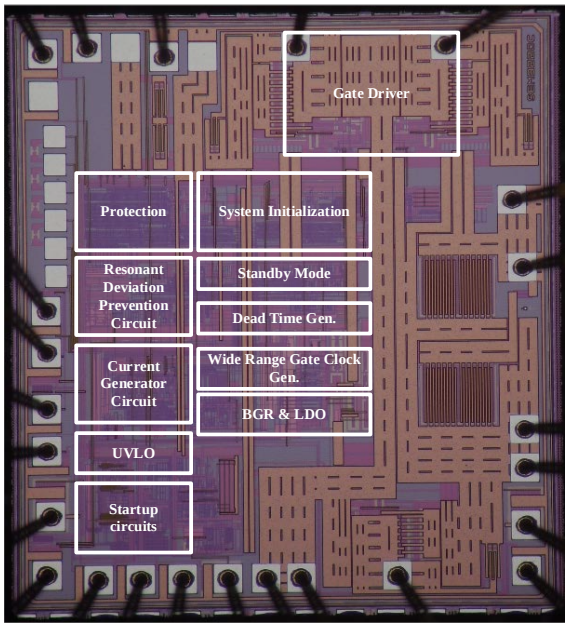

Fig. 23. The chip microphotograph.

detected by the IS_L signal. It is used inside the IC through the resistor division and level shifter. When IS_L is over the threshold of over voltage protection, HO and LO are turned off and another side gate is turned on. When the gates of the power MOSFETs are turned off, the current of the LLC converter does not increase any more. On the other hand, when the next side gate is turned on, the polarity of the current is changed.

This is the first step of the OCP operation. If the first step lasts more than 10 ms, the next OCP step operates and the HO and LO signals are low for 550 ms. The VCC voltage decreases if the HO and LO signals are low and the VCC voltage is lower than 11 V. Then, the startup circuit is enabled. When the VCC voltage is lower than 11.5V, the startup circuit is disabled to keep the IC voltage stable. After 550 ms, the auto recovery function of the OCP circuit is started. When the IS_L voltage is over the OCP detection level, the next step is started after the first step.

IV. Simulation and Measurement Results

The chip was fabricated using a BCD process with 0.35 μm technology using one poly layer, four metal layers, and the option of a high-voltage MOSFET. A microphotograph of the chip is shown in Fig. 23. The die area of the controller IC is 2 x 2 mm^2.

The blocks are placed with consideration of the power consumption and performance of the IC. The gate driver and start up circuits are located around the sides of the chip since they consumes a large amount of current. The length of the current path between the PAD and the circuits is minimized to reduce parasitic resistance and power loss. In the standby mode, current is consumed only when the gate switching is operated.

TABLE II
The Experiment Conditions

Parameters	Value
PFC Input Voltage (VPFC)	100 ~ 385 V
Output Current (I_{OUT})	0A or 6.75 A or 10A
Output Voltage (V_{OUT})	12.8 V
The transformer winding turns ratio	N_{P1} N_{P2}: N_{S1} = 34 : 3 : 2
Resonant Tank	L_M = 400 μH, Lr = 40 μH, Cr = 33 nF
Output Capacitor (C_{OUT})	100 μF / 50V
IS_L and VW_L detect circuits	Crd : 220 pF R_{VW1} : 15 kΩ R_{VW2} : 1.5 kΩ
FB_L Feedback parameter	C_{F1} : 1.1 nF C_{F2} : 10 nF R_F : 2.2 kΩ

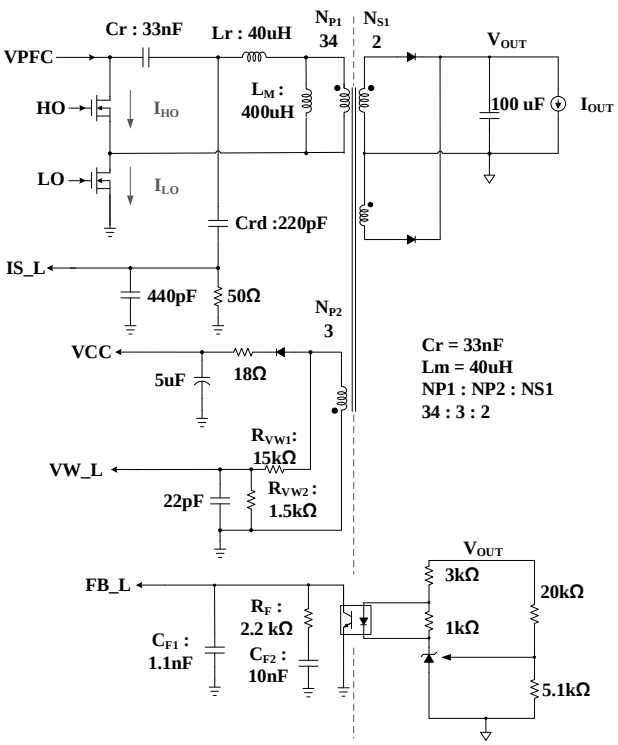

Fig. 24. The experimental environment.

The gate driver, wide range gate clock generator, dead time generator, current generator circuits, and RDPC are disabled to minimize the current consumption when the gate of the power MOSFET is turned off.

The experimental conditions for the proposed wide range LLC controller circuit are summarized in Table II.

N_P and N_S are the transformer winding turns ratios from Fig. 24. L_M is the transformer magnetizing inductance, and L_r is the series leakage inductance with the series capacitance, C_r. Crd is used for dividing the resonant current capacitor. R_{VW1} and R_{VW2} are used for dividing the resonant voltage.

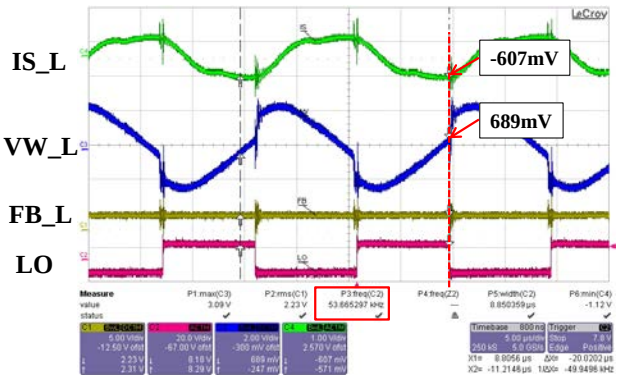

Fig. 25. The measured waveform of the RDPC.

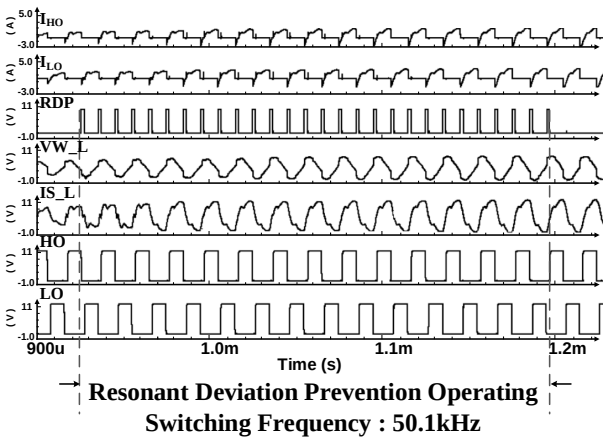

Fig. 26. The simulated waveforms of the RDPC.

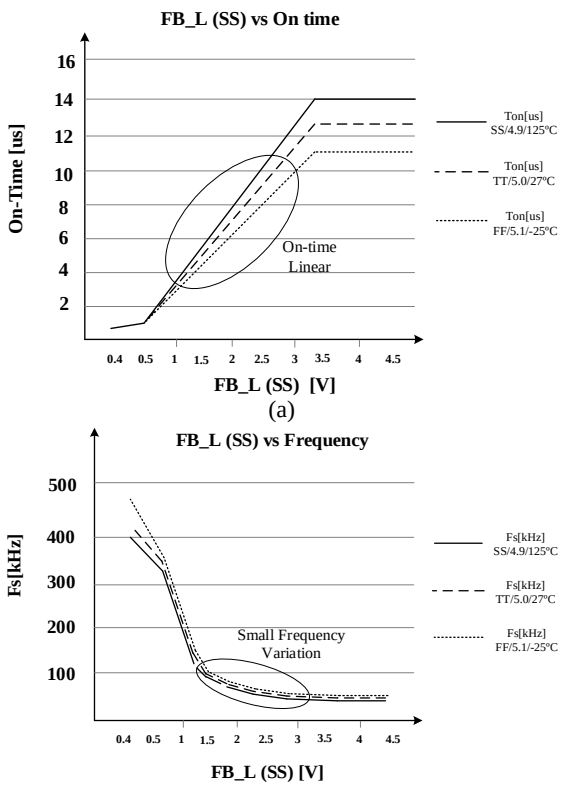

Fig. 27. The relationship between (a) On-Time (b) Switching Frequency and FB_L (SS).

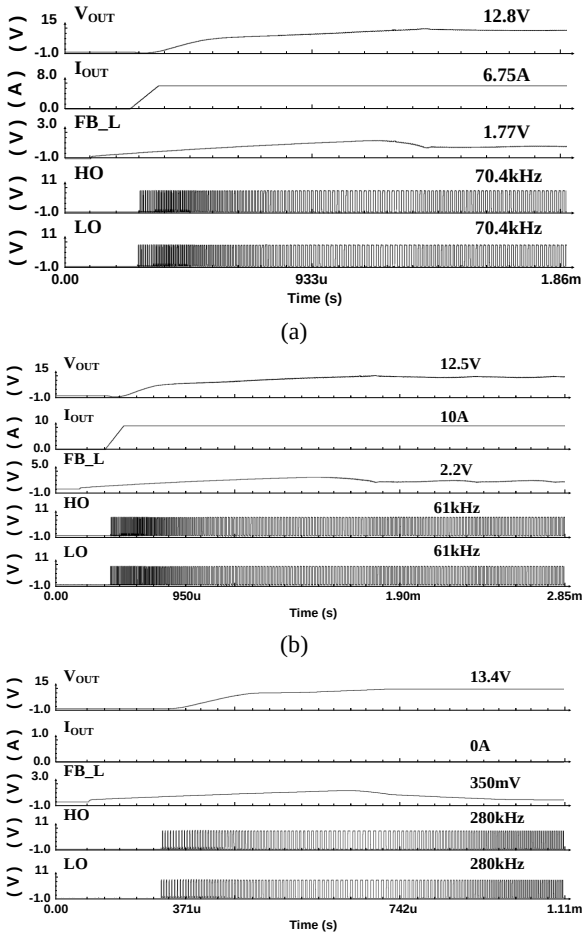

Fig. 28. The simulation regulation characteristics (a) I_{OUT} is 6.75 A (b) I_{OUT} is 10 A, (c) I_{OUT} is 0 A.

Fig. 25 shows a measured waveform of the RDPC when the VPFC voltage is 127 V and the output current is 5 A. The low side gate driver (LO) is turned off when the VW_L and IS_L voltages reach 689 mV and -607 mV, respectively. Under these operating conditions, the switching frequency is limited to 53 kHz.

Fig. 26 shows simulated waveforms of the RDPC. As the switching frequency gets lower, the RDPC senses the VW_L and IS_L waveforms to limit the switching frequency to 50.3 kHz.

Fig. 27(a) shows the linear relationship between the on-time and the FB_L or SS voltage. Under the typical conditions (VDD is 5.0 V, the process is TT, and the temperature is 27 ℃) the on-time can be controlled linearly from 936 ns to 12.86 μs. As shown in Fig. 27(b), the switching frequency is from 38 kHz to 400 kHz. Due to the linear on-time, the controllable frequency range is 100 kHz, which is relatively small when compared with conventional approaches.

Figs. 28(a)-(c) are the simulated regulation characteristics with respect to the load current (I_{OUT}) variations. Fig. 28(a)

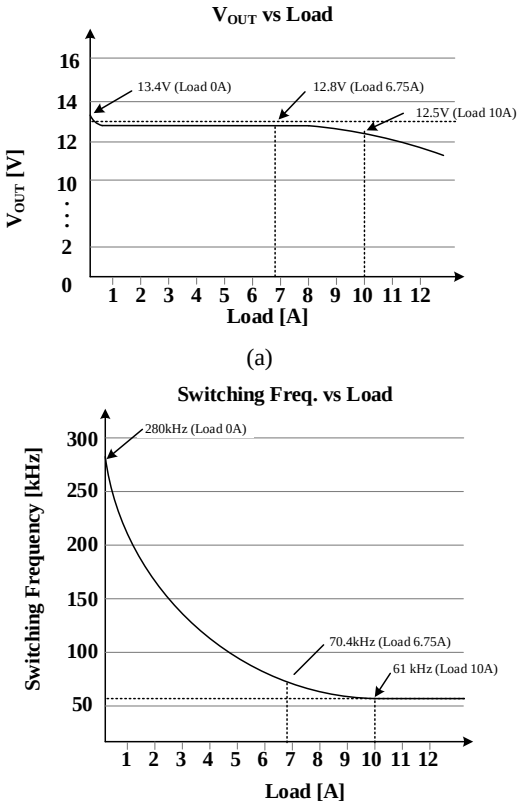

Fig. 29. The relationship between (a) output voltage (b) switching frequency and load current of proposed LLC resonant controller IC.

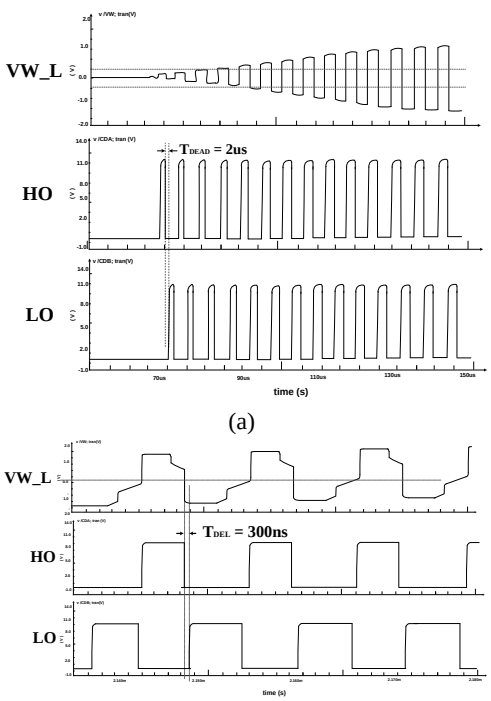

Fig. 30. The output waveforms of the automatic dead time generator in case of (a) dead time = 2 μs (b) dead time = 300 ns.

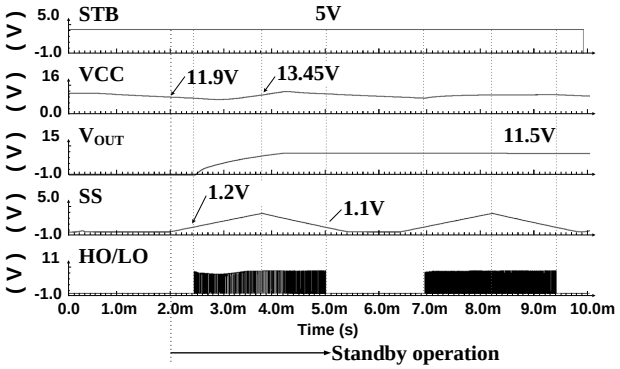

Fig. 31. The simulated waveforms in Standby mode.

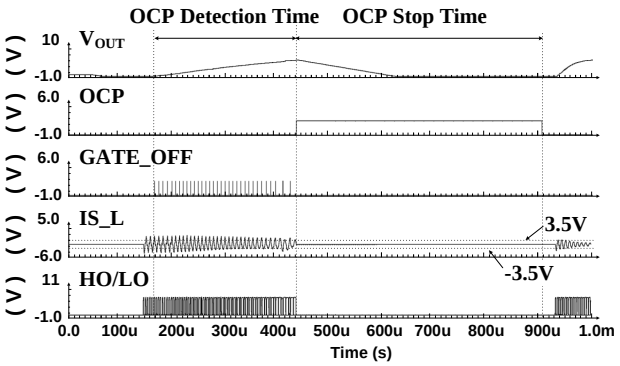

Fig. 32. The simulated waveforms for over current protection.

shows that the output voltage (V_{OUT}) is regulated to 12.8 V at a typical load current of 6.75 A. The FB_L voltage is 1.77 V and the switching frequency is 70.4 kHz. Fig. 28(b) shows that the output voltage (V_{OUT}) is regulated to 12.5 V with a ripple voltage of 0.5 V and at a full load current of 10 A. To regulate the output voltage, the switching frequency is reduced to 61 kHz so that the gain of the LLC converter increases. Fig. 28(c) shows that the regulated output voltage is 13.4 V at no load current. With no load, the switching frequency rises to 280 kHz to minimize the gain of the LLC converter. The FB_L voltage drops to 350 mV adjusting the on time and dead times of HO/LO to 930 ns and 900 ns, respectively.

Fig. 29(a) shows that the output voltage (V_{OUT}) is decreased as the load current is increased. With no load, the V_{OUT} voltage is regulated to 13.4 V. With load currents of 6.75 A and 10 A, the V_{OUT} voltage is regulated to 12.8 V and 12.5 V, respectively. Fig. 29(b) shows that the switching frequency is decreased as the load current is increased.

With no load, V, the switching frequency is 280 kHz. With load currents of 6.75 A and 10 A, the switching frequency is 70.1 kHz and 61 kHz, respectively.

Figs. 30(a)-(b) show the output waveforms of the automatic dead time generator. In Fig. 30(a), when the switching frequency is at its maximum, the duration of the dead time is 2 μs. From Fig. 30(b), at the minimum switching frequency, the duration of the dead time is 300 ns.

Fig. 31 shows the simulated waveforms in the stand-by

TABLE III
THE PERFORMANCE COMPARISON TO PRIOR WORKS

	[19]	[20]	[21]	**This work**
Operating Voltage	15 V	12 V	15 V	**15 V**
Current Consumption	25 mA	13.3 mA	8 mA	**4 mA**
Resonance Deviation Prevention Function	No	No	No	**Integrated**
Dead-time Adjustment Function	Integrated	No	No	**Integrated**
Frequency Control Range of Clock Generator	60 kHz ~ 235 kHz	50 kHz ~ 525 kHz	50 kHz ~ 215 kHz	**38 kHz ~ 400 kHz**
Dead-time	230 ns ~ 700 ns	290 ns	300 ns	**300 ns ~ 2 μs**

mode. The HO and LO signals become low to turn off the power MOSFETs when the STB signal reaches 5 V. The SS voltage starts charging when the VCC voltage drops to 12 V. When the SS voltage is over 1.2 V, the HO and LO signals start switching and the switching frequency decreases. When the VCC voltage reaches 13.5 V, the SS voltage is discharged and the switching frequency increases. When the SS voltage is below 1.1 V, the HO and LO signals become low to turn off the power MOSFETs.

Fig. 32 shows the simulated waveform of the Over Current Protection (OCP). When the IS_L voltage reaches 3.5 V, the GATE_OFF signal is generated and the HO/LO signals are turned off. After 10 ms, the OCL becomes high and the HO/LO signals are turned off. After 550 ms, the HO/LO signals are recovered automatically and the soft-start operation begins.

Table III shows a performance comparison between this and prior works. The parameters are written in the order of the operating voltage, the current consumption, the use of the resonance deviation prevention function, the use of the dead-time adjustment function, the frequency control range of the clock generator, the dead-time range and the use of the standby mode.

The current consumption of the proposed IC is lower than that of references, [19], [20], and [21]. The speed of the comparator does not need to be fast. Therefore, the current consumption of the comparator is minimized. In addition, the bias currents of the current mirror and operational amplifier are optimized.

V. CONCLUSIONS

This paper presents a wide range LLC resonant controller IC with a phase-domain resonance deviation prevention circuit for LED backlight units. The chip is fabricated using 0.35 μm BCD technology, and the die size is 2 x 2 mm^2. The frequency of the clock generator ranges from 38 kHz to 400 kHz, and the dead time ranges from 300 ns to 2 μs. The current consumption of the LLC resonant controller IC is 4 mA for a 100 kHz operation frequency using a supply voltage of 15 V.

ACKNOWLEDGMENT

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