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An Input-Powered High-Efficiency Interface Circuit with Zero Standby Power in Energy Harvesting Systems

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Abstract

This study presents an input-powered high-efficiency interface circuit for energy harvesting systems, and introduces a zero standby power design to reduce power consumption significantly while removing the external power supply. This interface circuit is composed of two stages. The first stage voltage doubler uses a positive feedback control loop to improve considerably the conversion speed and efficiency, and boost the output voltage. The second stage active diode adopts a common-grid operational amplifier (op-amp) to remove the influence of offset voltage in the traditional comparator, which eliminates leakage current and broadens bandwidth with low power consumption. The system supplies itself with the harvested energy, which enables it to enter the zero standby mode near the zero crossing points of the input current. Thereafter, high system efficiency and stability are achieved, which saves power consumption. The validity and feasibility of this design is verified by the simulation results based on the 65 nm CMOS process. The minimum input voltage is down to 0.3 V, the maximum voltage efficiency is 99.6% with a DC output current of 75.6 μA, the maximum power efficiency is 98.2% with a DC output current of 40.4 μA, and the maximum output power is 60.48 μW. The power loss of the entire interface circuit is only 18.65 μW, among which, the op-amp consumes only 2.65 μW.

Key words: Energy harvesting, High-efficiency, Input-powered, Zero standby power

I. INTRODUCTION

As a promising alternative power source, energy harvesting has considerably attracted more attention in recent years. It provides the replacement or recharge of batteries for a long-term maintenance-free system, and significantly extends the battery lifetime. A high-efficiency low-power interface circuit is necessary to convert the energy collected by the antenna/transducer into DC electrical energy because most energy scavenged from ambient source exists as diminutive AC signals [1]-[8], such as radio frequency (RF) and piezoelectric (PE). This interface circuit is required to maximize the energy transfer, minimize the power loss, and directly supplies the electronic equipments.

As an important method of energy saving and environmental protection, the energy harvesting technology has been studied in many fields of application. Numerous semiconductor companies, such as Linear Technology, ST Microelectronics, and Texas Instruments, have introduced related products, which are mostly applied to solar/PE energy harvesting. Currently, one of the major problems faced is how to improve the voltage and power conversion efficiency at significantly small input voltage while minimizing power consumption and die size. For this purpose, numerous studies on interface circuits for energy harvesting have been conducted in the industry and academe. The results of recent studies have led to remarkable advancements in conversion efficiency, scaling, and low power. Many novel design methods have also been presented to improve the performance of interface circuits. For example, to reduce the conduction voltage drop of switch transistors, the bridge rectifier circuit uses the double operational amplifier (op-amp) control instead of the self-biased design, and then obtains a high conversion efficiency [2]. Considering the diversity of energy sources, an input-powered charge pump is adopted,

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which could simultaneously harvest two different types of energy [3]. To enhance the output voltage further, a voltage doubler is used to replace the bridge rectifier, which obtains a higher voltage efficiency [4]. The positive feedback loop is introduced in the high-speed non-linear comparator to control the active diode and realize a quick and low power interface circuit [5]. For low-voltage low-power applications, the bulk-driven technology is adopted, which effectively reduces the system working voltage and power consumption [6], [7]. Most interface circuits could only provide low output voltage and power; thus, the boosted DC/DC converter is utilized with an integrated single-inductor structure that immensely enhances the output voltage and power [1], [8]. These design methods could significantly improve the system performance for different applications; however, a few problems still need to be considered. Based on this condition, this study conducts further research to explore a new structure and pursue high performance.

The current study presents an input-powered high-efficiency rectifier with zero standby power, which could convert the limited AC signals collected from outside into the stable DC voltage with small power consumption. The input-powered design removes the external power supply, simplifies the circuit structure, and achieves zero standby power to reduce the power consumption considerably. The proposed voltage doubler controlled by a novel feedback loop improves both the voltage and power conversion efficiency, as well as the dynamic response speed. The common-grid op-amp uses only four transistors to switch the active diode and eliminate the offset voltage that causes mismatch and switching delay, which significantly improves the conversion efficiency and energy utilization with a small die size. The entire interface circuit was designed in the 65 nm CMOS process. Both theoretical analysis and simulation results verified the validity and feasibility of the proposed rectifier.

The rest of this paper is organized as follows. Section 2 details the proposed interface circuit. Section 3 presents the simulation results and analysis. Section 4 presents the conclusion of this study.

II. Proposed Interface Circuit

Fig. 1 shows that the proposed rectifier comprises two sub-circuits, namely, the full wave converter and active diode. The first stage full wave converter converts AC to DC and provides the positive half-wave output voltage, supplying the entire circuit and serving as the input-powered. This stage also uses a voltage doubler based on the positive feedback control loop to boost the conversion efficiency and suppress noise. The second stage active diode controls the charging and discharging of storage capacitance and provides a stable output voltage for loads. This stage also employs an active diode controlled by an offset voltage adjustable op-amp to

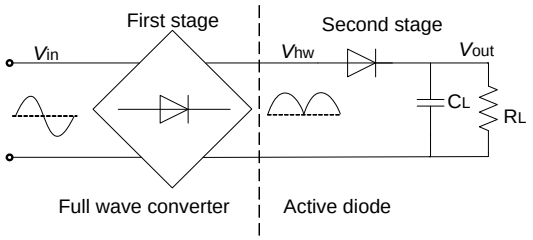


Fig. 1. The proposed interface circuit with two sub-circuits.

eliminate the mismatch, which significantly reduces the reverse leakage of the current and power consumption. The AC input signals are often diminutive and easily affected by the ambient environment; thus, the major design challenge is developing a method to improve the utilization of the harvested energy to maximize the output voltage and power with the power consumption as small as possible.

A. Full Wave Converter

To improve the output voltage swing, the voltage doubler is selected as the full-wave converter. Fig. 2(a) shows the simplified model. The voltage doubler has more advantages against the diminutive AC input signals than the bridge rectifier does. It extends the rectified voltage range with the optimum energy transfer, and enhances the maximum power available [4]. Consequently, it needs a special control circuit for high conversion efficiency and low power. The control circuit must be able to switch D1 and D2 accurately to avoid overlapping conduction; the non-overlapping time should be limited within the minimum allowable range while accounting for the size and power consumption.

Fig. 2(b) details that this study proposes a novel control circuit with a simple structure and low power. When the input voltage V_{in} exceeds the divider voltage of V_{hw}, MP1 turns on and MP3 turns off. The control signal V_c makes the active diode MPS (D1) open, while MNS (D2) closes. V_{in} charges the capacitance C1 through MPS and provides the output voltage V_{hw}. When V_{in} falls below the divider voltage of V_{hw}, MNS turns on and MPS turns off. In this case, C2 is charged by V_{in} and V_{hw} is supplied by C1. MP1 and MP2 form the positive feedback loop to amplify the signal, which boosts the conversion speed. This positive feedback loop also control MP3 to work alternately in the cut-off and saturation states, which prevents the two diodes from conducting simultaneously when V_c is in the middle voltage level. MP3 also helps strengthen the control signal V_c by a gain of $g_m r_{ds}$, where g_m is the transconductance and r_{ds} is the equivalent output resistance. A strong control signal could weaken the leakage current and body effect, and improve the noise immunity. To decrease the current flowing through the transistor MP3/MN3, the MP3/MN3 size should be small enough, and the MN3 length is larger enough than the width. This situation results in a large on-resistance and low power consumption. The small g_m of MN3 could limit the noise

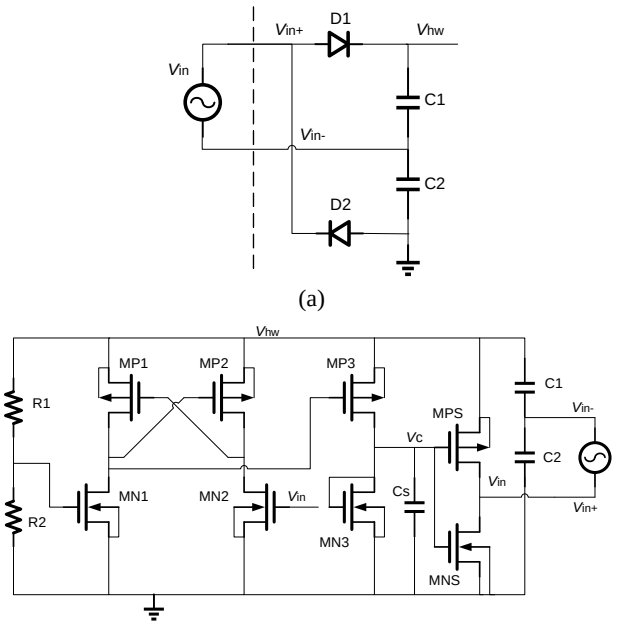


Fig. 2. The first stage voltage doubler. (a) Simplified model. (b) Proposed voltage doubler.

coupled from the power or ground to V_c. To improve the control circuit gain further, the cascade control structure is feasible at the cost of double current and power. The structure selected will depend on the different design requirements and application environment. The capacitance C_s is used to avoid the ringing of the active diodes. Compared with the voltage doubler in Ref. [4], the present study removes the extra control signals and simplifies the circuit structure. Unlike the circuit in Ref. [4], V_{in} is loaded on the transistor gate, and the entire control circuit is similar to a comparator. The power supply provided by the rectified output voltage V_{hw} immensely improves the performance of the voltage doubler, particularly the anti-jamming capability and conversion speed, as well as the good system stability and low power consumption. To obtain a better performance, the digital control could be a promising solution and worthy of further study.

The circuit harvests energy from the input to supply itself, that is, input-powered. Thus, the entire system automatically completes the work mode conversion between operating and standby, depending on the input voltage level. The system consumes power only when the input signal is large enough to start up the entire circuit, which realizes zero standby power. Note that the efficiency of the rectifier is sensitive to the zero crossing points of the input current [2]. Unavoidable reverse leakage current and oscillation often occurs near the zero crossing points of the input current. In the present study, the system will enter the standby mode near the zero crossing points, which significantly improves its stability. At this point, both the voltage doubler and the active diode, as well as their control circuits, are shut down. The system enters into the

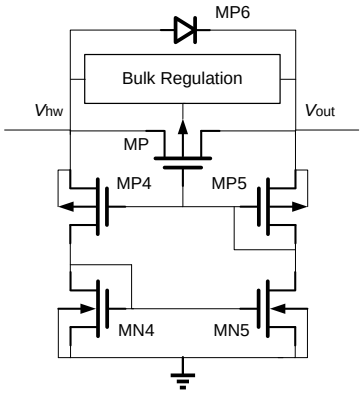


Fig. 3. The op-amp-based active diode with bulk regulation.

standby mode, which eliminates the reverse recovery losses of MPS/MNS, and the EMI problems induced by the zero crossing voltage/current. Hence, the input-powered design efficiently decreases power loss and removes the limits of time intervals between the charging events, which could ensure sufficient energy for energy storage element to activate the interface circuit. Compared with the input-powered techniques in Refs. [2] and [5], the current study provides the higher output voltage and power transfer, with the simple structure.

B. Active Diode

An undesired offset in the traditional comparator-based active diode always exists, which leads to the drift of operating point and the leakage current of the active diode. Thereafter, this condition degrades the system performance. This interface circuit mainly deals with diminutive signals, which requires a higher accuracy circuit cell. This study presents an op-amp-based active diode to eliminate the offset voltage. Fig. 3 shows the entire circuit.

A large PMOS transistor MP is adopted as the active diode for the small conduction loss at high potential. This transistor is controlled by a couple of common-grid differential PMOS (MP4/MP5) with an active load of NMOS current mirror, which acts as an op-amp with an adjustable offset voltage.

When V_{hw} is larger than V_{out}, MP4 extracts current from V_{hw}, the current mirror works, and MP turns on with a small on-resistance. The forward voltage drop $V_{DS,MP}$ depends on the aspect ratio of MP and the common-grid PMOS differential pair. The current $I_{DS,4}$ and $I_{DS,5}$ are considerably small and only exist during the conduction period, which efficiently reduces power loss. The timing of the conduction period is decided by V_{hw}.

$$|V_{GS,4}| = |V_{GS,MP}|, |V_{DS,MP}| = |V_{GS,4}| - |V_{GS,5}| \quad (1)$$

From Eq. (1), the transistor MP is in triode, and MP4 and MP5 are in saturation. Thus,

$$|I_{DS,4} / I_{DS,MP}| = K_4 K_5 / K_{MP}(K_5 - K_4) \quad (2)$$

where $K_i = \mu_p C_{ox}(W/L)_i$. The ratio $|I_{DS,4} / I_{DS,MP}|$ must be small enough to save the power consumption and accelerate

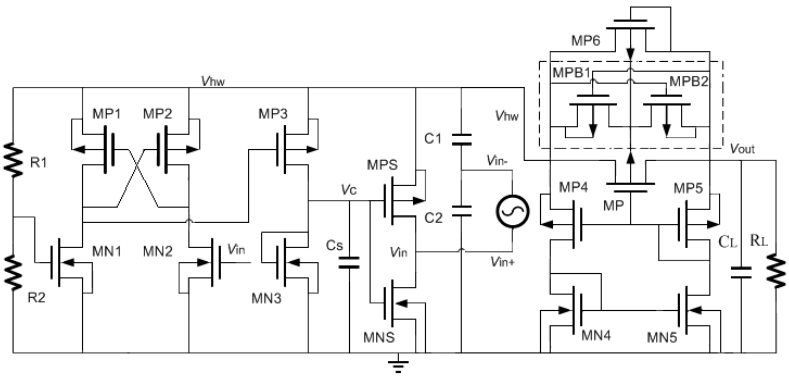


Fig. 4. The whole circuit structure.

the conversion efficiency.

MP is initially in weak conduction. In this short period, $V_{DS,MP}$ is constant depending on the aspect ratio of the transistors, and is independent of $I_{DS,MP}$. With the increase of $I_{DS,MP}$, MP enters in strong inversion. Apart from being affected by the size ratio of MP4 and MP5, $V_{DS,MP}$ is proportional to the square root of $I_{DS,MP}$, as presented in Eq. (3).

$$|V_{DS,MP}| = \frac{\sqrt{K_5} - \sqrt{K_4}}{\sqrt{K_{MP}(K_5 - K_4)}} \sqrt{2|I_{DS,MP}|} \tag{3}$$

At this point, the on-resistance of MP is significantly small and inversely proportional to $I_{DS,MP}$.

When V_{out} is closely equal to V_{hw}, $|V_{DS,MP}|$ is reduced to zero and MP shuts off. MP4 and MP5 still draw a small amount of current, which accelerates the release of the channel current in MP and improves the dynamic response speed. Finally, the increasing gate voltage makes MP4 and MP5 cut off. At this point, op-amp stops working to save power consumption. A transition time occurs during the period from the op-amp shutdown to the turning-off of the active diode, which improves the circuit stability. MP should be large enough to reduce the on-resistance and power loss. However, a considerably large MP will increase the parasitic capacitance and then worsens the offset. As previously mentioned, one of the most important advantages of this circuit is eliminating the mismatch by presetting the offset voltage of op-amp. The different sizes of MP4 and MP5 will lead to the different input voltage deviations; thus, utilizing the mismatched aspect ratio of MP4 and MP5 could preset the offset voltage and eliminate the mismatch in the traditional comparator-based active diode. This situation avoids the leakage current or oscillation, that is, the stability is improved significantly. This circuit consumes consideably little voltage redundancy and power loss. Furthermore, only the voltage gain is supplied at the output terminal of op-amp to drive the active diode, which contributes to reduce the parasitic effects. Compared with the bulk-driven technique in Ref. [7], the present study has a better noise suppression capability in the wider bandwidth, as well as almost the same power supply.

The bulk terminal of the active diode needs to be considered carefully for less parasitic effects because the interface circuit has no external power supply. Ref. [5]-[7] details that a bulk regulation circuit is introduced. A bypass PMOS diode avoids the undesired reverse current and opens the active diode safely in all process corners [7], [8].

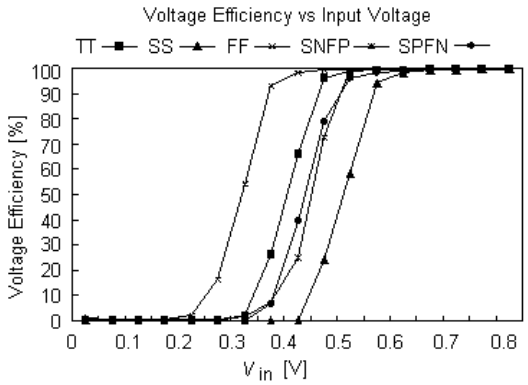
III. Simulation Results and Analysis

The proposed interface circuit is simulated in the 65 nm CMOS process, with the typical threshold voltage of 280 mV/−367 mV for NMOS/PMOS. The supposed input voltage V_{in} is 0.6 V at 50 Hz, with the default load resistance of 10 kΩ and capacitance of 10 μF, which balance the tradeoff between conversion efficiency and power. Fig. 4 shows the entire circuit. The rectified V_{hw} provides the operating power supply for the entire circuit. The novel voltage doubler and op-amp-based active diode play vital roles to improve the voltage and power conversion efficiency with low power consumption.

Fig. 5(a) shows the voltage efficiency as a function of input voltage V_{in} at different process corners. Under typical conditions, the output voltage increases slightly when V_{in} is beyond 0.3 V. Once $V_{in} > 0.32\text{V}$, the output voltage increases rapidly because the active diode starts working. The voltage efficiency η_V is calculated based on

$$\eta_V = \frac{\hat{V}_{out}}{\hat{V}_{in}} \times 100\% \tag{4}$$

Fig. 5(a) shows that when V_{in} is larger than 0.47 V, the voltage efficiency will increase to over 90%, and eventually reaches to the maximum of 99.6% at $V_{in} = 0.8\text{V}$ with a DC output of 75.6 μA. The average voltage efficiency is 88.2% when V_{in} changes from 0.32 V to 0.8 V, which is large enough to meet the application requirements. The voltage doubler with input-powered design effectively improves the output voltage and current, with low power consumption and good stability. The simple common-grid op-amp compensates the offset and eliminates the leakage current and oscillation of the active diode. This result improves the conversion efficiency and achieves the good anti-noise ability and wide



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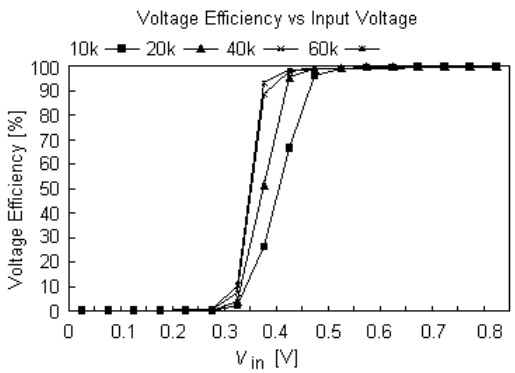
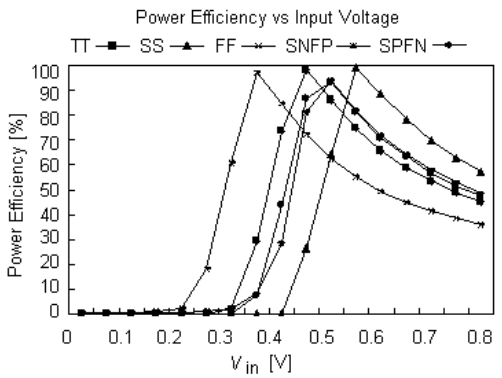


(b)

Fig. 5. Voltage efficiency vs input voltage. (a) At different process corners. (b) At different load resistances.



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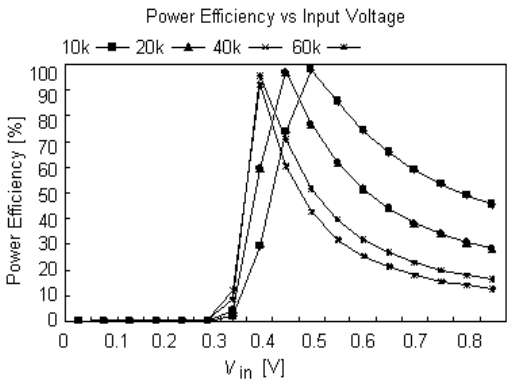

(b)

Fig. 6. Power efficiency vs input voltage. (a) At different process corners. (b) At different load resistances.

frequency working range. The bulk regulation circuit also remains the bulk-source of MP in the weak negative bias state for low threshold voltage and conduction loss. Compared with the traditional bridge rectifier and comparator-based active diode, the proposed circuit could improve efficiency by 10% and output current by 2.5 times.

Fig. 5(b) shows that the performance of the proposed rectifier is further investigated at different loads. With the increase of load resistance, the voltage efficiency slightly changes, except in the input voltage range from 0.32 V to 0.48 V, because the reason is that different loads lead to different charge time of load capacitance. However, the voltage efficiency is almost unaffected by the change of loads once the output voltage reaches the rated value. Therefore, the system has a good load regulation. Note that the minimum working voltage declines slightly with the increase of loads. The reason is that the decreasing load current leads to the smaller conduction voltage drop on the active diode and enhances the discharge cycle.

The power efficiency of rectifier η_p is defined as follows:

$$\eta_P = \frac{\hat{P}_{out}}{\hat{P}_{in}} \times 100\% = \frac{\frac{1}{T}\int_t^{t+T} v_{out} i_{out} dt}{\frac{1}{T}\int_t^{t+T} v_{in} i_{in} dt} \times 100\% \quad (5)$$

Fig. 6(a) presents that apart from being affected by various process corners, the power efficiency clearly changes based on the different input voltages. Such change is primarily caused by the significant change in the output current and power consumption of the entire circuit based on V_{in}. The rectifier initially starts to work from the zero state, and the output current is relatively small; thus, the output power is low. With the increase of V_{in}, the rectifier quickly reaches the optimal working point and obtains the highest power efficiency. Thereafter, the built-in control circuit extracts more energy from V_{hw} for the input-powered, and the power loss in the transistors increases faster than the harvested output power P_{out}. Although P_{out} is also increasing accordingly, the exhibited efficiency is still reduced; thus, the system provides the lower output current than the desired input common mode range of op-amp. The simulated maximum power efficiency is 98.2% at $V_{in} = 0.45\text{V}$, with an increasing DC output current of over 40.4 μA and an output power of over 16.3 μW. Thus, the voltage efficiency is 95.7%. The average power efficiency is 70.1% when V_{in} changes from 0.32 V to 0.8 V, which is significantly lower than the maximum power efficiency. The primary reason is that the power consumption grows faster than P_{out} with the increasing V_{in}. The new design techniques could be used to control the power efficiency attenuation, such as the MPPT circuit. Despite this condition, the proposed circuit improves the power efficiency by 8.7%, the output current by 2.5 times, and the output power by 3.2 times, compared with the traditional rectifier. The entire power consumption is 18.65

TABLE I
PERFORMANCE COMPARISON OF INTERFACE CIRCUITS FOR ENERGY HARVESTING

Parameters	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	The Current Study
Minimum input voltage (V)	0.5	3	0.03	0.44	0.5	0.35	0.15	0.6	0.3
Maximum voltage efficiency (%)	\	\	\	81	97	96	> 80	90	99.6
Average voltage efficiency (%)	\	\	\	\	\	\	\	\	88.2
Maximum power efficiency (%)	65	91.2	57	93	94.2	> 90	< 90	60	98.2
Average power efficiency (%)	\	\	\	\	\	\	\	\	70.1
Maximum output current (μA)	2	30	< 170	\	30	\	\	1300	75.6
Maximum output power (μW)	1000	90	< 170	162	\	19	\	3900	60.48
Power consumption (μW)	884.62	74	60	130	0.65	0.2	\	\	18.65
Manufacturing process (CMOS-μm)	0.35	0.18	0.18	0.35	0.35	0.35	0.18	0.5	0.065
Design complexity	High	High	High	Medium	Medium	Low	Low	High	Low

μW, among which the common-grid op-amp consumes only 2.65 μW.

The measured power efficiency is plotted against the input voltage at different loads in Fig. 6(b). The rectifier with a larger load first achieves the optimal working point; the greater the load, the output current decreases more rapidly, and the system is more sensitive to the current changes. Similar to Fig. 6(a), P_{out} improves with the increase of V_{in}. However, η_p begins to attenuate once the power loss consumed by the rectifier itself is greater than the power harvested at the output terminal. This result means that the current consumption of the rectifier itself becomes more important with a growing V_{in}, particularly at large loads. Despite that η_p decreases following the increasing V_{in}, an extreme value of 45.4% is noted under the typical conditions. Thereafter, the power consumption of the rectifier is gradually saturated, and the power efficiency stabilizes accordingly. Relative to η_V, η_p demands higher load matching. Fig. 6(b) shows that the greater the load is, the faster the power efficiency attenuates, particularly when the output current is close to that through the op-amp. Thus, further analysis of the load matching circuit is necessary to improve the load capacity.

To verify the feasibility and practical application value of the proposed rectifier, Table I provides the performance comparison of the recent, state-of-the-art interface circuits for energy harvesting. Providing a fair comparison is difficult because the harvested energy is limited by numerous factors, such as the ambient environment, antenna matching, process variation, input and output voltage, working frequency, and testing conditions, among others. Table I shows that the proposed rectifier could work at a relatively small input voltage of 0.3 V, and provide a large enough output current of 75.6 μA to drive the loads. This rectifier could also provide a good voltage efficiency and power efficiency with only μW level power consumption. The low power loss primarily benefits from the zero standby power design and the simplified circuit structure. Relatively speaking, the interface circuit in Ref. [1] has a wide input power range and high output power, which is primarily the result of its double boost converter design. Consequently, this circuit consumes more power and die size based on the expensive SOI process. The rectifier in Ref. [2] uses the double op-amp control to obtain a good conversion efficiency and output power. However, its minimum input voltage and power loss are relatively high; thus, this rectifier is not suitable for ultra-low-voltage applications. The regulator in Ref. [3] utilizes an input-powered charge pump to harvest two types of energy with good overall performance. However, the complex structure and low power efficiency limit its applications. Ref. [4] proposes a self-starting interface circuit with voltage doubler. Comparatively, the voltage double in the current study uses a simpler control circuit to complete the voltage doubling function with better voltage/power efficiency and stability. The rectifiers in Refs. [5] and [6] obtain the ultra-low-power of 0.65 μW and 0.2 μW, respectively; however, the comparator-based active diode reduces the system stability and response speed. The interface circuit in Ref. [7] has an ultra-low input voltage of 150 mV, but its conversion efficiency is slight low and the bulk-driven design reduces the noise immunity of the system. The rectifier in Ref. [8] utilizes the boost converter to improve the output current and power, and has a strong load capacity. However, its poor conversion efficiency limits the applications. Lastly, the present study also has a certain advantage despite the design complexity. Table I shows that the proposed rectifier in this study offers both a good conversion efficiency and a competitive output current and power loss. The maximum voltage efficiency of the proposed rectifier is 99.6% and the maximum power efficiency is 98.2%. Although its average power efficiency is only 70.1%, which is slightly low, the interface circuit could also meet the general application demands. The novel voltage doubler and op-amp-based active diode design simplify the circuit structure, improve the efficiency, and save power loss. The output power is slightly low because of the output voltage effects. At the cost of power loss and die size, a boost converter could be introduced to improve the output voltage and power. Furthermore, the load matching and MPPT circuit

could be utilized to avoid the rapid reduction of power efficiency following the increasing V_{in}, which improves the average power efficiency. All these aspects deserve further study. In summary, the proposed rectifier exhibits a few advantages and is suitable to the ultra-low voltage ultra-low power applications.

IV. CONCLUSION

An input-powered high-efficiency interface circuit with zero standby power is proposed in this study. The novel voltage doubler with the positive feedback control and the op-amp-based active diode simplify the circuit structure and improve the conversion efficiency with μW level power consumption. The input-powered design eliminates the extra battery and realizes zero standby power, as well as improves the system stability near the input zero crossing points. The proposed rectifier performs a good overall performance. Its maximum voltage efficiency is 99.6% at $V_{in} = 0.8\text{V}$ with a DC output of 75.6 μA and an output power over 60.48 μW. The average voltage efficiency is 88.2%. Its maximum power efficiency is 98.2% at $V_{in} = 0.45\text{V}$ with a dc output of 40.4 μA and an output power of over 16.3 μW. The average power efficiency is 70.1%. The maximum η_P appears earlier than the maximum η_V with the increasing V_{in}. Thereafter, the rectifier itself extracts more energy from the input terminal, which reduces η_P, with a lower I_{out} than the desired input common mode range of op-amp. The power loss of the entire circuit is only 18.65 μW. Depending on the different applications, a better performance indicator could be achieved by the additional circuits. The proposed interface circuit provides an energy harvesting system for a reliable theoretical basis and key technology solutions. This system could be applied to the related interface circuit development to help shorten the design cycle and reduce design costs. This aspect is worth being further studied to improve its overall performance.

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REFERENCES

[1] E. Dallago, A. L. Barnabei, A. Liberale, and P. Malcovati, "An interface circuit for low-voltage low-current energy harvesting systems," *IEEE Trans. Power Electron.*, Vol. 30, No. 3, pp. 1411-1420, Mar. 2014.

[2] X. Do, H. Nguyen, S. Han, and D. Ha, "A self-powered high-efficiency rectifier with automatic resetting of transducer capacitance in piezoelectric energy harvesting systems," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, Vol.23, No.3, pp.444-453, Mar. 2014.

[3] T. H. Tsai, B. Y. Shiu, and B. H. Song, "A self-sustaining integrated CMOS regulator for solar and HF RFID energy harvesting systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, Vol. 2, No. 3, pp. 434-442, Sep. 2014.

[4] L. Joachim, M. Dominic, and M. Yiannos, "Autonomous and self-starting efficient micro energy harvesting interface with adaptive MPPT, buffer monitoring, and voltage stabilization," in *European Solid-State Circuits Conference (ESSCIRC)*, pp.101-104, 2012.

[5] S. H. Abdalrahman, P. Oliver, and G. Tzeno, "An ultra-low power active AC-DC CMOS converter for sub-1V integrated energy harvesting applications," in *Sensors, 2013 IEEE, Baltimore*, pp. 1-4, 2013.

[6] P. Christian, H. Jonas, M. Dominic, and M. Yiannos, "An ultra-voltage active rectifier for energy harvesting applications," in *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pp.889-892, 2010.

[7] Z. Yang, Y. N. Li, J. G. Wang, Z. M. Zhu, and Y. T. Yang, "A highly efficient interface circuit for ultra-low-voltage energy harvesting," *IEICE Electronics Express*, Vol. 10, No. 24, pp. 1-6, Dec. 2013.

[8] R. Yuan and P. A. David, "An input-powered vibrational energy harvesting interface circuit with zero standby power," *IEEE Trans. Power Electron.*, Vol. 26, No. 12, pp. 3524-3533, Dec. 2011.

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