

Effects of Input Harmonics, DC Offset and Step Changes of the Fundamental Component on Single-Phase EPLL and Elimination

Linsong Luo^{*}, Huixin Tian^{*}, and Fengjiang Wu[†]

^{*}School of Electrical Engineering and Automation, Tianjin Polytechnic University, Tianjin, China

[†]Department of Electrical Engineering, Harbin Institute of Technology, Harbin, China

Abstract

In this paper, the expressions of the estimated information of a single-phase enhanced phase-locked loop (EPLL), when input signal contains harmonics and a DC offset while the fundamental component takes step changes, are derived. The theoretical analysis results indicate that in the estimated information, the n^{th} -order harmonics cause $n+1^{\text{th}}$ -order periodic ripples, and the DC offset causes a periodic ripple at the fundamental frequency. Step changes of the amplitude, phase angle and frequency of the fundamental component cause a transient periodic ripple at twice the frequency. These periodic ripples deteriorate the performance of the EPLL. A hybrid filter based EPLL (HF-EPLL) is proposed to eliminate these periodic ripples. A delay signal cancellation filter is set at the input of the EPLL to cancel the DC offset and even-order harmonics. A sliding Goertzel transform-based filter is introduced into the amplitude estimation loop and frequency estimation loop to eliminate the periodic ripples caused by the residual input odd-order harmonics and step change of the input fundamental component. The parameter design rules of the two filters are discussed in detail. Experimental waveforms of both the conventional EPLL and the proposed HF-EPLL are given and compared with each other to verify the theoretical analysis and advantages of the proposed HF-EPLL.

Key words: Delay signal cancellation, Enhanced phase-locked loop, Input DC offset and harmonics, Sliding Goertzel transform

I. INTRODUCTION

In many of the power electronics devices connected to single-phase utility grids, the synchronization information of the grid is usually estimated by phase-locked loop (PLL) technology to implement the control of the grid current [1]-[5].

Nowadays, many literatures on single-phase PLLs have been presented [6]-[13]. For example, the power PLL (pPLL), the inverse park transform-based PLL (park-PLL), the EPLL, the quadrature PLL (QPLL), the transport delay-based PLL (TDB-PLL), the second-order generalized integrator PLL (SOGI-PLL) [9], the synthesis circuit PLL (SC-PLL) [10], the variable sampling period based PLL[11]-[13], and so on.

Among the aforementioned PLLs, the EPLL has found wide acceptance due to its simple structure and robust performance [14]-[18].

In practice, grid voltage is usually a non-ideal sine wave while with some harmonics. Meanwhile, the DC offset generated by the measurement devices, conversion processes or a fault is another common disturbance in the input signal. Both harmonics and DC offset result in undesired periodic ripples in the phase and amplitude information estimated by the EPLL.

In recent years, several improved EPLLs have been presented. In [16], a window-based in-loop filter is introduced in the frequency loop to eliminate the periodic disturbances caused by input harmonics. However, the effect of the input DC offset cannot be eliminated. In [17], [18], an integrator is introduced and paralleled with the amplitude loop in the EPLL to estimate the input DC offset. The attached integrator can estimate the input DC offset. However, the effect of the input harmonics cannot be eliminated.

Manuscript received Dec. 4, 2014; accepted Apr. 5, 2015

Recommended for publication by Associate Editor Sung-Yeul Park.

[†]Corresponding Author: shimeng@hit.edu.cn

Tel: +86-0451-86412946, Fax: +86-0451-86412946, Harbin Institute of Technology

^{*}School of Electrical Eng. and Automation, Tianjin Polytechnic University, China

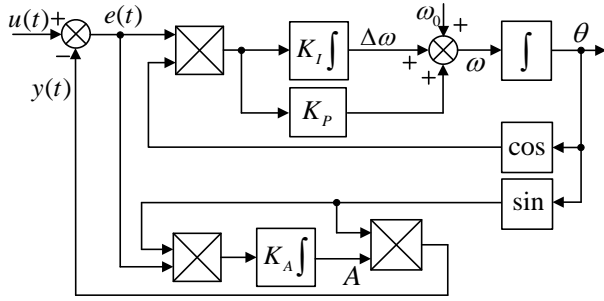


Fig. 1. Structure of conventional EPLL.

In this paper, the effects of the input harmonics, DC offset and step changes of the input fundamental component are theoretically analyzed. According to the obtained results, a hybrid filter based EPLL (HF-EPLL) is proposed. In the HF-EPLL, a delay signal cancellation filter (DSC filter) is set at the input of the EPLL to reject the input DC offset and even-order harmonics. In addition, a sliding Goertzel transform-based filter (SGT-filter) is introduced into the amplitude and frequency estimation loop to eliminate the periodic ripples generated by the residual input harmonics and step changes.

II. EFFECTS OF HARMONICS, DC OFFSET AND STEP CHANGES ON THE EPLL

A. Review of the Principle of the Conventional EPLL

The system configuration of the conventional EPLL is shown in Fig.1. The differential equations of the system are expressed as [14]:

$$\begin{cases} \dot{A} = K_A e(t) \sin \theta, \Delta \dot{\omega} = K_I e(t) \cos \theta \\ \dot{\theta} = \omega_0 + \Delta \omega + K_P e(t) \cos \theta, e(t) = u(t) - y(t) \end{cases} \quad (1)$$

Where A is the estimated amplitude of the fundamental component. $\dot{\omega}$, θ and $y(t)$ denote the derivative with respect to the time of the estimated angular frequency, phase angle and fundamental component of the input signal, K_P and K_I denote the proportional and integral coefficient of the PI controller in the frequency loop, and $\Delta \omega$ denotes the output

of the integrator. K_A is the gain of the integrator in the amplitude loop.

B. Effects of the Input Harmonics and DC Offset

The degraded performance of the conventional EPLL caused by the input harmonics and DC offset is analyzed first. Assume that the input signal, comprising of fundamental components, n -order harmonics and DC offset, is described as:

$$u(t) = U_f \sin(\omega_f t + \varphi_f) + \sum_{n=1}^{\infty} U_{2n+1} \sin[(2n+1)\omega_f t + \varphi_{2n+1}] \quad (2)$$

$$+ \sum_{n=1}^{\infty} U_{2n} \sin(2n\omega_f t + \varphi_{2n}) + U_{dc}$$

where U_f , ω_f , φ_f , U_{2n+1} , ω_{2n+1} , φ_{2n+1} , U_{2n} , ω_{2n} , φ_{2n} denote the amplitude, angular frequency and phase angle of the fundamental component, odd-order harmonic, and even-order harmonic component, respectively. In addition, U_{dc} denotes the voltage of the DC offset.

If it is assumed that the phase angle and frequency are estimated correctly, the output of the conventional EPLL is exactly same as the fundamental component. The output signal and error signal can be derived as:

$$\begin{cases} y(t) = U_f \sin(\omega_f t + \varphi_f) \\ e(t) = u(t) - y(t) \\ = \sum_{n=1}^{\infty} U_{2n+1} \sin[(2n+1)\omega_f t + \varphi_{2n+1}] + U_{dc} \\ = \sum_{n=1}^{\infty} U_{2n} \sin(2n\omega_f t + \varphi_{2n}) \\ \theta = \omega_f t + \varphi_f \end{cases} \quad (3)$$

According to (1) and (3), the input and output of the proportional and integral (PI) controller in the frequency loop can be obtained as in (4) and (5) (bottom of the page). Similarly, according to (1) and (3), the input and output of the integrator in the amplitude loop can be given by (6) and (7) (bottom of the next page).

It can be seen from (5) and (7) that the $2n^{\text{th}}$ harmonics cause ripples at $2n \pm 1$ times the fundamental frequency and that the $(2n+1)^{\text{th}}$

$$e(t) \cos(\theta) = \sum_{n=1}^{\infty} \frac{U_{2n+1}}{2} \left\{ \begin{array}{l} \sin[(2n+2)\omega_f t + \varphi_{2n+1} + \varphi_f] \\ + \sin(2n\omega_f t + \varphi_{2n+1} - \varphi_f) \end{array} \right\} + \sum_{n=1}^{\infty} \frac{U_{2n}}{2} \left\{ \begin{array}{l} \sin[(2n+1)\omega_f t + \varphi_{2n} + \varphi_f] \\ + \sin[(2n-1)\omega_f t + \varphi_{2n} - \varphi_f] \end{array} \right\} + U_{dc} \cos(\omega_f t + \varphi_f) \quad (4)$$

$$\begin{aligned} \Delta \omega = & -K_I \sum_{n=1}^{\infty} \frac{U_{2n+1}}{2} \left\{ \begin{array}{l} \frac{\cos[(2n+2)\omega_f t + \varphi_{2n+1} + \varphi_f]}{(2n+2)\omega_f} \\ + \frac{\cos(2n\omega_f t + \varphi_{2n+1} - \varphi_f)}{2n\omega_f} \end{array} \right\} - K_I \sum_{n=1}^{\infty} \frac{U_{2n}}{2} \left\{ \begin{array}{l} \frac{\cos[(2n+1)\omega_f t + \varphi_{2n} + \varphi_f]}{(2n+1)\omega_f} \\ + \frac{\cos[(2n-1)\omega_f t + \varphi_{2n} - \varphi_f]}{(2n-1)\omega_f} \end{array} \right\} + K_I \frac{1}{\omega_f} U_{dc} \sin(\omega_f t + \varphi_f) \\ & + K_P \sum_{n=1}^{\infty} \frac{U_{2n+1}}{2} \left\{ \begin{array}{l} \sin[(2n+2)\omega_f t + \varphi_{2n+1} + \varphi_f] \\ + \sin(2n\omega_f t + \varphi_{2n+1} - \varphi_f) \end{array} \right\} + K_P \sum_{n=1}^{\infty} \frac{U_{2n}}{2} \left\{ \begin{array}{l} \sin[(2n+1)\omega_f t + \varphi_{2n} + \varphi_f] \\ + \sin[(2n-1)\omega_f t + \varphi_{2n} - \varphi_f] \end{array} \right\} + K_P U_{dc} \cos(\omega_f t + \varphi_f) \end{aligned}$$

(5)

harmonics cause ripples at $2n$ and $2n+2$ times the fundamental frequency. Meanwhile, the DC offset causes ripple at the fundamental frequency in the outputs of both the frequency and amplitude loops. Therefore, either the harmonics or the DC offset causes a periodic disturbance in both the output frequency and amplitude. In summary, the conventional EPLL cannot obtain both a fast dynamic response and harmonic immunity.

C. Effect of Step Changes of the Fundamental Component

The dynamic performance of the conventional EPLL when amplitude step, phase angle and frequency jumps occur is derived in detail. To simplify the analysis, the following assumptions are made: (1) the input signal is an ideal sinusoidal wave, (2) only one variable changes at the start of each dynamic process, and (3) before the variable changes, the system has reached its steady state.

(1) Amplitude Step

First, considering the situation where the amplitude steps from U_f to U_{f1} , the input signal is described as:

$$u(t) = U_{f1} \sin(\omega_f t + \varphi_f) \quad (8)$$

The error signal is then derived as:

$$e(t) = u(t) - y(t) = (U_{f1} - U_f) \sin(\omega_f t + \varphi_f) \quad (9)$$

The amplitude and frequency estimated by the conventional EPLL are derived as:

$$\begin{aligned} A_{A1} &= A_0 + K_A \int (U_{f1} - U_f) \sin^2(\omega_f t + \varphi_f) dt \\ &= A_0 + \frac{K_A (U_{f1} - U_f)}{2} \left[t - \frac{\sin(2\omega_f t + 2\varphi_f)}{2\omega_f} \right] \end{aligned} \quad (10)$$

$$\begin{aligned} \omega_{A1} &= \omega_0 + K_I \int (U_{f1} - U_f) \sin(\omega_f t + \varphi_f) \cos(\omega_f t + \varphi_f) dt \\ &\quad + K_P (U_{f1} - U_f) \sin(\omega_f t + \varphi_f) \cos(\omega_f t + \varphi_f) \quad (11) \\ &= \omega_0 + \frac{(U_{f1} - U_f)}{2} \sqrt{K_P^2 + \left(\frac{K_I}{\omega_f}\right)^2} \sin\left(\begin{matrix} 2\omega_f t + 2\varphi_f \\ -\varphi_{A\omega} \end{matrix}\right) \end{aligned}$$

Where A_0 and ω_0 denote the initial value of the amplitude loop

and frequency loop, and $\varphi_{A\omega} = \arctan[K_I / (\omega_f K_P)]$. When an amplitude step change occurs in amplitude loop, except for DC term, a periodic ripple at the fundamental frequency is generated and in the frequency loop, a double-frequency periodic ripple is generated. Because the amplitudes of the dynamic periodic ripples in both the amplitude and the frequency loops are related to $U_{f1} - U_f$, when $U_{f1} = U_f$, the periodic ripples disappear. It means that periodic ripples exist only during the dynamic process, and they do not influence the steady state.

(2) Phase Angle Jump

Considering a phase angle jump to φ_{f1} , the input signal is:

$$u(t) = U_f \sin(\omega_f t + \varphi_{f1}) \quad (12)$$

The error signal is derived as:

$$e(t) = 2U_f \sin\left(\frac{\varphi_{f1} - \varphi_f}{2}\right) \cos\left(\omega_f t + \frac{\varphi_{f1} + \varphi_f}{2}\right) \quad (13)$$

The estimated amplitude and frequency of the conventional EPLL are derived as in (14) and (15) (bottom of the page).

$$A_{\varphi 1} = A_0 - \frac{K_A U_f}{2\omega_f} \sin\left(\frac{\varphi_{f1} - \varphi_f}{2}\right) \cos\left(2\omega_f t + \frac{\varphi_{f1} + \varphi_f}{2}\right) \quad (14)$$

Where $\varphi_{\varphi\omega} = \arctan(2\omega_f K_P / K_I)$. It can be seen from (14) and (15) that when the phase angle of the input signal jumps, a double-frequency ripple is generated in the amplitude loop. A DC term and a double-frequency ripple are generated in the frequency loop. The system will reach a new steady state without a double-frequency ripple in either the amplitude loop or the frequency loop when the estimated phase angle is equal to the input one.

(3) Frequency Jump

Considering a frequency jump to ω_{f1} , the input signal is:

$$u(t) = U_f \sin(\omega_{f1} t + \varphi_f) \quad (16)$$

The error signal is derived as:

$$e(t) = U_f \left[\sin(\omega_{f1} t + \varphi_f) - \sin(\omega_f t + \varphi_f) \right] \quad (17)$$

$$e(t) \sin(\theta) = \sum_{n=1}^{\infty} \frac{U_{2n+1}}{2} \left\{ \begin{matrix} \cos(2n\omega_f t + \varphi_{2n+1} - \varphi_f) \\ -\cos[(2n+2)\omega_f t + \varphi_{2n+1} + \varphi_f] \end{matrix} \right\} + \sum_{n=1}^{\infty} \frac{U_{2n}}{2} \left\{ \begin{matrix} \cos[(2n-1)\omega_f t + \varphi_{2n} - \varphi_f] \\ -\cos[(2n+1)\omega_f t + \varphi_{2n} + \varphi_f] \end{matrix} \right\} + U_{dc} \sin(\omega_f t + \varphi_f) \quad (6)$$

$$A' = K_A \sum_{n=1}^{\infty} \frac{U_{2n+1}}{2} \left\{ \begin{matrix} \frac{\sin(2n\omega_f t + \varphi_{2n+1} - \varphi_f)}{2n\omega_f} \\ -\frac{\sin[(2n+2)\omega_f t + \varphi_{2n+1} + \varphi_f]}{(2n+2)\omega_f} \end{matrix} \right\} + \sum_{n=1}^{\infty} \frac{U_{2n}}{2} \left\{ \begin{matrix} \frac{\sin[(2n-1)\omega_f t + \varphi_{2n} - \varphi_f]}{(2n-1)\omega_f} \\ -\frac{\sin[(2n+1)\omega_f t + \varphi_{2n} + \varphi_f]}{(2n+1)\omega_f} \end{matrix} \right\} - \frac{U_{dc}}{\omega_f} \cos(\omega_f t + \varphi_f) \quad (7)$$

$$\omega_{\varphi 1} = \omega_0 + U_f \sin\left(\frac{\varphi_{f1} - \varphi_f}{2}\right) \cdot \left\{ \sqrt{K_P^2 + \left(\frac{K_I}{2\omega_f}\right)^2} \sin\left(2\omega_f t + \frac{\varphi_{f1} + 3\varphi_f}{2} + \varphi_{\varphi\omega}\right) + \cos\left(\frac{\varphi_{f1} - \varphi_f}{2}\right) (K_I t + K_P) \right\} \quad (15)$$

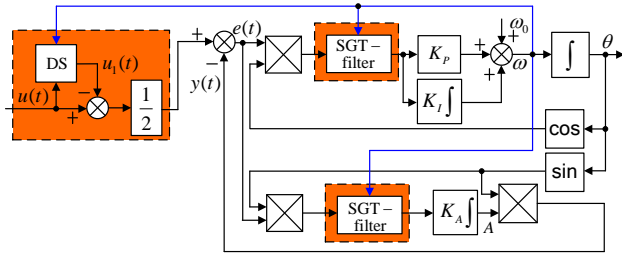


Fig. 2. Diagram of proposed HF-EPLL.

According to (1), the estimated amplitude and frequency of the conventional EPLL can be obtained as (18) and (19) (bottom of the page). When the frequency steps, a double-frequency ripple and a DC offset are generated in the output of the amplitude loop and a double-frequency ripple is generated in the output of the frequency loop. The system reaches a new steady state without a double-frequency ripple in the amplitude or frequency loop when the estimated frequency is equal to the input one.

III. IMPROVED EPLL BASED ON A HYBRID FILTER

Accordingly, a hybrid filters based EPLL (HF-EPLL) is proposed to eliminate the periodic ripple caused by these factors. Fig.2 shows the system configuration of the proposed HF-EPLL, where DS (delayed sampling) denotes the delayed sampling module. A DSC operator is employed in the input to eliminate the DC offset. In addition, a SGT-filter is introduced into both the frequency and amplitude loops to reject the periodic ripples caused by harmonics and step changes. The principle of the HF-EPLL is described in detail below.

After sampled and saved in DSs, the input signal is delayed by half of the fundamental period ($T_p = 2\pi / \omega_p$). Thus, the new signals consisting only of fundamental component and odd-order harmonics can be obtained by the following mathematical operation between the input signal and its delayed one:

$$\frac{1}{2}[u(t) - u(t - \frac{T_p}{2})] = u_i(t) + \sum_{n=1}^{\infty} U_{2n+1} \sin[(2n+1)\omega t + \varphi_{2n+1}] \quad (20)$$

Thus, the DC offset has been eliminated before inputting the EPLL. Only the odd-order harmonics exist in the new input signal. It can be known from the principle of the EPLL that

the odd-order harmonics cause periodic ripples at odd-order frequencies in the inputs of the frequency and amplitude loops. This effect is similar to the ones caused by step changes. Correspondingly, a SGT-filter is introduced in the frequency loop and amplitude loop to eliminate the effects. The SGT-filter is derived from the sliding Discrete Fourier Transform (DFT). According to the sliding DFT, the spectral component of the k^{th} frequency at time q for every N input time sample is derived as follows:

$$X_q(k) = e^{j-2\pi k/N} X_{q-1}(k) + x(q) - x(q-N) \quad (21)$$

Where $x(q)$ and $x(q-N)$ denote the sampling results at times q and $q-N$, respectively. Therefore, when $k=0$, the obtained signal only contains a DC component. The z-domain transfer function of the SGT-filter when $k=0$ is:

$$f(z) = \frac{1}{N} \frac{1-z^{-N}}{1-z^{-1}} \left(N = \frac{f_s}{f_0} \right) \quad (22)$$

Where f_s and f_0 denote the sampling and fundamental frequencies, respectively. With this filter, frequencies listed in (23) can be rejected while the DC component remains.

$$f = N' f_0 \quad (N' = 1, 2, \dots, N/2) \quad (23)$$

After applying the DSC operator to the system, the lowest frequency of the ripples included in the input signals of the frequency and amplitude loops are twice the fundamental frequency. Since the fundamental frequency in the Chinese grid is 50Hz, $f_0 = 100\text{Hz}$ was chosen for this study.

In addition, after choosing a sampling frequency of 10kHz as f_s in this system, $N=10k/100=100$ can be obtained. Furthermore, the estimated frequency is introduced into the DSC operator and SGT-filter. Thus, the sampling frequency can be adjusted online to enhance the frequency adaptability of the HF-EPLL.

IV. EXPERIMENTAL RESULTS AND COMPARISON

Experiments with a conventional EPLL and the HF-EPLL on a DSP chip (TMS30F28335) - based platform are performed in order to validate the presented analysis. The input signal is programmed in a DSP and transported to the EPLL algorithm. The input signal and estimated information are then transferred to an analog quantity with a DAC chip (DAC7515) so that they can be observed through an oscilloscope. The initial amplitude of the input signal is set

$$A_{\omega_1} = A_0 + \frac{K_A U_f}{2} \left\{ \frac{\sin[(\omega_{f_1} - \omega_f)t]}{\omega_{f_1} - \omega_f} + \frac{\sin(2\omega_f t + 2\varphi_f)}{2\omega_f} - \frac{\sin[(\omega_{f_1} + \omega_f)t + 2\varphi_f]}{\omega_{f_1} + \omega_f} - t \right\} \quad (18)$$

$$\omega_{\omega_1} = \omega_0 + \frac{U_f}{2} \left\{ \sqrt{K_p^2 + \left(\frac{K_I}{\omega_{f_1} - \omega_f} \right)^2} \sin \left[\begin{array}{l} (\omega_{f_1} - \omega_f)t \\ + 2\varphi_f - \varphi_{\omega\omega_1} \end{array} \right] + \sqrt{K_p^2 + \left(\frac{K_I}{2\omega_f} \right)^2} \sin \left[\begin{array}{l} 2\omega_f t + 2\varphi_f \\ - \varphi_{\omega\omega_2} \end{array} \right] + \sqrt{K_p^2 + \left(\frac{K_I}{\omega_{f_1} + \omega_f} \right)^2} \sin \left[\begin{array}{l} (\omega_{f_1} + \omega_f)t \\ + 2\varphi_f - \varphi_{\omega\omega_3} \end{array} \right] \right\} \quad (19)$$

Where $\varphi_{\omega\omega_1} = \arctan\{K_I / [K_p(\omega_{f_1} - \omega_f)]\}$, $\varphi_{\omega\omega_2} = \arctan[K_I / (K_p 2\omega_f)]$, $\varphi_{\omega\omega_3} = \arctan\{K_I / [K_p(\omega_{f_1} + \omega_f)]\}$.

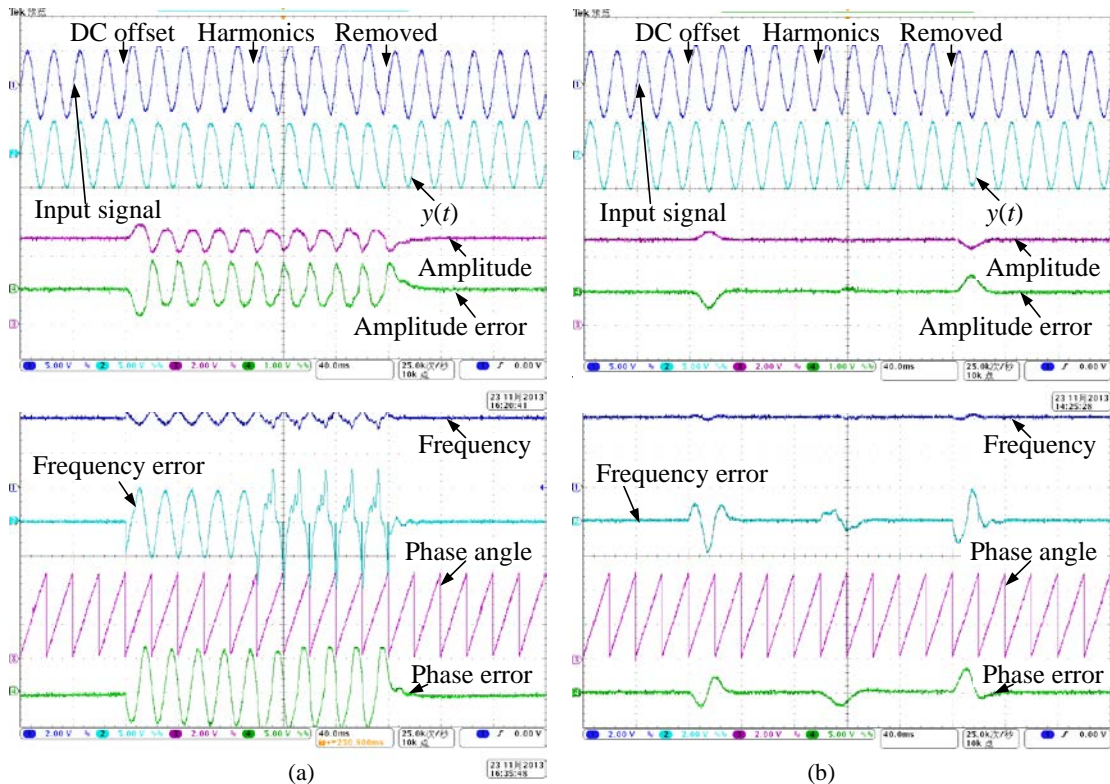


Fig. 3. Experimental waveforms with DC offset and harmonics. Scale: Input signal: 1.0 p.u./div, $y(t)$: 1.0p.u./div, Amplitude: 0.4p.u./div, Amplitude error: 0.2p.u./div, Frequency: 25Hz/div, Frequency error: 5Hz/div, Phase angle: 144°/div, Phase error: 5°/div, time: 40ms/div. (a) EPLL. (b) HF-EPLL.

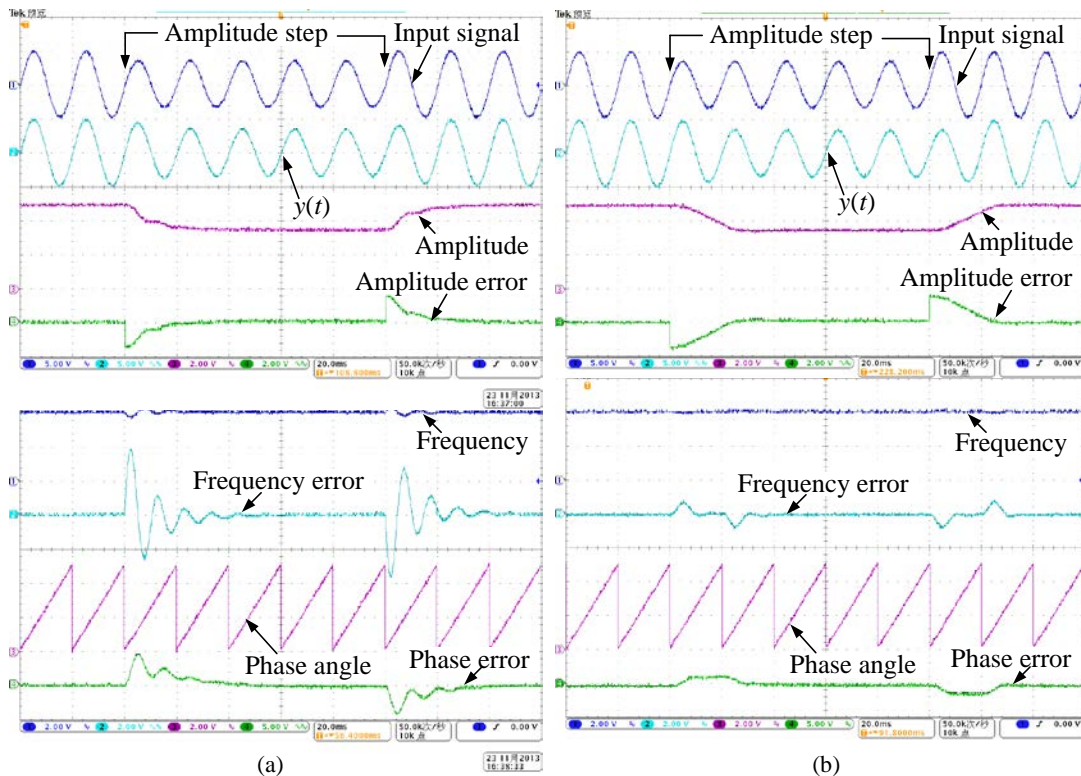


Fig. 4. Experimental waveforms with amplitude step. Scale: Input signal: 1.0 p.u./div, $y(t)$: 1.0p.u./div, Amplitude: 0.4p.u./div, Amplitude error: 0.4p.u./div, Frequency: 25Hz/div, Frequency error: 2Hz/div, Phase angle: 144°/div, Phase error: 5°/div, time: 20ms/div. (a) EPLL. (b) HF-EPLL.

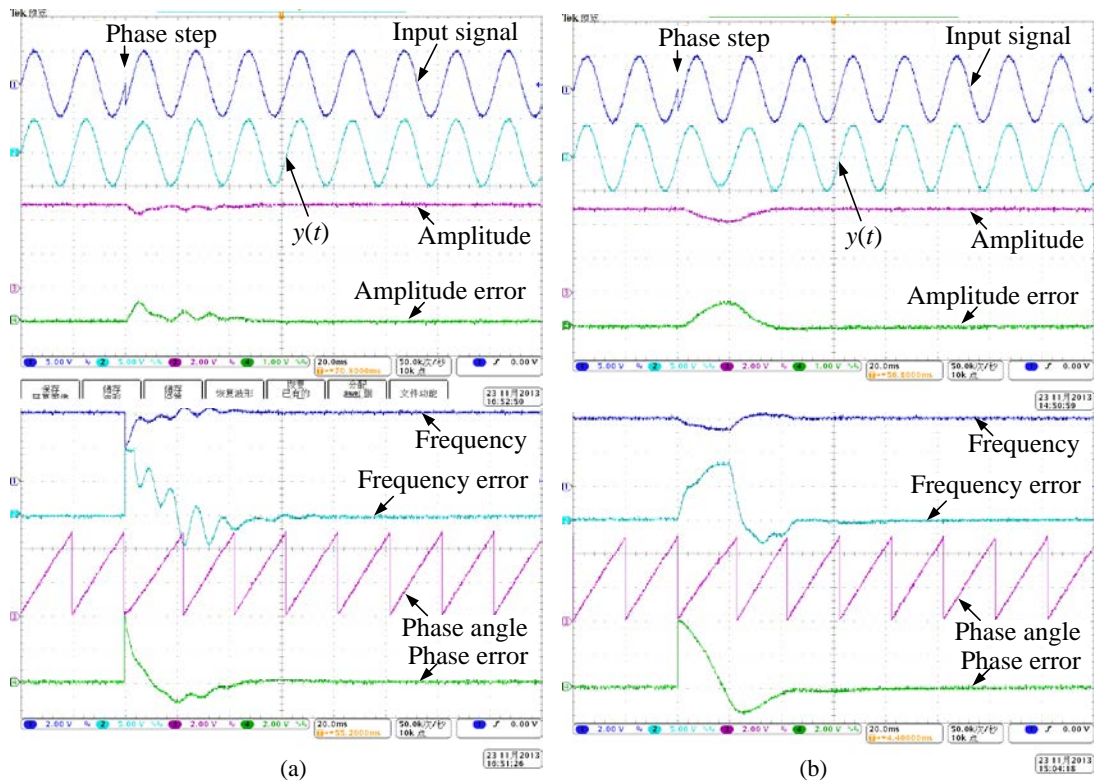


Fig. 5. Experimental waveforms with phase angle jump. Scale: Input signal: 1.0 p.u./div, $y(t)$: 1.0p.u./div, Amplitude: 0.4p.u./div, Amplitude error: 0.2p.u./div, Frequency: 25Hz/div, Frequency error: 5Hz/div, Phase angle: 144° /div, Phase error: 20° /div, time: 20ms/div. (a) EPLL. (b) HF-EPLL.

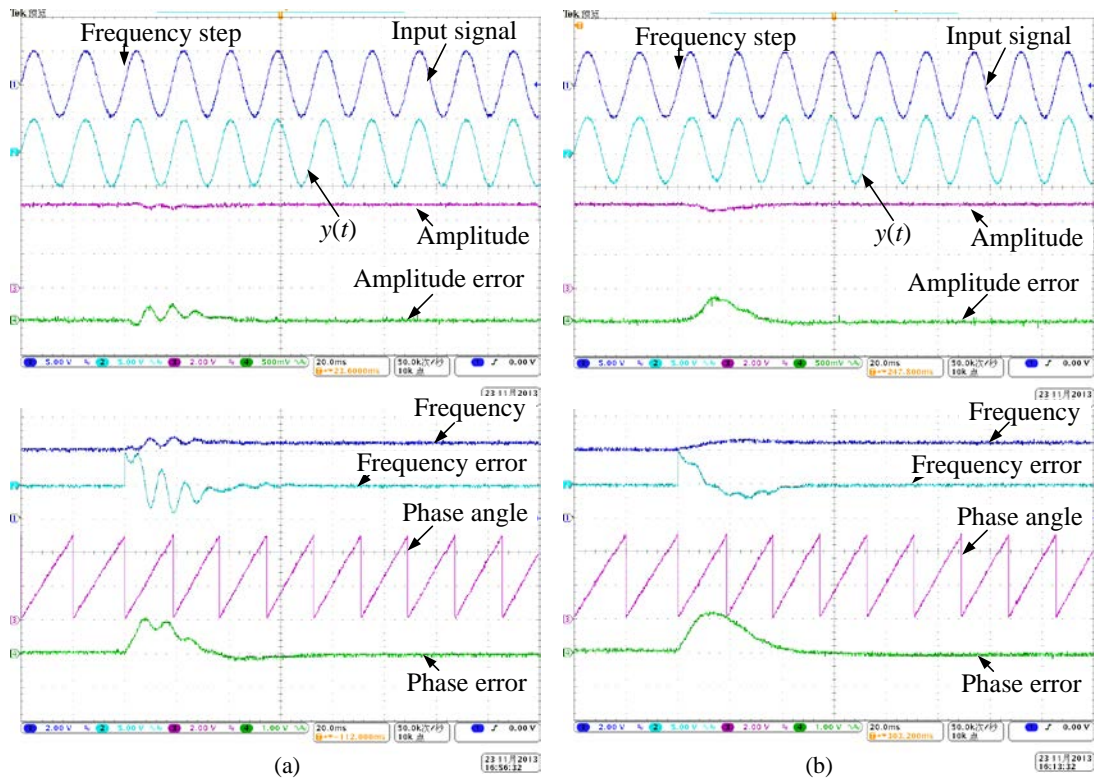


Fig. 6. Experimental waveforms with Frequency step. Scale: Input signal: 1.0 p.u./div, $y(t)$: 1.0p.u./div, Amplitude: 0.4p.u./div, Amplitude error: 0.1p.u./div, Frequency: 25Hz/div, Frequency error: 5Hz/div, Phase angle: 144° /div, Phase error: 1° /div, time: 20ms/div. (a) EPLL. (b) HF-EPLL.

with a nominal voltage (1 p.u.), and the frequency is 50Hz. In [16], the design rule of the various parameters of the EPLL has been presented in detail. According to [16], the parameters of the controller in the EPLL are selected as $K_A = 130$, $K_P = 130$, and $K_I = 3000$.

First, the performances of the conventional EPLL and the proposed EPLL suffering from the input harmonics and DC offset are tested. First, a 0.2 p.u. DC offset is added, and the 0.1 p.u. 2nd, 0.1 p.u. 3rd, 0.05 p.u. 5th, and 0.03 p.u. 7th harmonics are added after 100 ms. The corresponding voltage total harmonics distortion is 15.8%. Furthermore, after another 100ms, both the DC offset and the harmonics are removed. Fig. 3 shows the waveforms of the two EPLLs. Both of the EPLLs can obtain the correct information with an ideal sinusoidal wave. When the DC offset is added, a periodic disturbance is introduced in the estimated amplitude, phase angle and frequency of the conventional EPLL. Because of the introduction of input harmonics, periodic ripples are also generated in the estimated amplitude, phase angle and frequency. The proposed EPLL can estimate the required information without steady-state errors or ripples under both harmonics and DC offset. The settling time is less than 30 ms.

Moreover, the dynamic performances of the two EPLLs are tested. The case of an input signal amplitude step of $\pm 30\%$ is performed first and the experimental results are shown in Fig. 4. During the dynamic processes, there is twice frequency periodic ripple in the estimated results of the EPLL. The settling time of the EPLL is about 40ms, the maximum frequency error is about 4Hz and the maximum phase error is about 5° . The proposed EPLL shows a better dynamic response, with a settling time of 30ms, a maximum frequency error of 0.8Hz and a maximum phase error of 1.8° . In addition, there is almost no periodic ripple in the estimated results.

Secondly, the case of a phase angle jump of 40° is tested and the experimental results are shown in Fig. 5. For the dynamic response of the conventional EPLL, the maximum amplitude error is about 0.1p.u., and the maximum frequency error 10Hz. There is twice frequency periodic ripple in the estimated results. As for the proposed HF-EPLL, the dynamic time is about 45ms, the maximum amplitude error is 0.15p.u., and the maximum frequency error is 8Hz. Like the cases of the amplitude steps, the periodic ripples in the estimated results are so tiny that they can be neglected.

Finally, the case of a frequency jump from 50Hz to 55Hz is tested and the experimental results are shown in Fig. 6. The settling time of the conventional EPLL is 40ms, the maximum amplitude error is 0.05p.u., and the maximum phase angle error is 1° . There is a periodic ripple in the estimated results, and the frequency is about 100Hz. For the HF-EPLL, the dynamic time is about 40ms, the maximum amplitude error is 0.08p.u., the maximum frequency error is

5Hz, and the maximum phase error is about 1° . Just like the cases of the amplitude step and the phase angle jump, the periodic ripples in the estimated results are still tiny.

V. CONCLUSION

The conventional EPLL does not have the ability of rejecting the effects of input harmonics and DC offset, which cause periodic ripples in the estimated results. On the other hand, a step change of the input fundamental component also causes a transient periodic ripple in the estimated results. The proposed HF-EPLL achieves correct estimation of the synchronization information of the input signal with an almost equal settling time and a smaller transient oscillation relative to conventional EPLL, even under the presence of harmonics and DC offset. The proposed EPLL can be implemented easily by a digital controller while the burden of the digital controller is not noticeably increased.

ACKNOWLEDGMENT

This project was supported by the National Science Foundation of China (Grant No. 51107018 and 61403277).

REFERENCES

- [1] S. Golestan, M. Monfared, F. D. Freijedo, and J. M. Guerrero, "Dynamics assessment of advanced single-phase PLL structures," *IEEE Trans. Ind. Electron.*, Vol. 60, No. 6, pp. 2167-2177, Jun. 2013.
- [2] A. Ozdemir, I. Yazici, C. Vural, "Fast and robust software-based digital phase-locked loop for power electronics applications," *IET Gener. Transm. Distrib.*, Vol. 7, No. 12, pp. 1435-1441, Dec. 2013.
- [3] L. Wang, Q. Jiang, L. Hong, C. Zhang, and Y. Wei, "A novel phase-locked loop based on frequency detector and initial phase angle detector," *IEEE Trans. Power Electron.*, Vol. 28, No. 10, pp. 4538-4549, Oct. 2013.
- [4] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.*, Vol. 53, No. 5, pp. 1398-1409, Oct. 2006.
- [5] A. Teke, M. E. Meral, and M. U. Cuma, "OPEN unified power quality conditioner with control based on enhanced phase locked loop," *IET Gener. Transm. Distrib.*, Vol. 7, No. 3, pp. 254-264, Mar. 2013.
- [6] R. S. Filho, P. Seixas, P. Cortizo, A. Souza, and L. A. B. Torres, "Comparison of three single-phase PLL algorithms for UPS applications," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 8, pp. 2923-2932, Aug. 2008.
- [7] M. Karimi-Ghartemani, H. Karimi, and M. R. Iravani, "A magnitude/phase-locked loop system based on estimation of frequency and in-phase/quadrature-phase amplitudes," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 2, pp. 511-517, Feb. 2004.
- [8] S. M. Silva, B. M. Lopes, B. J. C. Filho, R. P. Campana, and W. C. Bosventura, "Performance evaluation of PLL algorithms for single-phase grid-connected systems," in *Proc. IEEE 39th Ind. Appl. Soc. Annu. Meet. Ind. Appl.*

- Conf.*, Vol. 4, pp. 2259-2263, 2004.
- [9] A. Nicasari and A. Nagliero, "Comparison and evaluation of the PLL techniques for the design of the grid-connected inverter systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Vol. 7, pp. 3865-3870, 2010.
- [10] F. Xiong, W. Yue, L. Ming, and L. Jinjun, "A novel frequency-adaptive PLL for single-phase grid-connected converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, Vol. 9, pp. 414-419, 2010.
- [11] B. P. McGrath, D. G. Holmes, and J. J. H. Galloway, "Power converter line synchronization using a discrete Fourier transform (DFT) based on variable sampling rate," *IEEE Trans. Power Electron.*, Vol. 20, No. 4, pp. 877-884, Apr. 2005.
- [12] M. A. Perez, J. R. Espinoza, L. A. Moran, M. A. Torres, and E. A. Araya, "A robust phase-locked loop algorithm to synchronize static-power converters with polluted AC systems," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 5, pp. 2185-2192, May 2008.
- [13] I. Carugati, P. Donato, S. Maestri, D. Carrica, and M. Benedetti, "Frequency adaptive PLL for polluted single-phase grids," *IEEE Trans. Power Electron.*, Vol. 27, No. 5, pp. 2396-2404, May 2012.
- [14] M. Karimi-Ghartemani, B. Ooi, and A. Bakhshai, "Application of enhanced phase-locked loop system to the computation of synchrophasors," *IEEE Trans. Power Del.*, Vol. 26, No. 1, pp. 22-32, Jan. 2011.
- [15] M. Karimi-Ghartemani, "Linear and pseudolinear enhanced phased- locked loop (EPLL) structures," *IEEE Trans. Ind. Electron.*, Vol. 61, No. 3, pp. 1464-1474, Mar. 2014..
- [16] M. Karimi-Ghartemani, S. A. Khajehoddin, K. P. Jain, and A. Bakhshai, "Derivation and design of in-loop filters in phase-locked loop systems," *IEEE Trans. Instrum. Meas.*, Vol. 61, No. 4, pp. 930-939, Apr. 2012.
- [17] M. Karimi-Ghartemani, S. A. Khajehoddin, K. P. Jain, and A. Bakhshai, "Comparison of two methods for addressing DC component in phase-locked loop systems," *Energy Conversion Congress and Exposition (ECCE), 2011 IEEE*, Vol. 10, pp. 3053-3058, 2011.

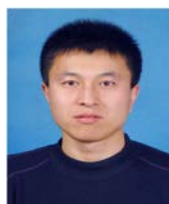
- [18] M. Karimi-Ghartemani, S. A. Khajehoddin, P. Jain, A. Bakhshai, and M. Mojiri, "Addressing dc component in PLL and notch filter algorithms," *IEEE Trans. Power Electron.*, Vol. 27, No. 1, pp. 78-86, Jan. 2012.



Linsong Luo received his B.S. degree from the Northeast Forestry University, Harbin, China, in 2012. He is presently working towards his M.S. degree in the Department of Electrical Engineering, Tianjin Polytechnic University, Tianjin, China. His current research interests include grid-connected inverters for renewable energy generation.



Huixin Tian received her B.S. degree in Automation from Fushun Petroleum College, Fushun, China, in 2001, and her M.S. and Ph.D. degrees in Information Science and Engineering from Northeastern University, Shenyang, China, in 2005 and 2009, respectively. She is presently an Associate Professor and a Master's Degree supervisor at Tianjin Polytechnic University, Tianjin, China. Her current research interests including modeling, control and optimization in complex industrial systems.



Fengjiang Wu received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from the Harbin Institute of Technology, Harbin, China, in 2002, 2004 and 2007, respectively. Since 2007, he has been with the Department of Electrical Engineering, Harbin Institute of Technology, where he is presently an Associate Professor. His current research interests include renewable energy generation, microgrids, multilevel inverter technology and electric machines drives.