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Practical Implementation of an Interleaved Boost Converter for Electric Vehicle Applications

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Abstract

This study presents a practical implementation of a multi-mode two-phase interleaved boost converter for fuel cell electric vehicle application. The main operating modes, which include two continuous conducting modes and four discontinuous conducting modes, are discussed. The boundaries and transitions among these modes are analyzed with consideration of the inductor parasitic resistance. The safe operational area is analyzed through a comparison of the different operating modes. The output voltage and power characteristics with open-loop or closed-loop operation are also discussed. Key performance parameters, including the DC voltage gain, input ripple current, output ripple voltage, and switch stresses, are presented and supported by simulation and experimental results.

Key words: CCM, DCM, Fuel Cell Electric Vehicle, Inductor parasitic resistance, Interleaved Boost Converter, Mode Transition, SOA

I. INTRODUCTION

Fuel cell electric vehicles (FCEVs) have been extensively used nowadays to replace the traditional internal combustion engine-based vehicles because of the advantages of the former in the aspects of high energy density, zero emissions, and high efficiency [1]-[5]. Fuel cell (FC) stacks can provide power for the motors, either stand-alone or combined with renewable energy sources, such as photovoltaic modules or wind turbines [6]. Among various FC technologies available for vehicle application, the proton exchange membrane fuel cell (PEMFC) is regarded as the best candidate because of its high power density and low operating temperatures [7]-[9]. Fig. 1 illustrates a typical volt-ampere characteristic of a 6 kW PEMFC stack, which comprises 65 FCs. The output voltage of the FC stack varies with the stack output current, which is determined with the FCEV output power demand. Fig. 1 shows that the output voltage of the FC stack in the low-power region is higher than that in the high-power region.

FC stacks exhibit good power capability for steady-state operation; however, their dynamic response is relatively low [10]-[12]. Thus, energy storage systems (ESS), including batteries or supercapacitors, are required to integrate with the FC stacks to provide high transient current and recover energy during the regenerative braking [13]. Fig. 2 shows the FCEV system topology, including the main power source (PEMFC), high power DC-DC converter connecting FC with the high-voltage DC bus, inverter, and motor. An auxiliary power source, including a battery stack or ultracapacitor, is also connected to the high-voltage DC bus via bidirectional DC-DC converter for its rapid dynamic response. The total power of the EV DC bus P_{DC} is provided by two sources, namely, FC stacks P_{FC} and supercapacitors P_{ESD}.

For the FC application, a high-power DC-DC power interface is the key component to achieve excellent power management and full usage of the FC stacks. High voltage ratio is one of the most important requirements for this DC-DC converter. Fig. 1 shows that FC is the main energy source to power the vehicles, and its voltage changes in a wide range. The current ripple and its harmonic content are

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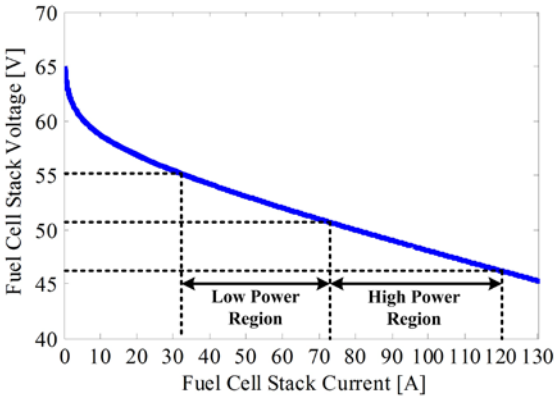


Fig. 1. Volt-ampere characteristic of fuel cell stacks based on power demands.

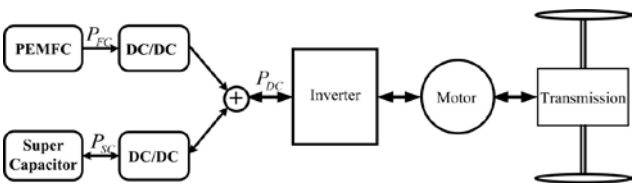


Fig. 2. Vehicle system topology of FCEV.

also determining factors for the FC lifetime [14], [15]. Volume, cost, weight, manufacturing complexity, and efficiency are also major concerns for the high-power DC-DC converter.

Several topologies have been discussed in prior studies, including conventional boost converter [16], buck-boost converter [17], half-bridge [18] or full-bridge converter [19], and push-pull converter [20]. Considering the increasing demands in power density, non-isolated DC-DC converter is preferred for FCEV application. For the conventional boost converter (CBC), the major concern is the boost inductor because it is the heaviest component in the high-power DC-DC converter. A low inductance is preferred to reduce the inductor size and weight. However, this condition will result in high input current ripple and affect the FC stack lifetime. The CBC efficiency is also lower for a higher duty cycle [21], [22]. A multi-device structure with interleaved control was proposed in [12] to reduce the input current ripples and the passive component size. However, the component number is doubled, which will lower the system reliability. A high-gain three-level boost converter for FCEV vehicle applications was discussed in [23]. However, the current control for this topology is complicated and the neutral-point voltage balance is still a design challenge. An interleaved reduced-component-count DC-DC converter was discussed in [24] in FCEV with a multi-voltage electric net. However, this system is difficult to use for high power applications.

From the previous analysis, an interleaved boost converter (IBC) can be used to improve the power density and transient response [25], [26]. For low-power application, the interleaved winding-coupled boost converter is commonly

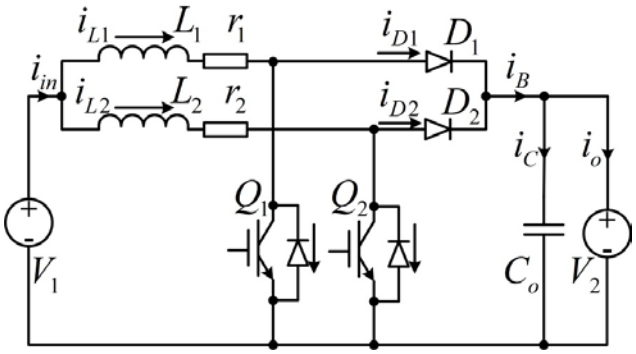


Fig. 3. Topology of a two-phase interleaved boost converter.

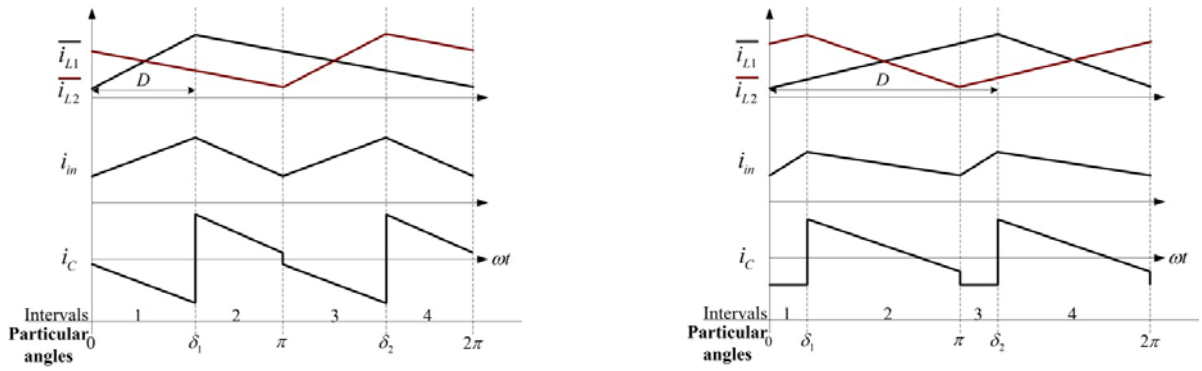
used [27]-[29]. However, for FCEV application, the inductor current reaches 600 A, and the coupled inductor is difficult to manufacture. IBC can be controlled to operate in two modes, namely, continuous conduction mode (CCM) or discontinuous conduction mode (DCM). A total of two CCMs and four DCMs are present for a two-phase IBC. The input current ripple patterns of a two-phase IBC are highly complicated. Thus, discussing the key performance parameters is essential, which include the DC voltage gain, input ripple current, output ripple voltage, and switch stresses that consider the parasitic resistance effects.

In the current study, a practical implementation of a multi-mode two-phase IBC is presented for FCEV applications. Various modes, including two CCMs and four DCMs, are discussed with their equivalent circuits. The effects of the inductor parasitic resistance in the voltage conversion ratio are analyzed. The safe operational area is analyzed through a comparison of the different operation modes. The output voltage and power characteristics with open-loop or closed-loop operation are discussed. Simulation and experimental result are also presented.

II. IBC Operating Modes

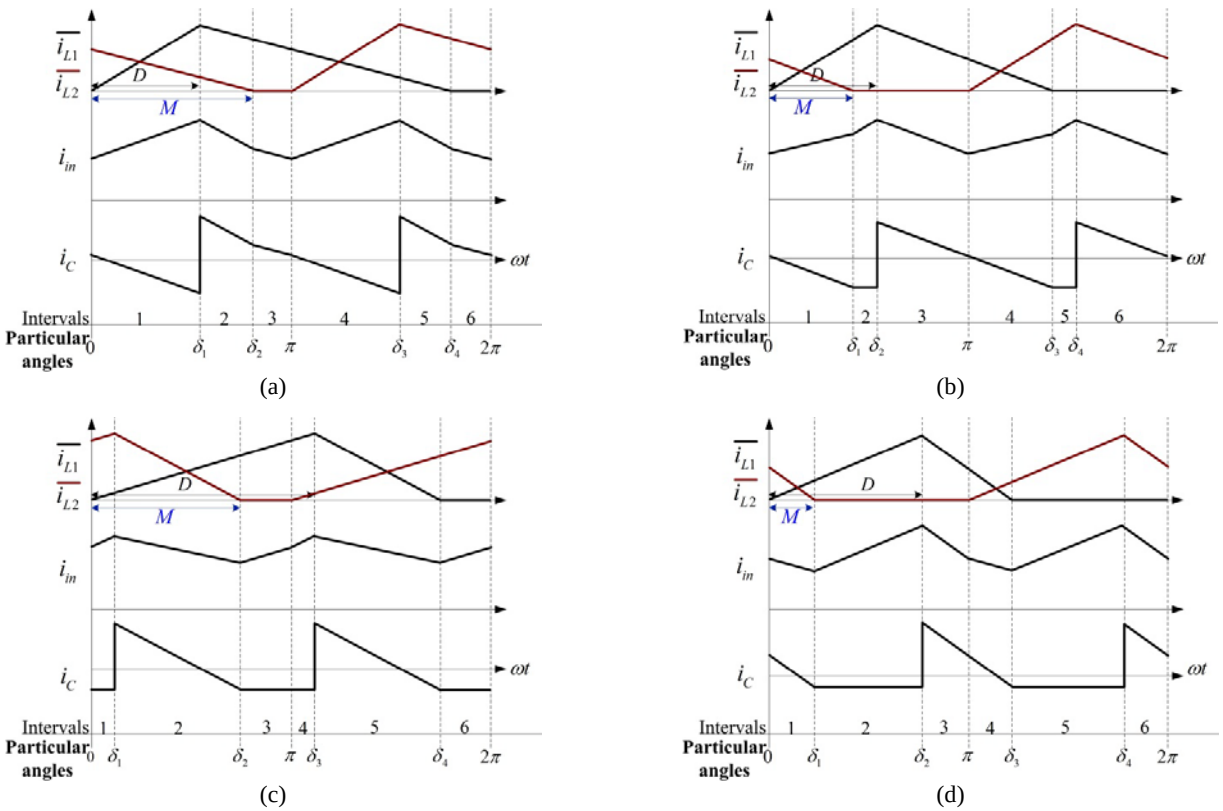
Fig. 3 depicts the topology of the two-phase IBC. This converter consists of two CBCs interleaved with one IGBT and diodes connected in parallel. The phase-shift interleaved operation will double the inductor current ripple frequency and reduce the size of the inductor. A rapid dynamic response for the converter can also be achieved because of the increased system bandwidth.

For the two-phase interleaved IBC, the phase shift between the gate drive signals for *Q1* and *Q2* is 180°. The input current is the sum of the two phase currents. Fig. 1 shows that the operating voltage of the FC stack is changing with different power regions of FCEV. IBC should regulate its duty ratio *D* to provide a certain voltage to the motor inverter. One constraint is that the input current i_{in} must be designed in CCM because FC is the main power source in the FCEV system. However, each phase current can operate in either CCM or DCM. Thus, a total of two CCMs and four DCMs



(a) (b)

Fig. 4. Typical IBC waveforms with *CCM*. (a) *CCM-I*: $0 < D < 0.5$; (b)*CCM-II*: $0.5 \le D < 1$.



(a) (b)

(c) (d)

Fig. 5. Typical IBC waveforms with *DCM*. (a) *DCM-I*; (b) *DCM-II*; (c) *DCM-III*; and (d) *DCM-IV*.

are present based on the duty ratio range and input current distribution.

Fig. 4 illustrates the typical IBC waveforms for two CCMs. Fig. 4(a) shows that in the low-power region case, only one inductor current is increasing during $0-\delta_1$ and all switches are off during $\delta_1-\pi$. Thus, during $\delta_1-\pi$, both the inductor and input currents are decreasing. However, Fig. 4(b) shows that for the high-power region, at least one phase has an increased inductor current for each stage. During $0-\delta_1$ and $\delta_2-\pi$, two inductor currents are increasing for these two stages.

Fig. 5 illustrates the typical IBC waveforms for DCM. Four operating modes are present based on the duty ratio range and input current distribution. The main differences in these modes are reflected on the boost inductor current waveforms. For DCM, each inductor current has three states, namely, rising, falling, and zero. These three states are symbolized as "R", "F", and "Z," respectively. Thus, considering all the possible combinations of two IBCs, a total of eight operations are possible: "R-R," "R-F," "R-Z," "F-R," "F-F," "F-Z," "Z-R," and "Z-F." Fig. 6 illustrates the equivalent circuits. These eight equivalent circuits can explain all the operating modes, whether CCM or DCM. DCM-II is used as an example to analyze the operation briefly.

TABLE I
OPERATING MODES AND MAIN SUB-CIRCUITS

Modes	Main Subcircuits
CCM-I	$B \to E \to D \to E$
CCM-II	$A \to B \to A \to D$
DCM-I	$B \to E \to F \to D \to E \to H$
DCM-II	$B \to C \to F \to D \to G \to H$
DCM-III	$A \to B \to C \to A \to D \to G$
DCM-IV	$A \to C \to F \to D \to G \to H$

"*R-F*" operation during [0–δ_1]: Q_1 is turned on and current i_{L1} is increasing linearly from zero. Diode D_2 is conducting to freewheel the current i_{L2}. Thus, i_{L2} is decreasing to zero. Based on the volt-second balance, the duration of the current i_{L1} decreasing to zero is defined as M and can be expressed as

$$M = \frac{2dD - d + 1}{2d - 2} \tag{1}$$

where the voltage conversion ratio $d = V_2/V_1$. The output capacitor current i_C during this stage is expressed as

$$i_C = i_B - i_o = i_{L2} - i_o \tag{2}$$

"*R-Z*" operation during [δ_1–δ_2]: Q_1 is still on and current i_{L1} is increasing to the maximum I_{max_L1}. Diode D_2 is off during this stage. The input current i_{in} is the same as i_{L1}. The output capacitor current i_C is the opposite of the load current i_o. The current I_{max_L1} can be expressed as:

$$I_{\max\_L1} = \frac{DV_2}{dL_s f_s} \tag{3}$$

"*F-Z*" operation during [δ_2–π]: Current i_{L2} remains constantly zero. Diode D_1 is conducting to freewheel the current i_{L1}. Thus, the current i_{L1} is decreasing linearly. The output capacitor current i_C during this stage is expressed as

$$i_C = i_B - i_o = i_{L1} - i_o \tag{4}$$

A similar operation can be analyzed for the rest stages of "*F-R*," "*Z-R*," and "*Z-F*." TABLE I shows that all operating modes can be explained by using the eight possible operations.

III. MODES DISTRIBUTION AND BOUNDARIES

A. DCM and CCM

The input current i_{in}, which is the sum of i_{L1} and i_{L2}, can be expressed as

$$i_{in} = i_{L1} + i_{L2} \tag{5}$$

With the dynamics of the currents i_{L1} and i_{L2} shown in Fig. 3, the analytical expressions of current i_{in} at the switching angles for each operating mode of IBC can be derived. TABLE II shows the expressions of the input current at the switching angles.

For mode I, the relationship of the voltage conversion ratio d and the duty cycle D can be expressed as

$$d_{CCM} = 1/(1-D) \tag{6}$$

However, the average current of input current i_{in} for DCM-II can be expressed as

$$\begin{aligned}\overline{i_{in}} &= \left[i_L(0) + i_L(\delta_1)\right]M + \left[i_L(\delta_1) + i_L(\delta_2)\right](D - M) \\ &+ \left[i_L(\delta_2) + i_L(0)\right](0.5 - D) = \frac{V_2 D^2}{(d-1)L_s f_s}\end{aligned} \tag{7}$$

If the power losses in the components are neglected and the equivalent load resistance is R, then the IBC power transfer characteristic can be expressed as

$$\frac{V_2^2}{R} = V_1\overline{i_{in}} = \frac{V_2^2 D^2}{d(d-1)L_s f_s} \tag{8}$$

Thus,

$$d^2 - d - RD^2/L_s f_s = 0 \tag{9}$$

$$d_{DCM-II} = \frac{\sqrt{4RD^2 L_s f_s + L_s^2 f_s^2}}{2L_s f_s} + \frac{1}{2} \tag{10}$$

Define $k = R/L_s f_s$; thus, (10) can be simplified as

$$d_{DCM-II} = \frac{\sqrt{4D^2 k + 1}}{2} + \frac{1}{2} \tag{11}$$

As shown in (11), the voltage conversion ratio for DCM-II is affected by the circuit parameters and load conditions. Fig. 7(a) shows the simulated waveforms of "i_{L1}," "i_{L2}," "i_{in}," "i_C," and "v_{out}" under the condition of "v_{in} = 100 V, v_{out} = 400 V, P_o = 2.91 kW." IBC operates in CCM-II. However, for the same P_o, IBC will operate in DCM-III, as shown in Fig. 7(b). By using DCM, the inductance will be reduced from 300 μH to 180 μH, and the input current ripple is merely slightly
increased. Fig. 7(c) shows that the output voltage ripple with DCM-III is lower than that with CCM-II. The reduction of inductance is beneficial for the size reduction and power density improvement. The power devices can also be operated with ZCS; thus, the switching loss of IGBTs and the reverse recovery loss of the diodes can be reduced [30].

B. Mode Distribution and Their Boundaries

A total of four criteria determine the mode distribution.

(1) ***Boundary I***: The line of D = 0.5 is the boundary line of CCM-I and CCM-II, DCM-III, and the other three DCMs;

(2) ***Boundary II***: The line D = M will distinguish DCM-I with DCM-II and DCM-IV;

(3) ***Boundary III***: The difference between DCM-II and DCM-IV is the current slope of i_{L1} and i_{L2} during [0, δ_1]. The boundary line is expressed as

$$D = D/(d-1) \tag{12}$$

$$d = 2 \tag{13}$$

Combining (1) and (13), the boundary line can be derived

$$D = 0.25 + 0.5M \tag{14}$$

(4) ***Boundary IV***: For each mode, the total rising and falling duration should be shorter than one switching period. Thus,

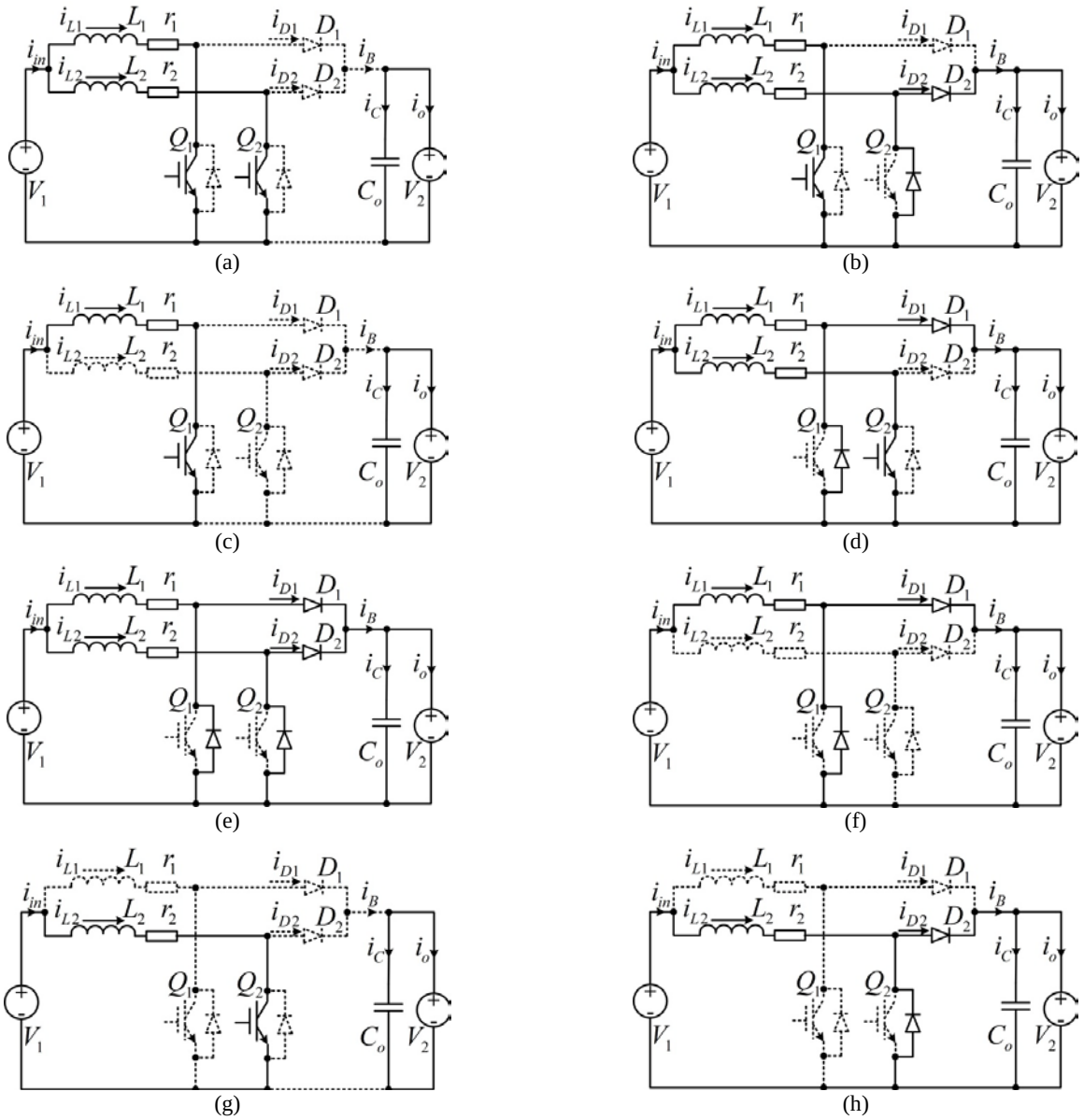


Fig. 6. Equivalent circuits of the IBC. (a) "R-R"; (b) "R-F"; (c) "R-Z"; (d) "F-R"; (e) "F-F"; (f) "F-Z"; (g) "Z-R"; (h) "Z-F."

TABLE II

EXPRESSIONS OF THE INPUT CURRENT AT THE SWITCHING ANGLES (PU)

Modes	$i_{in}(0)$	$i_{in}(\delta_1)$	$i_{in}(\delta_2)$
CCM_I	$\frac{P}{V_2(1-D)}+\frac{D(2D-1)V_2}{2L_s f_s}$	$\frac{P}{V_2(1-D)}+\frac{D(1-2D)V_2}{2L_s f_s}$	-
CCM_II	$\frac{P}{V_2(1-D)}+\frac{\left(d-2D-2dD+\mathrm{d}D^2+2D^2\right)V_2}{2L_s f_s}$	$\frac{P}{V_2(1-D)}-\frac{\left(d+2D-6dD+9\mathrm{d}D^2-2D^2-4dD^3\right)V_2}{2L_s f_s}$	-
DCM_I	$\frac{(2dD-d+1)V_2}{2dL_s f_s}$	$\frac{(4D-d+1)V_2}{2dL_s f_s}$	$\frac{(d-1)V_2}{2dL_s f_s}$
DCM_II (DCM_IV)	$\frac{(2dD-d+1)V_2}{2dL_s f_s}$	$\frac{(2dD-d+1)V_2}{2(d-1)dL_s f_s}$	$\frac{DV_2}{dL_s f_s}$
DCM_III	$\frac{V_2}{2dL_s f_s}$	$\frac{(4D-1)V_2}{2dL_s f_s}$	$\frac{(2dD-d+1)V_2}{2(d-1)dL_s f_s}$

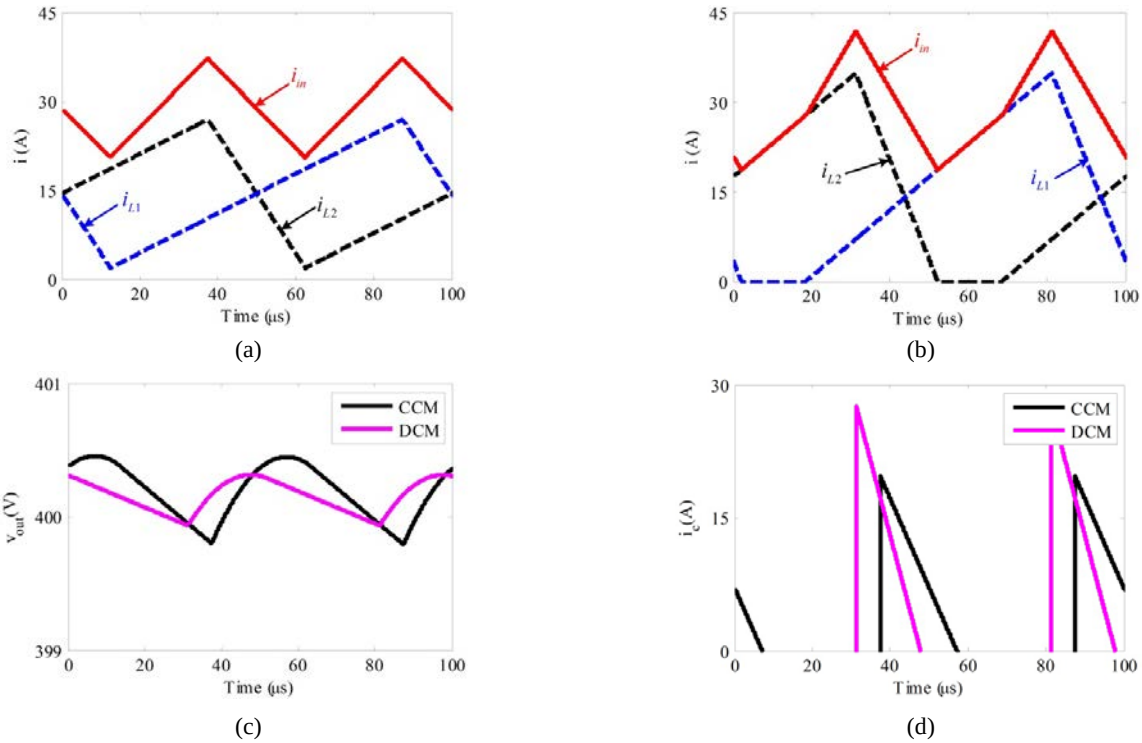


Fig. 7. Comparison of the simulated waveforms with CCM-II and DCM-III. (a) Simulated inductor current and input current waveforms with CCM-II; (b) Simulated inductor current and input current waveforms with DCM-III; (d) Comparison of the output voltage ripple; (e) Comparison of the output capacitor current.

TABLE III
VOLTAGE CONVERSION RATIO, MODE BOUNDARIES, AND INPUT CURRENT RIPPLES

Modes	d	ΔI_{in}	Boundaries
CCM-I	$\frac{1}{1-D}$	$\frac{D(1-2D)V_2}{L_s f_s}$	$D<0.5, P>\frac{D(1-D)(1-2D)V_2^2}{2L_s f_s}$
CCM-II		$\frac{(2D^3-5D^2+4D-1)V_2}{(1-D)L_s f_s}$	$D>0.5, P>\frac{(2D^3-5D^2+4D-1)V_2^2}{2L_s f_s}$
DCM-I	$\frac{\sqrt{4D^2k+1}}{2}+\frac{1}{2}$	$\frac{(2-d)DV_2}{dL_s f_s}$	$D<0.5, D<M<0.5$
DCM-II		$\frac{(1-2D)(d-1)V_2}{2dL_s f_s}$	$D<0.5, \mathrm{M}<D<0.25+0.5M$
DCM-III		$\frac{(d-2)DV_2}{(d-1)dL_s f_s}$	$D>0.5, \mathrm{M}<D<1-1/d$
DCM-IV		$\frac{(d-1-2D)V_2}{2(d-1)dL_s f_s}$	$D<0.5, D>M, \mathrm{D}>0.25+0.5\mathrm{M}$

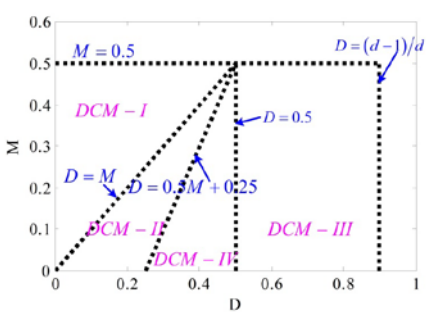


Fig. 8. Modes distribution with their boundary lines.

$$D+D/(d-1)=1 \quad (15)$$

$$D=1-1/d \quad (16)$$

The analytical expressions of the voltage conversion ratio and mode boundaries can be obtained and summarized in TABLE III.

Based on the boundaries analysis, the modes distributions with their boundaries are shown in Fig. 8. The boundary line with expression (16) is changing with the voltage conversion ratio d. Expression (1) indicates the relationship between D and M, which is valid for all DCMs. However, the variable

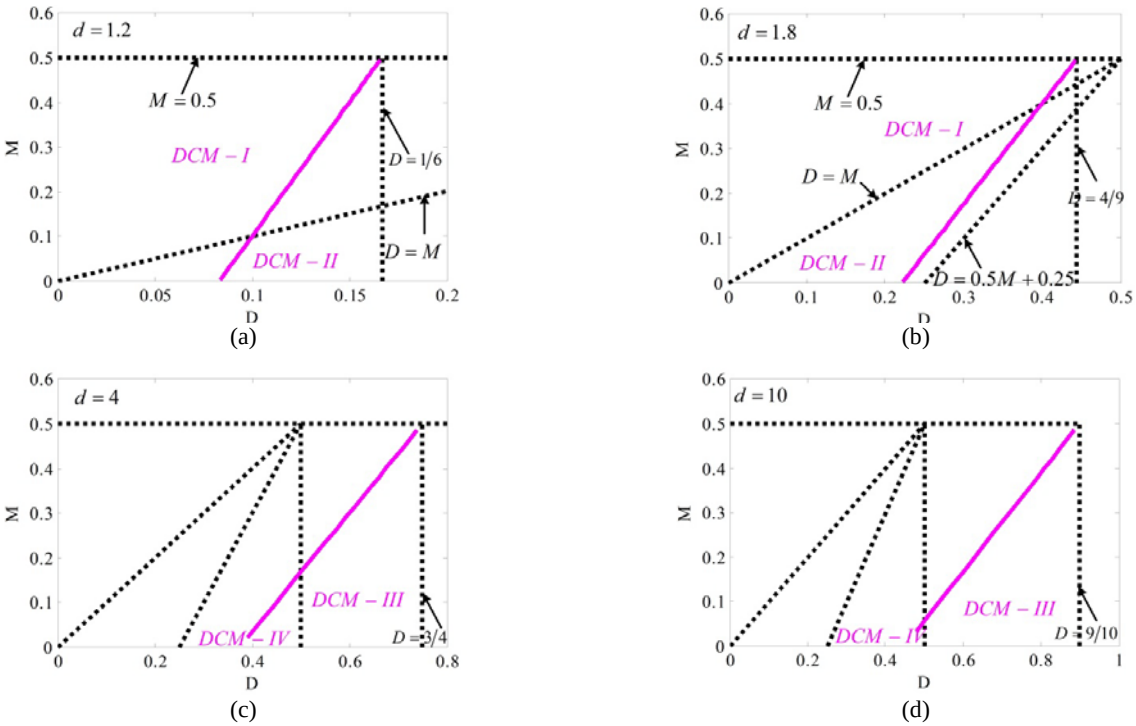


Fig. 9. Modes distribution for various voltage conversion ratios. (a) d=1.2; (b) d=1.5; (c) d=4; (d) d=10.

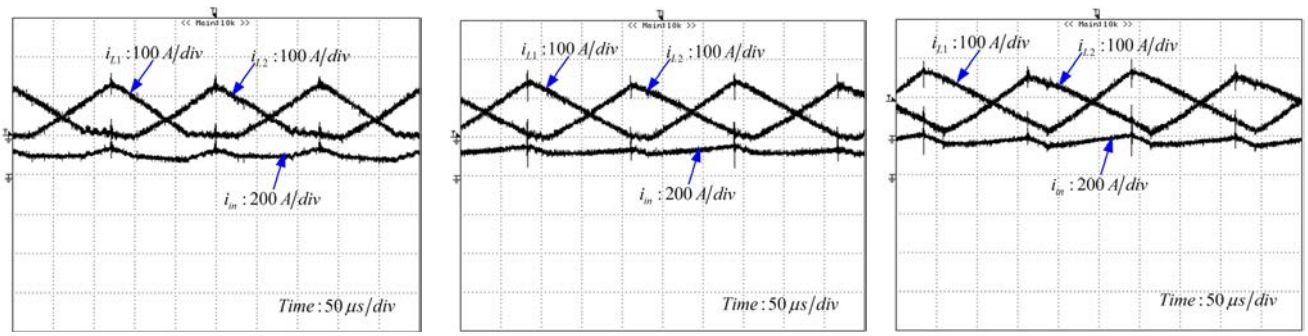


Fig. 10. Experimental waveforms of inductor current i_{L1} and i_{L2} and input current i_{in} with different operating modes: (a) DCM-II with P_o = 23 kW; (b) DCM-I with P_o = 38 kW; and (c) CCM with P_o = 57 kW.

pairs (D, M) are affected by d, the circuit parameters, and load conditions. Fig. 9 illustrates the mode distribution for various d. Two conclusions can be drawn from Fig. 9.

(1) DCM-I and DCM-II are valid for "$d \le 2$."The DCM-II distribution is wider for a higher d.

(2) DCM-III and DCM-IV are valid for "$d > 2$." The DCM-III distribution is wider when the voltage conversion ratio d is larger.

Fig. 10 shows the measured waveforms for the different operating modes. The inductor currents i_{L1} and i_{L2}, and input current i_{in} are illustrated and compared. The measured conditions are V_{out} = 520 V, V_{in} = 280 V to 320 V, f_s = 10 kHz, and L_s = 50 μH. The voltage conversion ratio is less than 2; thus, DCM-I and DCM-II are valid, as shown in Figs. 10(a) and (b), respectively. Their output power values are 23 kW and 38 kW, respectively. In the test, the duty-cycle ratios are tuned as 38% and 40%. With further increase of the output power, the converter is operating in CCM and the waveforms are shown in Fig. 10(c). The inductor current is always larger than zero at any instant. The experimental results verified the effectiveness of the previous theoretical analysis.

IV. Key Design Issues and Verification

A. Effects of Inductor Parasitic Resistance

Expressions (10) and (11) indicate that the DCM output voltage is determined by both duty-cycle D and circuit parameters k. However, each inductor inevitably has the parasitic resistance r_i (i = 1, 2); thus, the output voltage is also affected. Fig. 6 shows that the state space equations are derived from the equivalent circuits. The IBC steady-state characteristic is expressed as:

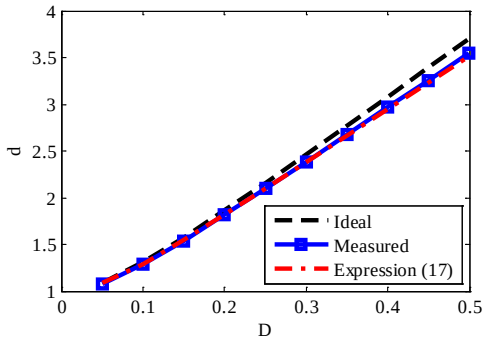


Fig. 11. Comparison of the theoretical and experimental results of *d* versus *D*.

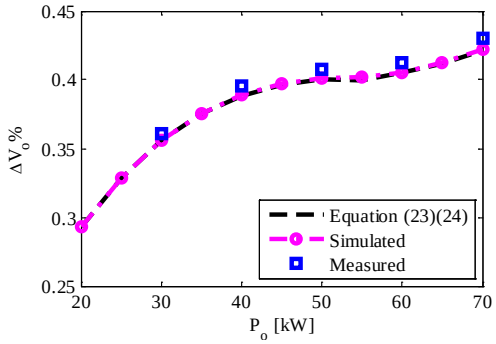
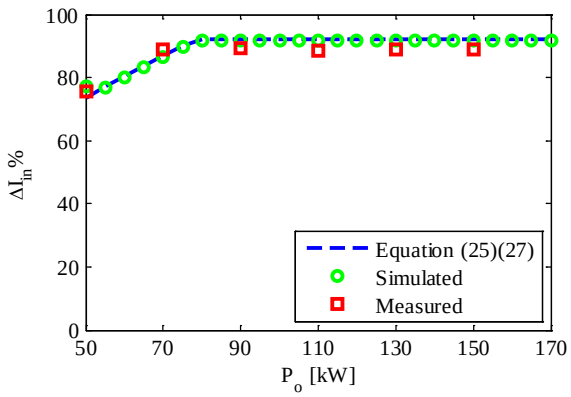
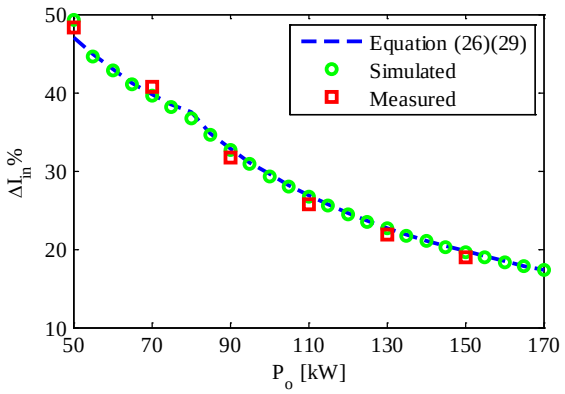


Fig. 12. Output voltage ripples versus output power.



(a)



(b)

Fig. 13. Input current ripple. (a) Absolute input current versus output power. (b) Input current ripple versus output power.

$$d_{DCM\_r_i} = \frac{RD_P\left(D+D_P\right)\left(r_1+r_2\right)}{RD_P^2\left(r_1+r_2\right)+\left(D+D_P\right)r_1r_2} \tag{17}$$

where D_p represents the falling time of the inductor current and is expressed as

$$D_P = \frac{1+\sqrt{1+4D^2k}}{2Dk} \tag{18}$$

Fig. 11 shows the comparison of the theoretical and experimental measured output voltage ratio *d* versus the duty-cycle *D* under the condition of "*k* = 40." The black dotted line represents the ideal voltage conversion ratio. The red dashed line represents the derived *d* by using expression (17). The experimental results are shown with the blue line with square symbol. Fig. 11 indicates that the experimental measured *d* is consistent with expression (17). Compared with the ideal result, discrepancy is noted, which is mainly caused by the parasitic resistance of IBC.

B. Output Voltage Ripple

The output voltage ripple is determined by the current flowing through the output capacitor i_C, which is the combination of the current i_B and the load current i_o. Fig. 5 illustrates the typical current waveform of i_C with DCM-II, which is negative during interval ΔT, and positive during other intervals. Fig. 5 shows that the capacitor current meets the following expression:

$$i_{L2}\left(\delta_2\right) - \frac{\left(d-1\right)V_2}{dL}\Delta T = I_o \tag{19}$$

Thus,

$$\Delta T = \frac{dL\left(i_{L2}\left(\delta_2\right)-I_o\right)}{\left(d-1\right)V_2} \tag{20}$$

The output voltage ripple is derived as

$$\Delta V_o = \frac{1}{C_o}\int_0^{\Delta T}\left(i_{L2}\left(\delta_2\right)-I_o\right)dt = \frac{\Delta T}{2C_o}\left(i_{L2}\left(\delta_2\right)-I_o\right) \tag{21}$$

$$\Delta V_o\,\% = \frac{\Delta V_{C_o}}{V_2} = \frac{\Delta T}{2V_2C_o}\left(i_{L2}\left(\delta_2\right)-I_o\right) \tag{22}$$

For DCM-II, the output voltage ripples can be derived and expressed as

$$\Delta V_o\,\%_{Mode\_II} = \frac{\left(RD-dL_sf_s\right)^2}{2d\left(d-1\right)R^2f_s^2C_oL_s} \tag{23}$$

Similarly, the output voltage ripples with DCM-I can be derived as

$$\Delta V_o\,\%_{Mode\_I} = \frac{\left(R-dR+2RD-2dL_sf_s\right)^2}{8d\left(d-1\right)R^2f_s^2C_oL_s} \tag{24}$$

Fig. 12 shows the comparison of calculated input current ripple with simulated and experimental measured results when "V_1 = 320 V, V_2 = 520 V, and C_o = 600 μF." Fig. 12 indicates that the expressions derived for the input current ripple are correct regardless of the operating mode. The output power boundary for DCM-I and DCM-II is P_o = 55

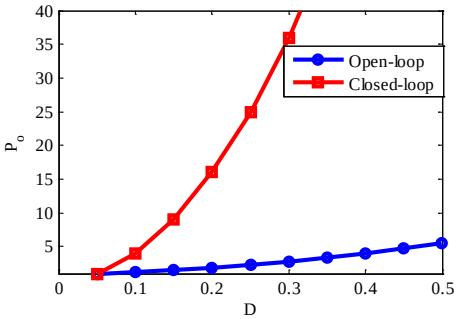


Fig. 14. Comparison of the output power versus D for the open-loop and closed-loop controls.

kW. The inductance in this design is set at 50 μH because the DCM modes are used for the low-power region. The simulation and experimental results indicate that the output voltage ripple ratio is well-regulated within 1%. If only CCMs are used, then the inductance should reach 300 μH. Thus, the hybrid mode shows significant advantages in both keeping low output voltage ripples and improving power density.

C. Input Current Ripple

Based on the input current expressions presented in TABLE II, the input current ripple with CCM-I is expressed as

$$\Delta I_{in\_CCM\_I} = \frac{D(1-2D)V_2}{L_s f_s} \tag{25}$$

$$\Delta I_{in\_CCM\_I}\% = \frac{\Delta I_{in\_CCM\_I}}{I_{in\_CCM\_I}} = \frac{D(1-D)(1-2D)V_2^2}{PL_s f_s} = \frac{D(1-D)(1-2D)R}{L_s f_s} = kD(1-D)(1-2D) \tag{26}$$

The input current ripple with DCM-I is expressed as

$$\Delta I_{in\_DCM\_I} = \frac{D(2-d)V_2}{dL_s f_s} \tag{27}$$

The average input current with DCM-I is obtained by

$$I_{in\_DCM\_I} = \left[i_L(0)+i_L(\delta_1)\right]D + \left[i_L(\delta_1)+i_L(\delta_2)\right](M-D) + \left[i_L(\delta_2)+i_L(0)\right](0.5-M) = \frac{D^2V_2}{(d-1)L_s f_s} \tag{28}$$

Thus,

$$\Delta I_{in\_DCM\_I}\% = \frac{\Delta I_{in\_DCM\_I}}{I_{in\_DCM\_I}} = \frac{(d-1)(2-d)}{Dd} \tag{29}$$

Fig. 13 shows the comparison of the calculated input current ripple with simulated and experimental measured results when "V_1 = 320 V and V_2 = 520 V." Fig. 13 indicates that the expressions derived for the input current ripple are valid for all operating modes. The input ripple ratio for the rated power 150 kW is also well-regulated within 20%.

D. Output Power

With DCM, the average output power of IBC can be expressed as

$$P_o = \frac{V_1^2}{L_s f_s k}\left(\frac{\sqrt{4D^2k+1}}{2}+\frac{1}{2}\right)^2 \tag{30}$$

For the voltage close-loop operation, the voltage conversion ratio d is constant. The load resistance R is decreased with an increasing D to obtain an increased output power. With open-loop operation, for a given V_1 and R, V_o and P_o will increase with D based on (17) and (30). Fig. 14 shows the relationship of the output power with duty-cycle D for both the open-loop and voltage closed-loop operations. Their base values are the output power values under the condition of "D = 0.05." Fig. 14 indicates that the output power will be increased with D for both the open-loop and closed-loop operations. However, with the closed-loop control, the changing speed of the output power is faster than that with the open-loop control.

E. SOA Design

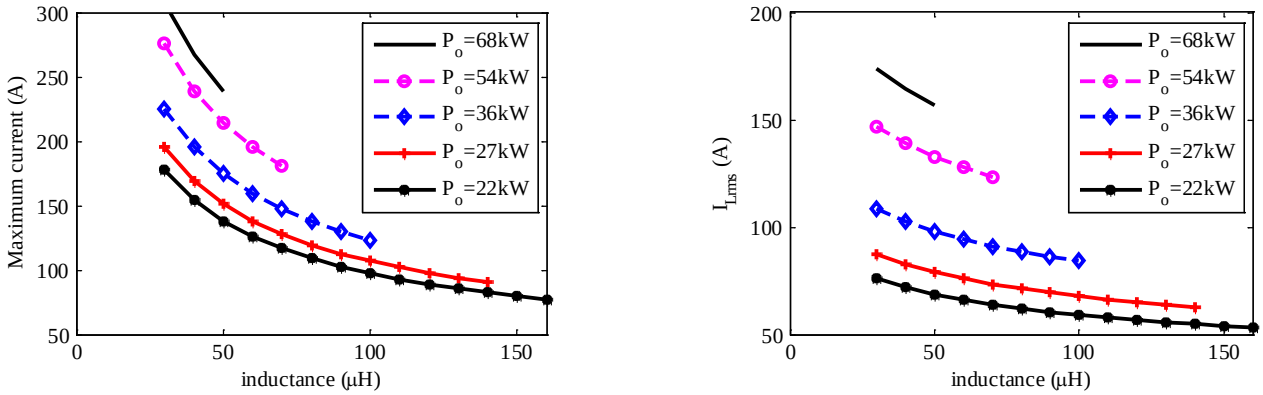
Figs. 4 and 5 show the dynamics of the current. Thus, the inductor peak current i_{Lpeak} in a switching period can be determined. For CCM, DCM-I, and DCM-III, i_{Lpeak} corresponds to $i_L(\delta_1)$; for the other modes, i_{Lpeak} corresponds to $i_L(\delta_2)$. The inductor rms current in a switching period I_{rms} can be expressed as:

$$I_{Lrms}^2 = \frac{1}{2}\left[i_L(\delta_1)\right]^2(D+D_P) = \frac{1}{2}\left[\frac{DV_2}{dL_s f_s}\right]^2\left(D+\frac{D}{d-1}\right) = \frac{D^3V_2^2}{2d(d-1)L_s^2 f_s^2} \tag{31}$$

Fig. 15 shows the inductor peak current i_{Lpeak} and inductor rms current i_{Lrms} of IBC as a function of L_s. IGBTs are used as the main power device; thus, the switching frequency is set at 10 kHz. Fig. 15 shows that both i_{Lpeak} and i_{Lrms} are decreased with the inductance. The inductance determines the output power range. Fig. 15 shows the maximum output power with "L_s = 100 μH" is 36 kW, while the maximum output power is 68 kW when "L_s = 50μH." The comparison results shown in Fig. 7 indicate that the inductance will be significantly reduced by using DCM instead of CCM for the same output power. The reduction of inductance is beneficial for the size reduction and power density improvement. In this design, a hybrid mode is adopted, which considers the entire power range. DCM is used for the low-power region and CCM is adopted for the high-power region. The boundary for DCM and CCM is set at close to "P_o = 70 kW."

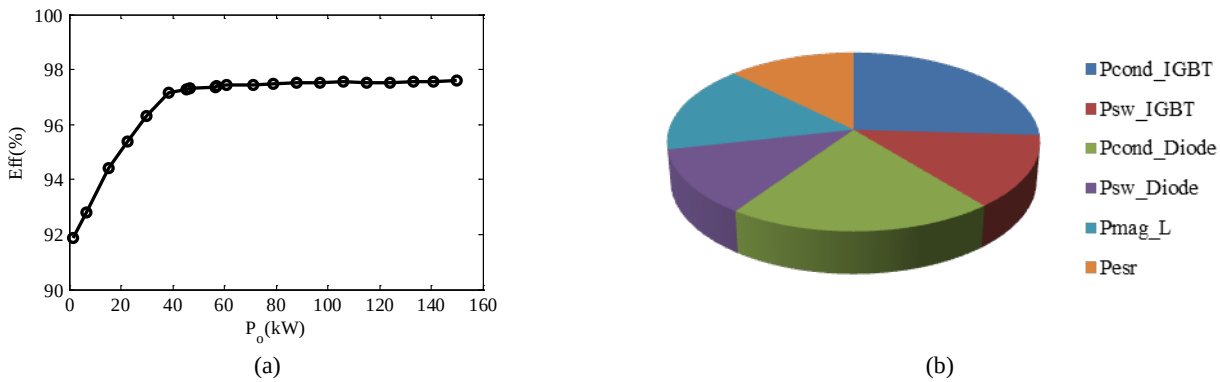
F. Efficiency

Fig 16(a) is the system efficiency curve, which indicates that the entire efficiency is approximately between 95% and 98%; the efficiency is over 97% when the output power is larger than half of the rated power. Fig. 16(b) shows the estimated power loss distribution of the prototype with P_o = 20 kW using the proposed hybrid mode for IBC. DCM is used for the low-power region and CCM is used for the



(a) (b)

Fig. 15 SOA design of IBC with DCM. (a) Relationship of the inductor peak current i_{Lpeak} with L_s; (b) Relationship of the inductor rms current i_{Lrms} with L_s.



(a) (b)

Fig. 16 System efficiency curve and power loss breakdown distribution. (a) System efficiency curve; (b) power loss distribution.

high-power region. The main power losses include the IGBT conduction loss P_{cond_IGBT}, IGBT switching losses P_{sw_IGBT}, diode conduction loss P_{cond_Diode}, IGBT switching losses P_{sw_diode}, losses of inductor P_{mag_L}, and other losses, including the parasitic resistor losses. By using DCM, both the turn-on switching loss of IGBTs and the reverse recovery loss of the diodes can be eliminated. Thus, the efficiency of IBC for the low-power region can be improved from 90% to close to 92%.

V. Conclusion

This study presents the operation, design, and performance characteristics of a multi-mode two-phase IBC for FCEV applications. Different modes, including two CCMs and four DCMs, are discussed with their equivalent circuits. Four criteria to determine the mode distribution are also discussed. The mode distributions for various d are illustrated and verified with the experimental results. The effects of the inductor parasitic resistance in the voltage conversion ratio and mode boundaries are analyzed. The safe operational area is analyzed through a comparison of the different operation modes. The output voltage and power characteristics with the open-loop or closed-loop operations are discussed. A hybrid mode is adopted in this design. DCM is used for the low-power region and CCM is adopted for the high-power region. The input inductance is reduced from 300 uH to 50 uH. The input ripple ratio for the rated power 150 kW is well-regulated within 20% and the output voltage ripple ratio is well-regulated within 1%. The system efficiency curve indicates that the entire efficiency is approximately between 95% and 98%; the rated efficiency is over 97%.

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