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Design of High-Speed Comparators for High-Speed Automatic Test Equipment

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** Short Paper*

***Abstract*:** This paper describes the design of a high-speed comparator for high-speed automatic test equipment (ATE). The normal comparator block, which compares the detected signal from the device under test (DUT) to the reference signal from an internal digital-to-analog converter (DAC), is composed of a rail-to-rail first pre-amplifier, a hysteresis amplifier, and a third pre-amplifier and latch for high-speed operation. The proposed continuous comparator handles high-frequency signals up to 800MHz and a wide range of input signals (0~5V). Also, to compare the differences of both common signals and differential signals between two DUTs, the proposed differential mode comparator exploits one differential difference amplifier (DDA) as a pre-amplifier in the comparator, while a conventional differential comparator uses three op-amps as a pre-amplifier. The chip was implemented with 0.18μm Bipolar CMOS DEMOS (BCDMOS) technology, can compare signal differences of 5mV, and operates in a frequency range up to 800MHz. The chip area is 0.514mm^2.

***Keywords*:** ATE, High-speed continuous comparator, Hysteresis, Differential difference amplifier

1. Introduction

For testing and characterizing an application processor (AP) and a system on chip (SoC), the pin card in high-speed automatic test equipment (ATE) includes a driver integrated circuit (IC) to force the signal to the device under test (DUT) and to detect the signal from the DUT. In the driver IC, a parametric measurement unit (PMU), a digital-to-analog converter (DAC), comparators, an active load and serial peripheral interface (SPI) memory resistors are included [1], [2]. This paper describes new techniques in designing a high-speed comparator for this driver IC in ATE with Bipolar CMOS DEMOS (BCDMOS) technology.

The comparator compares the detected signal values from the DUTs to the output of the DAC, which are the reference values. The comparator must be able to handle a wide input signal range (0V to 5V) and operate with an input signal up to 800MHz. Also, it should have sufficient accuracy to compare a signal difference of 5mV. Moreover, considering unexpected noise, the comparator must have a hysteresis function. The implementation of a high-speed comparator with 0.18μm BCDMOS technology is challenging work because BCDMOS devices have large parasitic capacitors and greater resistance.

2. Architecture of the Comparator

A block diagram of the high-speed comparator is depicted in Fig. 1. This comparator is continuous, so it

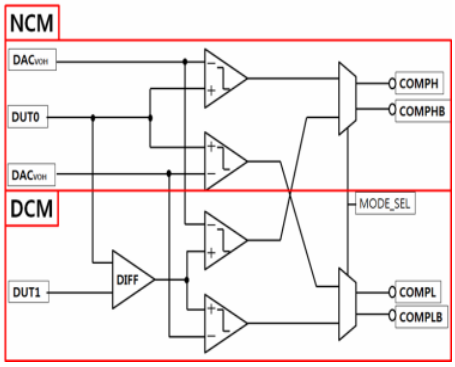

Fig. 1. Block diagram of the comparator.

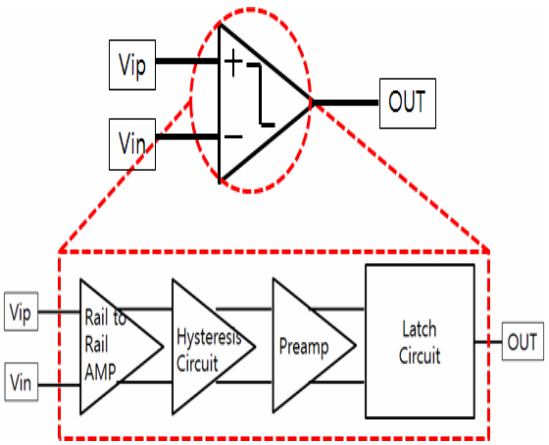

Fig. 2. Block diagram of continuous comparator.

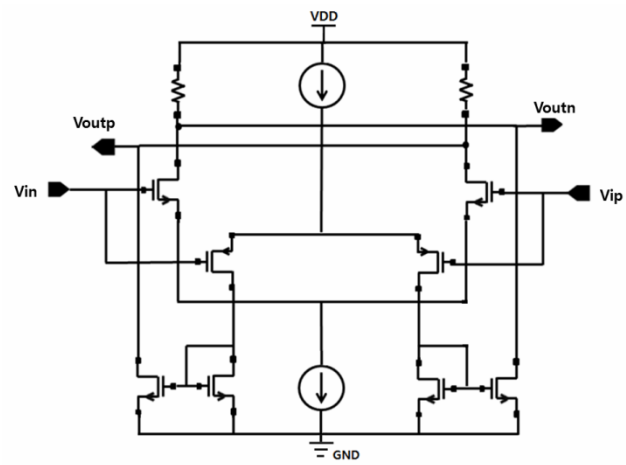

Fig. 3. First stage rail-to-rail pre-amplifier.

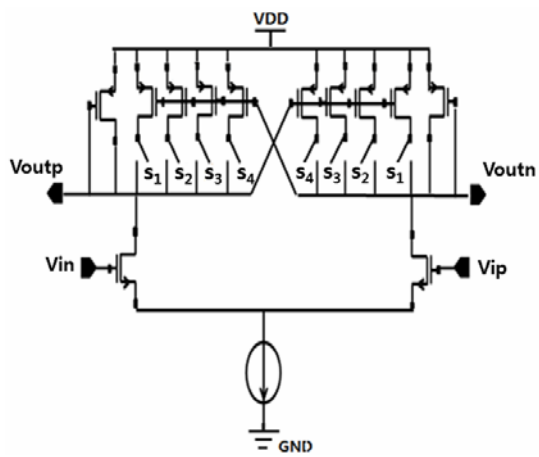

Fig. 4. Second pre-amplifier with hysteresis function.

does not need a clock signal. This comparator has two operating modes. The first mode is normal comparator mode (NCM), which compares the detected values from the DUT (DUT0) to the output of the DAC reference values (DAC_{VOH}, DAC_{VOL}).

The second mode is differential comparator mode (DCM), which also compares the difference of both common mode signals and differential signals from the two DUTs (DUT0, DUT1) to the output of the DAC reference signals (DAC_{VOH}, DAC_{VOL}). Decided results from comparators are transferred to the control blocks through the high-speed driver circuits.

3. The Proposed Comparator Design

3.1 High Speed Comparator in Normal Mode

Fig. 2 shows the proposed block diagram of the high-speed continuous comparator. For high accuracy and high-speed operation with BCDMOS technology, three cascode stages of a pre-amplifier and a latch are considered.

The first stage pre-amplifier is the rail-to-rail amplifier to deal with the wide input range of 0V to 5V. And then, the second stage amplifier has hysteresis circuits controlled from 2b SPI signals. Finally, the high-speed third pre-amplifier and latch are designed to accomplish high-speed and high-accuracy requirements.

Fig. 3 shows the first stage rail-to-rail pre-amplifier for accepting the wide range of input signals (0V to 5V). Because the active load devices in BCDMOS technology have large parasitic capacitors and large output resistances, small passive resistances instead of active loads are used for high-bandwidth operation.

The second pre-amplifier with the hysteresis function is shown in Fig. 4 [3]. This hysteresis circuit provides hysteresis voltages in a continuous comparator to overcome unexpected noise. Hysteresis can be achieved with the difference of device ratios between the diode-connected active transistors and switch-controlled active transistors. The 2b signals from the SPI resister can control the S_1, S_2, S_3 and S_4 switches and achieves hysteresis of four-step voltages from a minimum 0mV to a maximum 96mV. The relation between the hysteresis voltage and device size of switch-connected PMOSFET (PMOS) transistors is shown in Eq. (1).

$$V_{hys} = \left(1-\sqrt{M}\right)\sqrt{\frac{2I}{(1+M)\mu_n C_{ox}(\frac{W}{L})}} \qquad (1)$$

M is the device ratio between the diode-connected active transistors and switch-controlled active transistors. I is the tail current of the second pre-amplifier.

Figs. 5 and 6 show the third pre-amplifier and latch, respectively. A fully differential third pre-amplifier exploits simple common mode feedback (CMFB) with two resisters to stabilize the output common mode voltage. The latch is composed of two inverters, which are connected to each other forming positive feedback. Inverter chains are added to clarify the high or low output level with minimum delay.

3.2 Comparator in Differential Mode

To implement DMC mode, a differential difference amplifier (DDA)[4] is used, as shown in Fig. 7, as a pre-

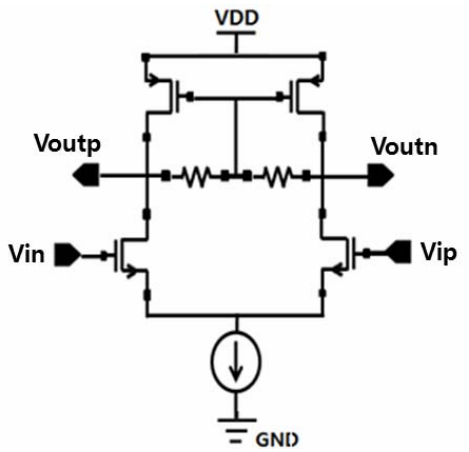

Fig. 5. Third pre-amplifier.

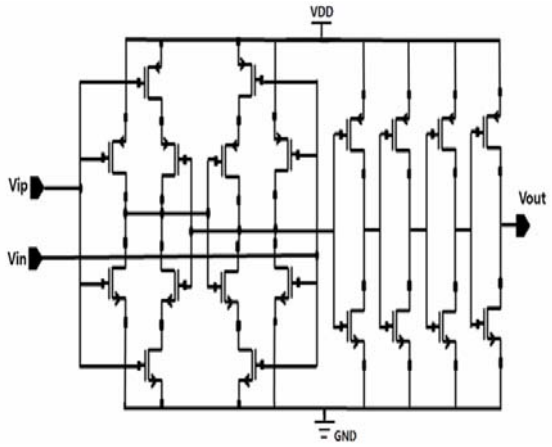

Fig. 6. Latch with inverter chain.

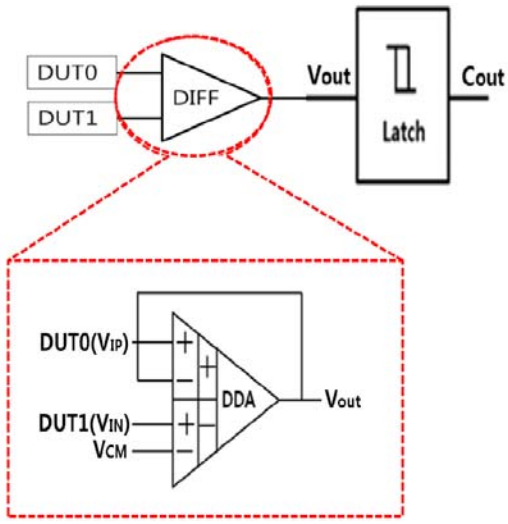

Fig. 7. Block Diagram of the DDA.

amplifier.

Conventional design of the DMC needs three amplifiers, one for differential signal generation, another for common mode signal generation, and the final one for summing these two signals. But if we use a DDA, only one DDA

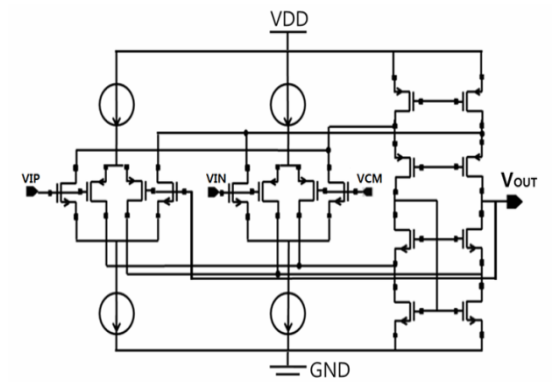

Fig. 8. The Circuits of DDA.

amplifier is enough for processing all differences in common mode signals and the difference in differential mode signals. Since the proposed DMC uses one op-amp, it does not suffer from mismatches, the cumulated offsets and the noise of many op-amps. Moreover, the proposed DMC consumes less power and requires less hardware area, and hence, offers low-cost implementation.

Fig. 8 shows a transistor-level schematic diagram of the DDA. For high gain, a folded cascode structure was used. This folded cascode structure inherently guarantees stable high-frequency operation and does not require additional compensation capacitors. The input stage is designed for rail-to-rail operation by paralleling the PMOS input pair and the NMOSFET (NMOS) input pair.

The output voltage, VOUT, includes both the difference of common mode signals and the difference of differential signals from DUT0 (VIP) and DUT1 (VIN), as expressed in Eq. (2):

$$\begin{aligned} V_{OUT} &= V_{IP} - V_{IN} + V_{CM} \\ &= (V_{p.di} - V_{n,di}) + (V_{p,cm} - V_{n,cm}) + V_{CM} \end{aligned} \quad (2)$$

4. Simulated and Measured Results

The proposed comparator was implemented with 0.18μm BCDMOS technology. The layout size of the proposed comparator is 620μm x 830μm, as shown in Fig. 9. There are four continuous comparators without clock signals, a DDA and two output stages. All the supply voltages in comparators are 5V. The first rail-to-rail pre-amplifier has a gain of 10dB, and a unit gain frequency of 2.5GHz, while the third pre-amplifier has a gain of 14dB and a unit gain frequency of 1.53GHz.

Fig. 10 shows the simulation results of normal mode continuous comparators. The proposed comparator can compare a difference of 5mV at a frequency of 800MHz.

Fig. 11 shows the simulation results of hysteresis voltages. Hysteresis voltages such as 0mV, 37.9mV, 68mV and 96mV are achieved according to the codes 00, 01, 10 and 11, respectively.

The AC simulation results of the DDA in DMC mode are shown in Fig. 12. The gain is 32dB, and the unity gain frequency is 1.33GHz. Phase margin is 65°.

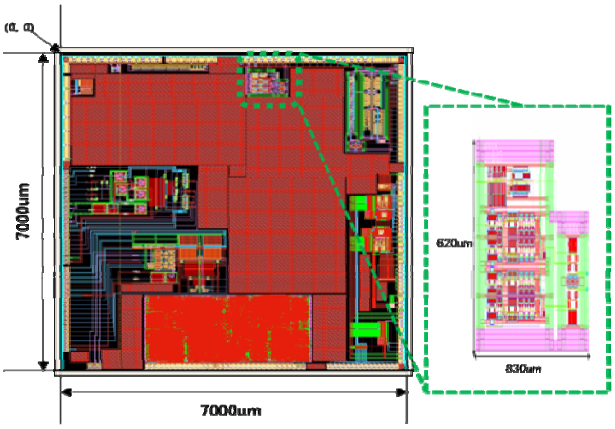

Fig. 9. Comparator Layout (0.5146mm^2).

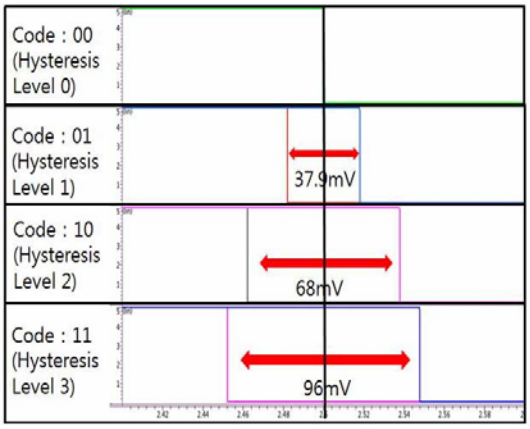

Fig. 11. Simulation results of hysteresis.

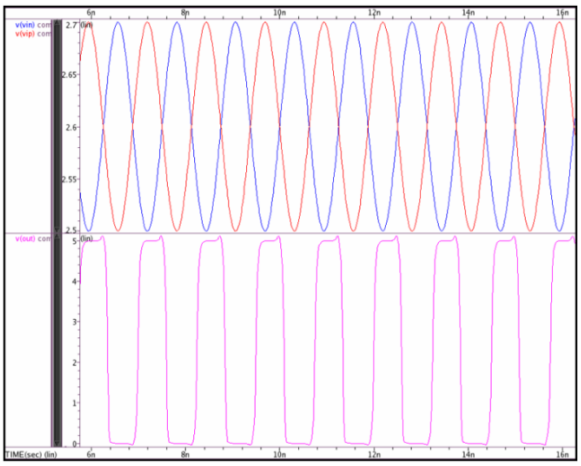

Fig. 10. Transient simulation results of comparator.

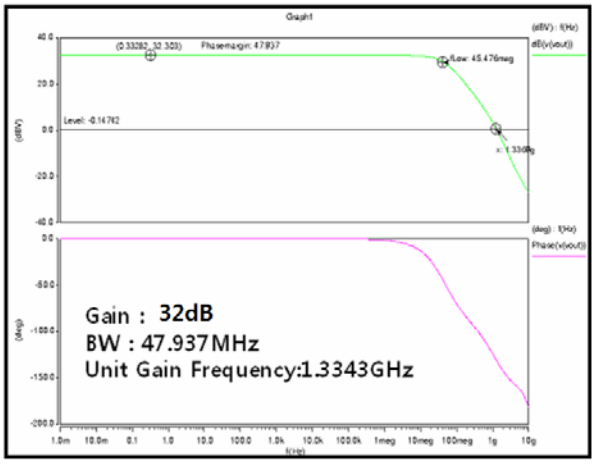

Fig. 12. AC simulation results of DDA.

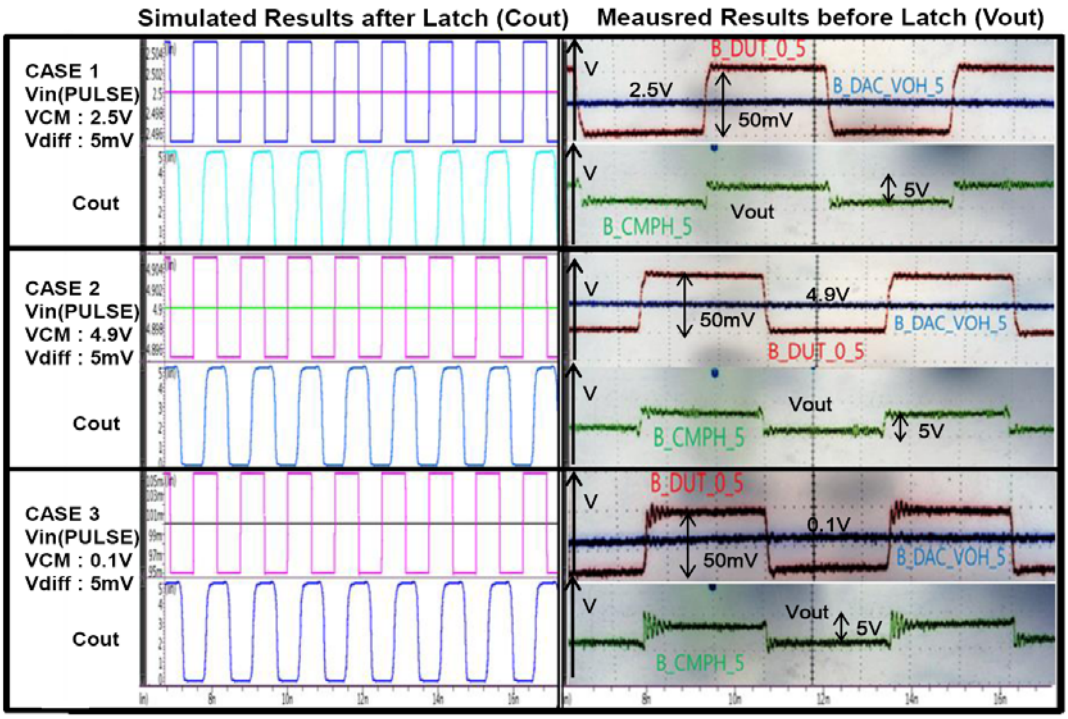

Fig. 13. Simulated and measured results of normal comparator.

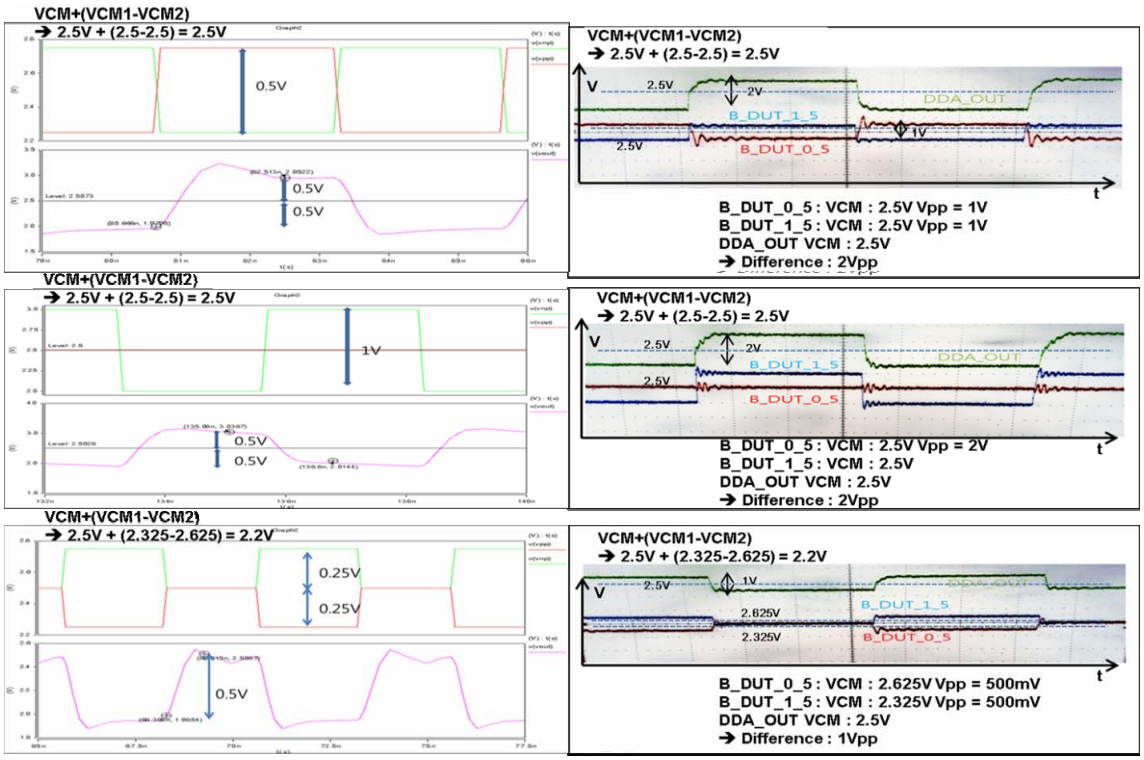

Fig. 14. Simulated & measured results of DDA (Vout).

Table 1. Performance Comparison.

	This Work	[2]
Process	0.18μm BCDMOS	BiCMOS
Supply Voltage	5V	5V
Input Range	0 ~ 5V	0 ~ 5V
Maximum Input Freq.	800MHz	1.2GHz
Hysteresis (00 ~ 11)	0mV ~ 96mV	0mV ~ 100mV
Power Consumption	300mW	1.1W (per channel)
Resolution	5mV	N/A
Chip Area (w/o pad)	620μm × 830μm	N/A

Fig. 13 shows the simulated results of the proposed continuous comparator on the left side and the measured results of the proposed continuous comparator on the right side. To verify the wide range of operation, the difference voltage of 5mV from the common mode voltage of 2.5V, 4.9V and 0.1V were tested. And the outputs of the comparator were correctly detected with high or low levels, as shown in Fig. 13 at a signal frequency of 800MHz.

Fig. 14 shows the simulated results of the proposed DDA on the left side and also the measured results of the proposed DDA on the right side. As shown in Fig. 14, the differences in the common mode voltages and the difference in differential mode voltages are measured correctly. Three cases of input signals are tested to prove correct operation of the DDA. For simulated results on the left side, there are two input signals on the top, and the simulated output of the comparator is on the bottom, while for measured results on the right side, two input signals are shown on the bottom.

The performance summary of this comparator is in Table 1.

5. Conclusion

This paper describes how to design a high-speed comparator in a driver IC for automatic test equipment with BCDMOS technology. To accept a wide input range of signals from 0V to 5V and to handle a frequency range up to 800MHz, a cascode amplifier structure for a continuous comparator is proposed. Also, to measure the difference in output signals between the two DUTs, a DDA is exploited with minimum hardware, with less power consumption and with lower noise to detect the differences of both common mode signals and differential signals.

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