

An Efficient FPGA based Real-Time Implementation Shunt Active Power Filter for Current Harmonic Elimination and Reactive Power Compensation

Charles S[†] and Vivekanandan C^{*}

Abstract – This paper proposes a new approach of Field Programmable Gate Array (FPGA) controlled digital implementation of shunt active power filter (SAPF) under steady state and dynamic operations. Typical implementations of SAPF uses microprocessor and digital signal processor (DSP) but it limited for complex algorithm structure, absence of feedback loop delays and their cost can be exceed the benefit they bring. In this paper, the hardware resources of an FPGA are configured and implemented in order to overcome conventional microcontroller or digital signal processor implementations. This proposed FPGA digital implementation scheme has very less execution time and boosts the overall performance of the system. The FPGA controller integrates the entire control algorithm of an SAPF, including synchronous reference frame transformation, phase locked loop, low pass filter and inverter current controller etc. All these required algorithms are implemented with a single all-on chip FPGA module which provides freedom to reconfigure for any other applications. The entire algorithm is coded, processed and simulated using Xilinx 12.1 ISE suite to estimate the advantages of the proposed system. The coded algorithm is also defused on a single all-on-chip Xilinx Spartan 3A DSP-XC3SD1800 laboratory prototype and experimental results thus obtained match with simulated counterparts under the dynamic state and steady state operating conditions.

Keywords: Digital control, Shunt active power filter, Field programmable gate array, Harmonic elimination, Reactive power compensation, Synchronous reference frame transformation

1. Introduction

Now a days, electric power quality is an essential issue in the transmission, distribution and utilization of electric energy. Improvements in power quality lead to reduction in electric power and production losses and a significant improvement in quality of industrial products. Although the reactive power is not direct power quality parameter, it will indirectly affect the quality of electrical power and causes the extra losses in the transmission and distribution systems. Therefore the reactive power in overhead lines and feeders should be kept under control. In response to the power quality concerns the utilities and the operators have published grid codes, regulations, and IEEE 519 and EN 50160 standards to ensure the quality of the electric power in transmission and distribution systems. Therefore the industrial and commercial customers pay their attention predominantly in power factor correction and reactive power compensation by installing the usually shunt passive filter. However, they are often large, heavy and it is not suitable for fast changing loads.

To cope with these problems, the implementation shunt active power filter (SAPF) have emerged as solutions for harmonic damping throughout and reactive power compensation a power distribution lines has been proposed in the literature [1-3]. A significant part of this kind of applications is the control stage of power converters and current controller, which is indispensable for the proper operation of such equipment. In effect, important research works in this field have been focused on improved hardware to implement the digital controllers [4-6]. This work mainly deals with the FPGA digital implementation of SAPF controllers, which is an important part of industrial control systems. The design considerations and equivalent results presented in this paper can be also applied for any power electronic applications as it operates at medium and high frequency applications.

Recently many research works have been have been implemented the digital version of SAPF for current harmonics elimination and reactive power demand using digital signal processing (DSPs) and microcontroller unit [7-10], Nevertheless, DSPs or microcontroller face the fundamental challenges such as large execution time [11], adaptability, less accuracy, absence of feedback loop delays, limited complex algorithm structures and cost and limited sampling period [12-13]. The main constraints of DSPs are serial processing of the control algorithm to be implemented

[†] Corresponding Author: Dept. of Electrical and Electronic Engineering, Sri Shakthi Institute of Engineering and Technology, Tamilnadu, India. (charles.siluvaimuthu@gmail.com)

^{*} Dean, Dept. of Electrical and Electronic Engineering, S.N.S College of Engineering, Tamilnadu, India. (vp.snsce@gmail.com)

Received: May 9, 2014; Accepted: April 6, 2015

and, as a consequence, the limitation of the performance in terms of throughputs and achievable bandwidth. An important component of SAPF is the current controller, which has the task of making the controlled current tracking its respective reference. Also current controller requires relatively faster sampling rate and computation update rate, typically in microseconds, to sustain the closed-loop bandwidth, to increase the accuracy in sensing the voltage and current, parameter estimation and to provide high-frequency pulse width modulation. The processing speed needed to deal with these tasks is in the order of microseconds, which makes it difficult to implement within a DSPs or microcontroller software computation environment [14-15].

FPGAs [16] basically contain an array of logic elements or cells (each cell containing look-up tables and registers), whose interconnections are decided by the contents of a random access memory (RAM). The FPGA design, typically using hardware description languages, decides the final circuit structure to achieve a desired functionality and it is therefore said to be hardware programmable. Besides a large number of configurable input/output blocks, FPGAs also typically contain additional optimized RAM blocks and multipliers to increase the performance of the device. Logic, adders subtractors, comparators, multipliers and special functions are easy to implement in these typical FPGAs. Special functions are implemented using look-up tables in RAM blocks. However, RAM size increases exponentially with the resolution of the input variables. The hardware programmability of FPGAs allows both the concurrent or parallel processing of data and pipelining, which may dramatically reduce the required processing time and increase the number of computations per switching cycle, compared to microcontrollers and DSPs. Additionally, in cases where the implementation of the desired control benefits from the use of a CPU, this can be embedded within the FPGA through the programming of the corresponding circuit. FPGA allows the development of well-adapted control architecture with fast circuit modification and rapid prototyping through hardware description language [17-18]. This tremendous uniqueness of FPGA easily handles the high speed challenging algorithms in different control functions of SAPF in single all-on-chip integration [19-20]. Given the powerful and fast FPGA digital controllers today, have been already used in many different industrial applications such as, high switching frequency DC/AC inverters [21], AC drive applications [22], three phase inverter [23], induction machine [24], and DSTATCOM [25] have been implemented with FPGAs.

Due to the FPGA in-built advantages and expected future improvements, the authors forecast a progressive trend towards a full closed-loop SAPF digital control implementation within a single all-on-chip FPGA. In addition to performance improvements, this also boost the performance of the current controller with less execution time, saves costs and avoids the cumbersome synchronization

and communication between microcontroller or DSP and the FPGA. Therefore, a full FPGA based digital implementation of three phase SAPF controller concluded to be the best choice. The authors final goal is developed a digital control of SAPF using FPGA technology in order to boost the performance of current controller. The FPGA realization is to validate the synchronous reference frame theory (SRF), fundamental current extraction, phase locked loop (PLL), low pass filter (LPFs), digital hysteresis current controller and to design and implement the entire control algorithm in a single all-on-chip FPGA having dedicated hardware architecture with low computational overhead. The proposed system has been implemented using a single all on chip Xilinx Spartan 3A DSP – XC3SD1800 FPGA laboratory prototype under the steady state and dynamic conditions. The results show the practicability of the proposed implementation scheme in executing the algorithms at relatively faster execution time to compare with the existing system. Also the high dynamic performance of SAPF is satisfactory under the very less execution time.

The paper is organized as follows, Section II reviews the system configuration and operating principle of SAPF. Section III presents the suitable algorithm for harmonic extraction from which the FPGA implementation can be discussed. Section IV reviews the FPGA description and design methodology. Section V explains the FPGA implementation structure and relevant design details to obtain an efficient controller. In Section VI, simulation and experimental results are compared to verify the good performance of the designed modulator under different operating conditions. Finally, Section VII presents the conclusions.

2. System Configuration and Operating Principle

The schematic of the SAPF under consideration is shown in Fig. 1. The proposed system comprises of a three-phase SAPF, connected to the grid with a nonlinear load. An IGBT based three phase VSI with a DC link capacitance acts as SAPF. This SAPF generate currents that are equal and opposite to that of the harmonic currents.

The AC side of the VSI is connected through the

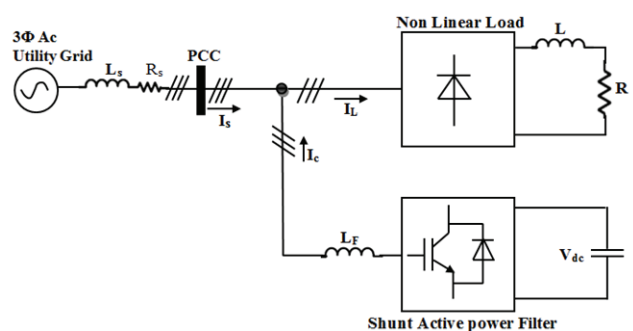


Fig. 1. Basic schematic of shunt active power filter

series inductance with resistance at PCC. A three-phase uncontrolled diode rectifier, feeding RL load, acts as nonlinear load. The compensation current that has to be supplied by SAPF, which decides the effectiveness of the SAPF and vital in controlling the switching of IGBTs in VSI, is determined by SRF transformation. On the basis of current references, digital hysteresis current controllers are employed to generate the PWM pulses to the IGBTs through the gating signals.

The proposed SAPF system consists of the following basic blocks.

- i) **Distortion detection:** A harmonic and reactive-power current identifier that detects the distorted components from the load currents $i_{Labc} = [i_{La} \ i_{Lb} \ i_{Lc}]^T$ and forms the reference current of VSI.
- ii) **PLL:** A voltage phase synchronizer based on Phase Locked Loop (PLL) technology that identifies the instantaneous phase transformation synchronized with utility voltage.
- iii) **Digital current control:** Hysteresis current controller that ensures that the VSI output currents i_c can track in accordance with the reference current rapidly and accurately.
- iv) **Inverter module:** This module that injects the current which is equal and opposite to that of distorted components of the load currents. In addition, the DC capacitor acts as the voltage source for the converter.

3. Control Scheme

The proposed SAPF system, based on the SRF transformation, uses minimum computational steps and simple circuits. This system is applied to improve the power quality by eliminating harmonics when distorted and asymmetrical AC source supplying nonlinear balanced loads. In addition, for harmonic compensation, the system is so

designed to meet the reactive power requirements of the load and to maintain the unity power in a three phase system with different source and load conditions. A digital hysteresis current controller generates the switching signals according to the supply voltage, DC link capacitor voltage, modulation frequency and slope of the reference compensating current.

3.1 Synchronous Reference Frame (SRF) transformation

The synchronous reference frame transformation separates the harmonic currents from the fundamental component of the load current which enables the calculation of current references [26-27] as shown in Fig. 2. In this method the active and reactive component of the three-phase systems are represented by the direct and quadrature components respectively. The three phase voltages v_a, v_b, v_c are measured and processed by a phase locked loop (PLL) to generate the unit voltage templates i.e. sine and cosine signals [28]. The three phase load currents i_{Labc} are also measured and transformed into $d-q$ frame. These current signals are further filtered using LPFs to transform them back to the abc frame and then fed to the digital hysteresis current controller to generate the proper switching signals to the SAPF.

The current components in $\alpha-\beta$ coordinates are generated and using θ as a transformation angle, these currents are transformed from $\alpha-\beta$ to $d-q$ frame called as park's transformation,

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{1}$$

SRF isolator extracts the DC component by low-pass-filters for each i_d and i_q . The extracted dc components i_{ddc} and i_{qdc} are transformed back in to $\alpha-\beta$ coordinates using

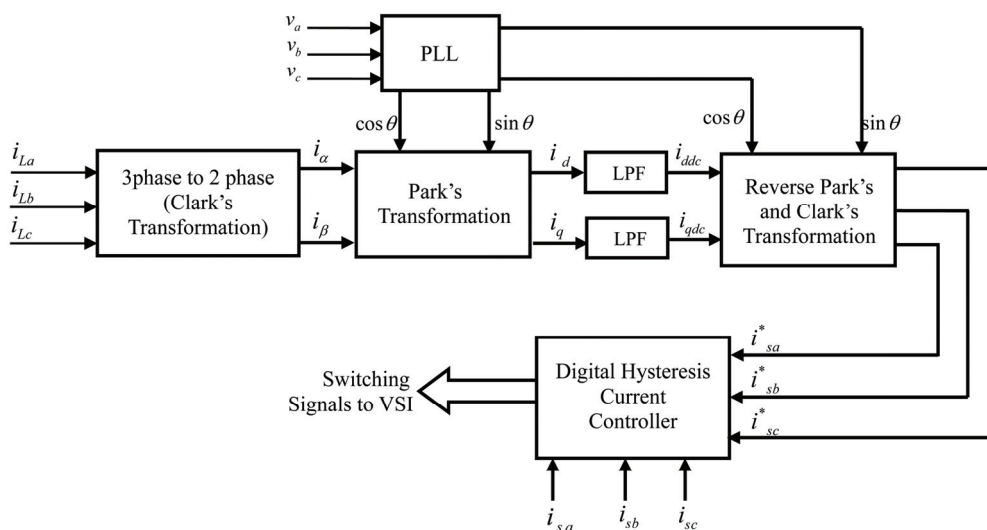


Fig. 2. Block diagram of the reference current generator

Reverse Park's transformation.

$$\begin{bmatrix} i_{\alpha dc} \\ i_{\beta dc} \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} i_{ddc} \\ i_{qdc} \end{bmatrix} \quad (2)$$

From these currents, the transformation is made to obtain three – phase reference source currents in *a-b-c* coordinates using Clark's transformation. Reactive power compensation can be provided by keeping i_q component zero for calculating the reference source currents.

Clark's transformation,

$$\begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \frac{1}{\sqrt{2}} & 1 & 0 \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_0^* \\ i_{s\alpha}^* \\ i_{s\beta}^* \end{bmatrix} \quad (3)$$

3.2 DC link voltage control

The DC link capacitor C_{dc} is fed by the AC system to which SAPF is connected. The total DC voltage can be decreased by injecting active power from the DC capacitor in to the system. When supply voltage is pure sinusoidal, reactive power is demanded only by the current harmonics.

Hence, the losses of SAPF are the active power that needs to be injected by the power system into the DC link to maintain constant DC voltage. The losses of SAPF are primarily the conduction and switching losses of IGBTs and diodes. As a dc bus voltage regulator, a PI regulator as shown in Fig. 3 is utilized to generate a fundamental current reference I_{Fdc}^* for the regulation of the DC bus voltage to its reference value V_{dc}^* and the compensation of VSI losses. A digital PI controller, realized using an efficient FPGA module, has been implemented to control and maintain the DC link voltage.

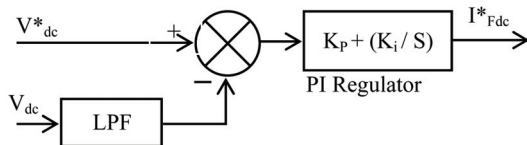


Fig. 3. DC link voltage control block diagram

3.3 Hysteresis current controller

Among the various current control methods proposed for SAPF configurations, hysteresis-band (*hb*) method has been chosen in this work for its quick controllability and easy implementation [29]. In hysteresis-band current controller the actual current continuously tracks the reference current within a hysteresis band to generate the switching patterns for SAPF. When the actual line current of

the SAPF tries to leave the hysteresis band, the appropriate power transistor is switched to ON or OFF state to force the current to lie within the hysteresis band limit. The hysteresis band PWM current controller is employed over the reference active filter current $i_s^* (i_{sa}^*, i_{sb}^*, i_{sc}^*)$ and sensed source current $i_s (i_{sa}, i_{sb}, i_{sc})$ to obtain the switching patterns of SAPF. The switching pattern formulated is as follows,

i) If the upper switch of the leg is ON, and the lower switch is OFF.

ii) If the upper switch of the leg is OFF, and the lower switch is ON.

4. FPGA Description and Design Methodology

In general, flexible and reconfigurable architecture of FPGA devices allow the designer to comply with specific tasks by programming the functionality of the device and hence, suitable for almost all applications. FPGA consist of different types of potential configurable logic blocks (CLBs), including general logic, memory and multiplier blocks which are surrounded by a programmable routing fabric that allows blocks to be programmable interconnected. There exists many configurable technologies and in this work SRAM based FPGA technology is used to reconfigure CLBs, to enable the device for wide range of suitable various applications.

4.1 FPGA design methodology

FPGA is a novel technology against the DSP and MCU with respect to the proposed work in terms of the medium and high running control time 50 KHz. The FPGA module could be used for various applications which include the time multiplexing and parallelism which include the time multiplexing and parallelism. In FPGA *Hierarchy* concept is mainly used to divide the complex design in to modules that are more controllable and the concept *Regularity* is intend to transform, (*abc* to *dq0* to *abc*) for three phase system, discussed in section III is simplified with an adequate choice of scale factors and implemented on FPGA. The first level of reduction allows reducing the number of operations to be implemented to realize the Park's transformation given in (1). The Clark's transformation given in (3) is converted in to *n*- bits fixed point format and the size of the format is arrived on a compromise between the accuracy and the available hardware resources. In the second level partitioning the entire control algorithm is divided in to subparts or modules according to hierarchy and regularity concepts, to realize LPF, IIR filtering and anti-windup circuits. Finally, A^3 methodology is used to find out optimized hardware architecture for a proposed algorithm, while satisfying size and time constraints. The entire control algorithm which includes the signal processing,

SRF transformation, synchronization, LPF, etc., have been implemented using a single all on chip Xilinx Spartan 3A DSP-XC3SD1800 FPGA realize the benefits of high speed computation and flexibility features.

5. Implementation of FPGA Based SAPF

The major objective of this work is to generate the reference compensation signals and actual filter output currents to address the harmonic issues and to maintain unity power factor. Hence, the implementation of the proposed method requires a well-defined modular structure that can be converted in to VHDL coding. In the first step, the system is divided into five modules as shown Fig. 4 and all these five complex modules are decomposed in to sub modules. The second step is to create the register transfer level (RTL) description of the internal data flows. Finally all the defined structures were converted into VHDL code and synthesized into Spartan 3A DSP – XC3SD1800 FPGA using Xilinx ISE design suite.

5.1 Analog to digital conversion module

The Spartan 3A DSP – XC3SD1800 FPGA contains the on-board 12-bit bi-polar AD7266 high speed ADC with a sampling rate up to 2 MSPS. This device contains two 4- input ADCs, each preceded by a 3-channel multiplexer, and a low noise wide bandwidth track-and-hold amplifier that can handle input frequencies in excess of 30 MHz. It manages the clock signals and sends the acquired 12bit data to SRF based distortion detection and PLL modules. These modules operate with a 100MHz clock that allows the A-to-D conversion processes. The inputs are 0-5V signals received from the current-voltage transceiver

connected to the ADC through the general Input / Output (I/O) lines. As the number of analog inputs is limited to 8, 4 each for two ADCs, only two source phase voltages and two source phase currents along with DC link voltage and three load currents are given to the ADCs. It is so programmed in FPGA to estimate the third source voltage and current.

5.2 SRF based detection module

The SRF-transformation contains the Park’s transformation and inverse Park’s transformation. First, it performs the Park’s transformation over the three phase input voltages and load currents to compute the dq0 voltage components. The phase information is calculated and synchronized with utility voltages using PLL module. The three phase PLL module implemented in this work provides an appreciable tracking capability. These modules use the pipelining technique to share multipliers and adders. The Park’s transform ($dq0$) RTL level based schematic diagram is depicted in Fig. 5. The multiplexer selects the inputs and de-multiplexers route the results to output registers. Finally the adders compute the dq components at 50 KHz.

The output variables in the dq frame are sent to the third order LPF to filter out the DC terms. A standard third order Butterworth LPF is used as it offers the lighter in hardware resource consumption and a better understanding of the resulting filter to assure its correctness. Butterworth filter allow the fundamental positive-sequence components and suppress the harmonics and fundamental negative-sequence components effectively. The cut off frequency of LPF is 25 Hz, and the data resolution is 19 bits, which can be managed by the 18-bit multipliers in the Spartan 3A DSP – XC3SD1800 FPGA kit. The numerator and denominator values are scaled and rounded to operate

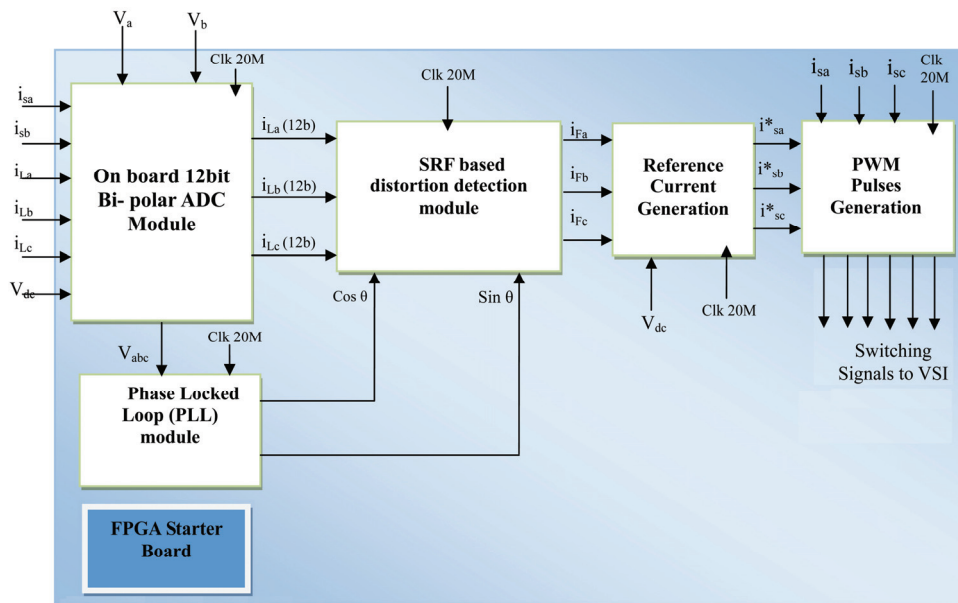


Fig. 4. Modular Design of FPGA Controller

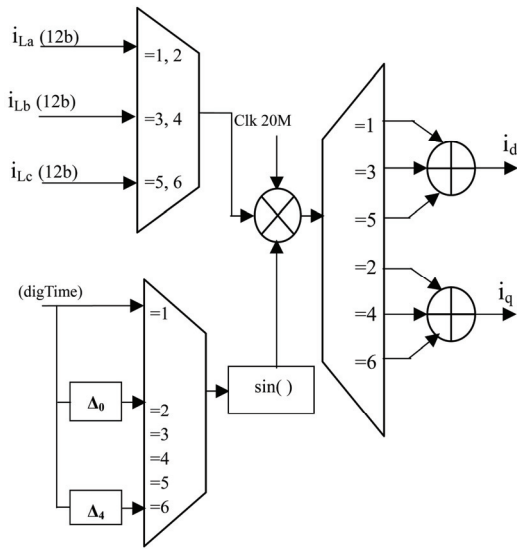


Fig. 5. Direct Park transform schematic at register transfer level

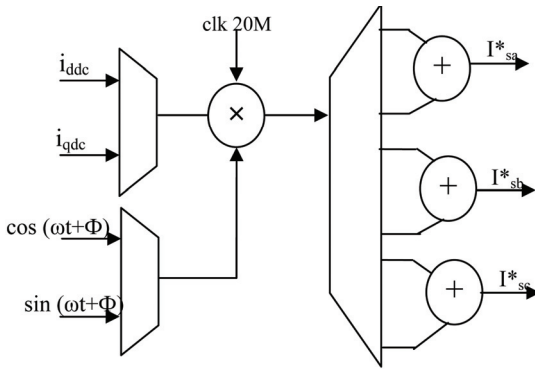


Fig. 6. Clark's transform schematic at register transfer level

with the 18-bit multiplier. Then the resulting values are shortened to maintain value consistency.

Finally the instantaneous active power currents are computed using inverse Clark's transformation. The computed active power currents are subtracted from their corresponding instantaneous source current counterparts and fed to digital hysteresis current controller to produce switching signals to VSI. The RTL schematic of Clark's transformation is presented in Fig. 6.

6. Simulation and Experimental Results

The proposed VLSI architecture for SAPF controller has been simulated using the ModelSim SE6.3f and implemented using the Xilinx 12.1 ISE suite, which includes the Xilinx Plan Ahead package to implement the reconfigurable FPGA design. Compared with the available DSP based method, the proposed method has two merits. The first advantage is the flexibility for reconfiguration which permits the implementation of a modified strategy, if required and error corrections in case of realization or detection of errors on a

later stage. Synthesis and reprogramming are automatically done by specific tools thus shortening the time spent on the modification and correction phases. The same process is used for adding any new functionality also. No hardware change is required for changing the control algorithm. Second, the same VHDL code may be easily synthesized into any other FPGA hardware or even into an ASIC. This allows the advantage of using different technologies for the final hardware implementation

6.1 Simulation results

The entire control has been realized using the VHDL code, which is one of the IEEE industry standard hardware description languages. The complete design flow such as, mapping, routing and synthesis are processed by the Xilinx 12.1 ISE suite. The ModelSim 6.3 and Xilinx simulator has been used for simulation of the Pulse Width Modulation (PWM) pulses. The PWM waveform with a switching frequency (f_s) of 10 KHz and an instantaneous fundamental frequency (f_o) of 50Hz are shown Fig. 7. The complete design flow of SAPF is implemented using Xilinx Plan Ahead [30-31]. The simulation results of complete design flow as shown in Fig. 8, which contains the phase voltages,

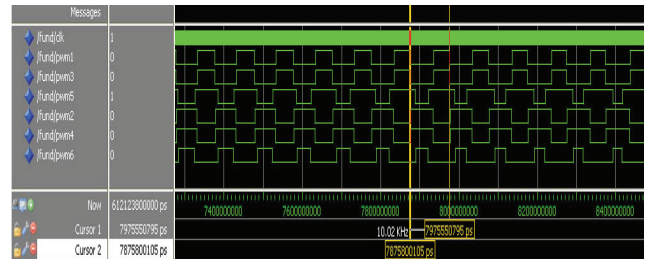


Fig. 7. Simulation results of PWM pulses with $f_s=10$ KHz and $f_o=50$ Hz

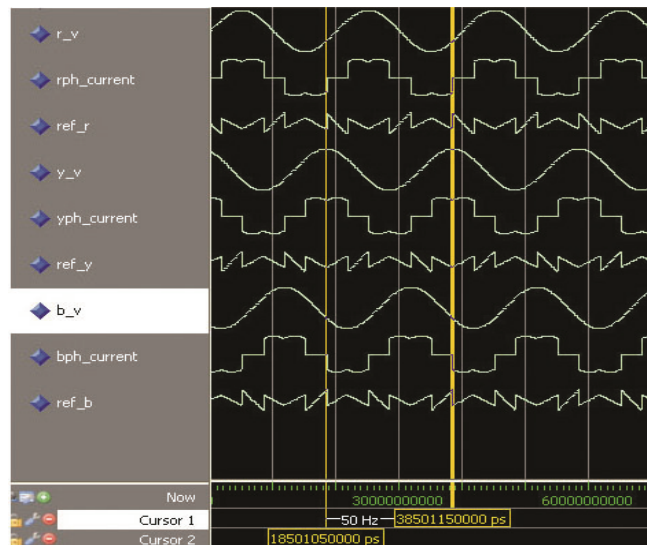


Fig. 8. Simulation results of SAPF complete design flow (ModelSim Simulator)

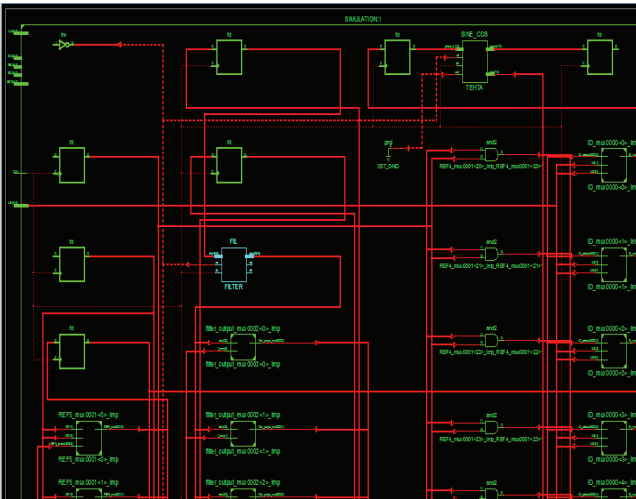


Fig. 9. Schematic of PWM controller showing internal Logic

Table 1. Resource utilization – subsystems

Module	Logic elements	LUT/ Reg LCs	LC, IOBs registers	Bonded
ADC	316	133	256	26
PLL	795	165	220	61
LPF	498	443	896	93
Current controller	58	248	299	32

load currents and reference currents of all the three phases and FPGA controller runs at a synchronous clock rate up to 50MHz. The schematic of the PWM design obtained using Plan Ahead tool as shown in Fig. 9. Table 1 show the resource utilization of ADC, three- phase PLL, LPFs and current controller. The Fig. 8 shows that the reference compensation currents generated in three phases and the reconfiguration time is 2ns when 100MHz system clock. The reconfiguration time depends upon the clock frequency and the logic utilization of the design.

6.2 Experimental results

The laboratory experimental setup was developed to test the performance of the complete design flow including analysis, mapping and controller programmed in Verilog HDL, synthesized using Xilinx's 12.1 ISE design suite and finally loaded to the Spartan 3A DSP – XC3SD1800 FPGA based starter board. The FPGA board can run at a synchronous clock rate of up to 300MHz. The experimental parameters are listed in Table 2.

Table 2. Experimental system parameters

System Parameters	Values
Utility Line Voltage	70V _{rms} / 50Hz
Dc Link capacitor	1300 μ F
Dc Link voltage	250V
Interface Inductor	1500 μ H
Nonlinear Load (Diode bridge rectifier)	1.25 KW

The hardware circuit consists of a Hall-effect voltage sensor, Hall-effect current sensor, power supply, DC side capacitor, AC side inductor, photoreceptors, IGBTs with associated driver circuits. Fast on board ADCs have been used so that the overall control algorithm takes less than 1 μ s, which is negligible compared to the switching period. The utility voltage and DC bus voltage are measured using EM010TENPHIN Hall-effect voltage transducer and the nonlinear load current and inverter currents are measured using the EL100P2 Hall-effect current transducer. The control and gate driver circuits are isolated from the power circuit using fiber optic transmitter (HFBR-1521) and receiver (HFBR-2521). A three level VSI assembly, which consists of a three-phase IGBT based inverter (Intelligent Power Module) stack along with a large DC link capacitor, is being used as the SAPF.

The hardware utilization summary, resulting from the synthesis, is listed in Table 3, which shows the number of Slice flip flops, look-up tables (LUTs), occupied slices, bonded IOBs and DSP48 with the number of available and used resources along with the percentage of utilization. As Table 3 shows the complete design flow can be synthesized in to the single all-on-chip FPGA without any auxiliary circuits.

Table 3. Verilog program summary generated by ise design suite

Logic Utilization	Used	Available	% Utilization
Slice Flip Flops	3187	33280	9%
4 input LUTs	13774	33280	41%
Occupied slices	8258	16640	49%
Bonded IOBs	55	519	10%
DSP48As	45	84	53%

6.2.1 Steady state analysis

The experimental results of three-phase SAPF connected to a 1.25kW diode bridge rectifier feeding a RL load are presented to demonstrate its compensating characteristics. The nature of the load current is non-sinusoidal and it contains the fundamental component and significant harmonics at the PCC as shown in Fig. 10. These signals were recorded using a high performance power analyzer (Yokogawa WT1800). THD of the source currents is found to be 23.5% which is far away to meet the harmonic current distortion constraints set by the IEEE 519 harmonic standard

The Fig. 11 shows that actual compensation current generated by the FPGA for the three-phases which are changing rapidly in accordance with the harmonic signals. It is found that the compensation currents generated experimentally matches accurately with the simulated compensation currents. The output of the SAPF is connected directly to PCC through the 1500 μ H coupling reactance. Therefore the harmonics in the source current are eliminated and source current becomes sinusoidal,

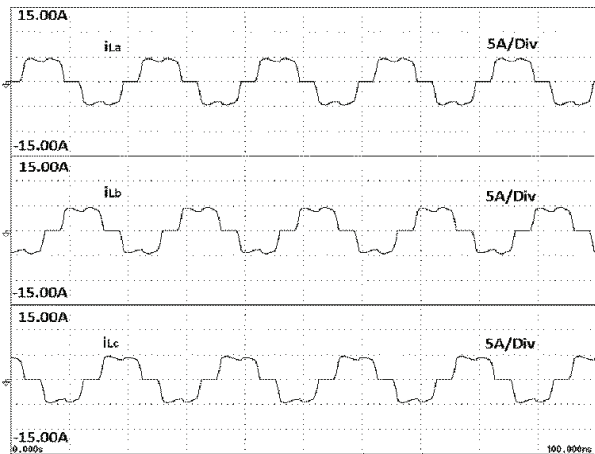


Fig. 10. Three phase load currents of diode rectifier: (a) a-phase load current, Amps; (b) b-phase load current, Amps; (c) c-phase load current, Amps

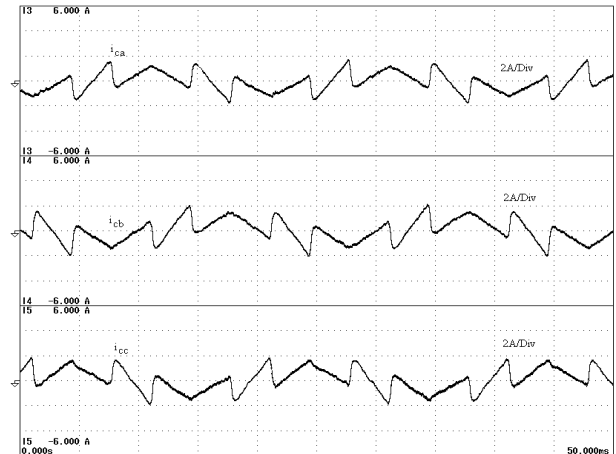


Fig. 11. Reference compensation currents of SAPF; (a) a-phase in Amps; (b) b-phase in Amps; (c) c-in Amps

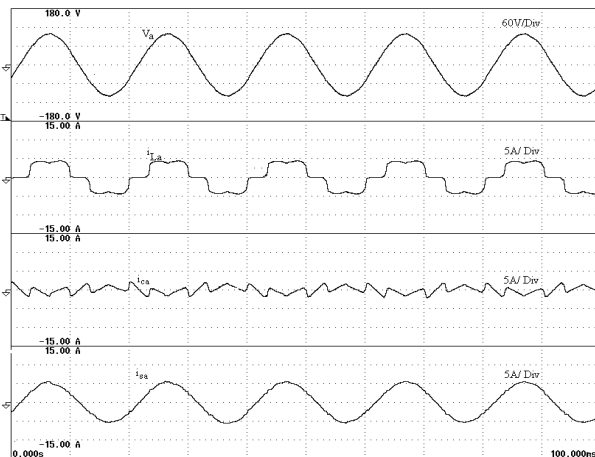


Fig. 12. Experimental steady-state waveform showing phase-a quantities: (a) source voltage; (b) load current; (c) compensation current; (d) source current.

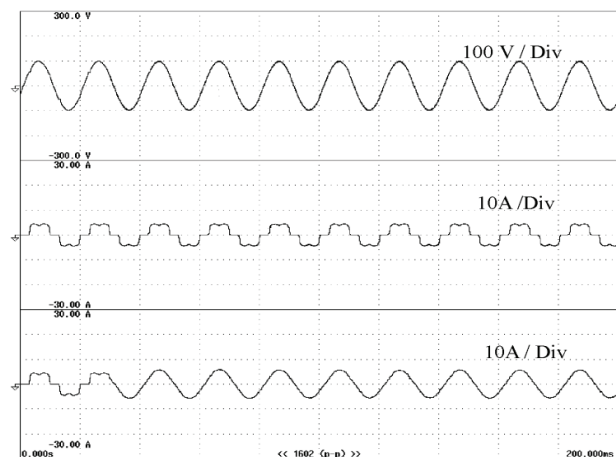


Fig. 13. Experimental steady-state switching response of SAPF phase-a waveforms; (a) source voltage; (b) load current; (c) compensation current; (d) source current.

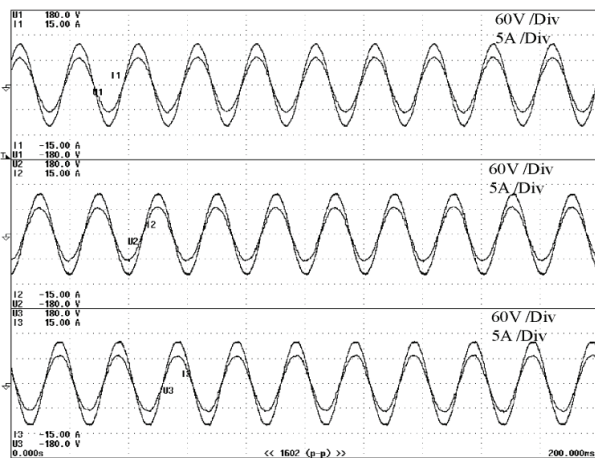


Fig. 14. Experimental steady-state waveform of three phase balanced voltage and currents: (a) a-phase source voltage and current; (b) b-phase source voltage and current; (c) c-phase source voltage and current.

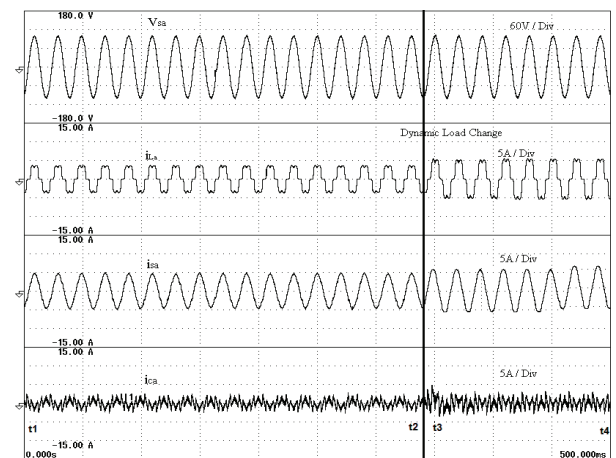


Fig. 15. Dynamic Performance of SAPF step change load condition, where t1–t2 and t3–t4 are steady state durations, and t2–t3 is the transient duration. (Load varies from 1KW to 1.5 KW)

which provides the harmonic and reactive power compensation for the nonlinear load as shown in Fig. 12. The switching performances of the SAPF are depicted in Fig. 13. It is observed that the SAPF system feeds harmonics and reactive power of the nonlinear load locally at the PCC within $4\mu s$ i.e. with the SAPF the supply current once polluted and becomes non-sinusoidal due to harmonics by the addition of nonlinear loads, becomes sinusoidal. The steady state balanced source currents in all three phases are sinusoidal and at unity power factor, when the shunt active filter is functioning, as depicted in Fig. 14. Also, as the reactive power compensation is provided by the SAPF the source current in phase with source voltage.

During the steady state operation all the outputs are stable including the PLL and DC voltage regulators. Due to parallelism operation, all the controllers of the FPGA based architecture are running simultaneously and independently. Under this condition, the gate pulses are generated through the fast ADC to PWM module. The time taken to generate the PWM signals for VSI to generate compensating current, after acquiring the harmonic signals, is estimated as $4\mu s$ (the moment of various analog signals available to AD conversion to reference current generation, ADC sampling is the major part), whereas the time taken by DSP based strategy for same process is $156\mu s$ [32] and $625\mu s$ [11], which is relatively very much higher [33]. The proposed method evidently stating that, key feature of this FPGA based controller over existing DSP or MCU implementations.

6.2.2 Dynamic Analysis

The dynamic response of the proposed FPGA based SAPF system has been analyzed during transients caused by sudden load variations. The load value is varied from 1KW to 1.5KW due to which source current rises rapidly within 20ms as depicted in Fig. 15, where t_1-t_2 and t_3-t_4 are steady state durations, and t_2-t_3 is the transient duration. The supply currents become sinusoidal and balanced, it is observed that the current waveform stabilizes again with in one cycles of the fundamental frequency approximately. This confirms the faster response of the FPGA based SAPF



Fig. 16. Experimental dynamic response of DC-link voltage under step change load condition (load varies from 1KW to 1.5 KW)

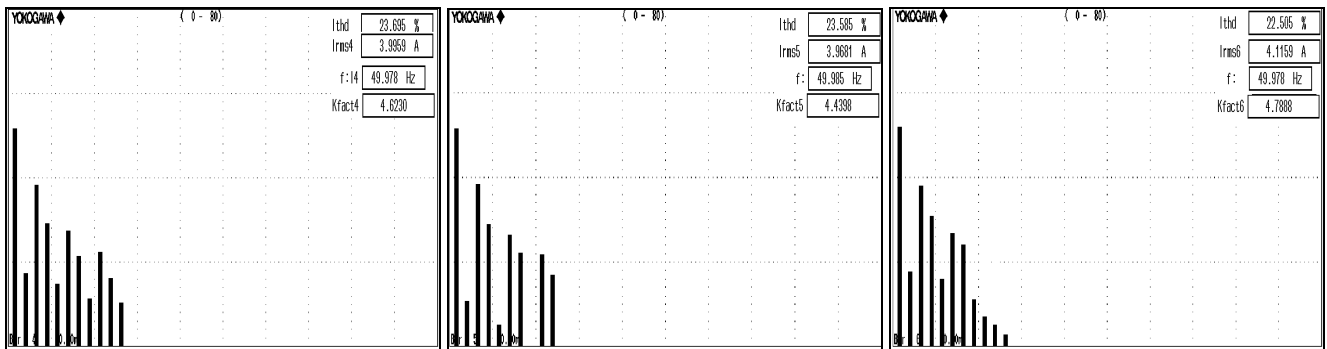


Fig. 17. Harmonic Spectra of (a) phase-a load current; (b) phase-b load current; (c) phase-c load current

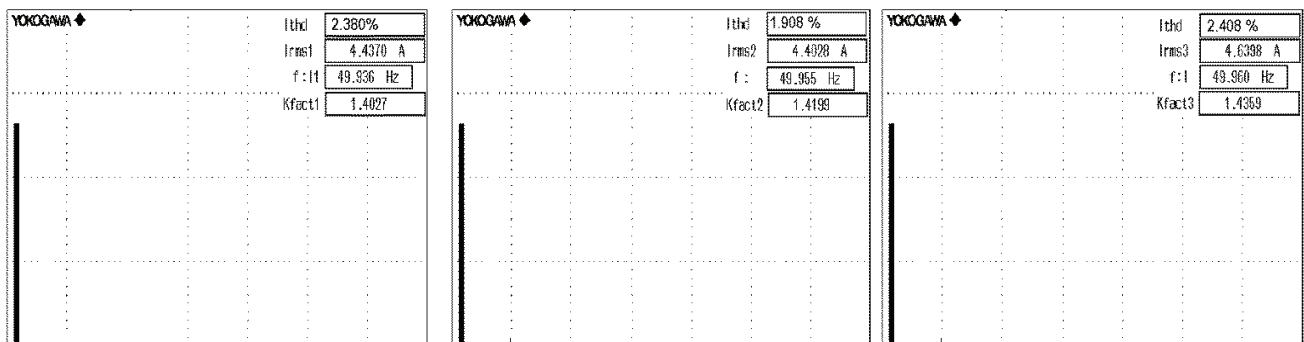


Fig. 18. Harmonic Spectra of (a) phase-a source current; (b) phase-b source current; (c) phase-c source current.

system than DSP based systems.

The DC link capacitor voltage V_{DC} of SAPF is shown in Fig. 16, which was recorded using a mixed signal oscilloscope (Agilent MSO6014A). It is observed that the DC link voltage is stable initially and when the load changes from 1KW to 1.5KW the DC link voltage deviates from the nominal value. However, under the FPGA based fast dynamic control, the DC link voltage is boosted up to the original value of 250V with in the one cycle of the fundamental frequency. This result also proves that the SAPF performs better under dynamic operating conditions.

The Total Harmonic Distortion (THD) in the source current before and after compensation as shown in Fig. 17 and Fig. 18 respectively and the comparison of the same is given in Table 4. The THD value comes down to about 2.2% after compensation from the uncompensated value of 23.6% in phase-A, 23.5% to 1.9% in phase-B and 22.5% to 2.4% in phase-C.

Table 4. THD comparison

Phase	% THD	
	Before compensation	After compensation
A	23.6	2.2
B	23.5	1.9
C	22.5	2.4

7. Conclusion

The simulation and experimental verification of the suitability of a digital implementation of high performance FPGA based control of SAPF has been demonstrated under both steady state and dynamic operating conditions. The dynamic performance of the proposed high performance single all-on-chip FPGA is found to be much faster than the existing DSP based SAPFs. In the proposed controller, with the exception of A/D converters, entire task has been completely built on the FPGA hardware, comprising registers, adders, comparators and multipliers. To analyze the robustness of the proposed technique in terms of harmonic compensation current and reactive power compensation of the system is simulated using ModelSim SE6.3f and Xilinx 12.1 ISE Suite and the simulated results show that the performance of FPGA based SAPF system is relatively far better than that of DSP based systems. To validate the simulated results the entire hardware is fabricated using Xilinx Saptran 3A DSP-XC3SD1800 and its performances are compared with simulated results. It is observed that the experimental results very closely follow the simulated results with negligible differences, during both dynamic and steady states.

Moreover, the proposed FPGA based system exhibits a very fast dynamic response to maintain almost pure sinusoidal supply current around unity power factor, thus mitigating the amplification of load current harmonics in the neighborhood of the associated power system

frequency. The proposed system proves that FPGA based fast dynamic control algorithm is a flexible and successful solution for SAPF and the same design may be replicated on most of the recent FPGA's such as Altera Cyclone II, Xilinx Spartan – 3A/E, and their newer models. The hardware usage summary report motivate authors to take an additional and independent voltage source converter can be controlled with remaining resources, for example control a complete Unified Power Quality Conditioner under balanced and unbalanced load conditions. It is also encouraged to share code in the form of IP cores to leverage FPGA use in power electronics applications.

References

- [1] P. Jintakosonwit, H. Akagi, H. Fujita and S Ogasawara, "Implementation and performance of automatic gain adjustment in a shunt-active filter for harmonic damping throughout a power distribution system", *IEEE Transactions on Power Elect.*, Vol. 17, No. 3, pp. 438-447, 2002.
- [2] R. Inzunza and H. Akagi, "A 6.6-kV transformerless shunt hybrid active filter for installation on a power distribution system", in *Proc. IEEE-PSEC*, 2004, pp. 4630-4636.
- [3] Nasser Eskandarian et al., "Improvement of Dynamic behaviour of Shunt Active Power Filter Using Fuzzy Instantaneous Power Theory," *Journal of power Electronics*, Vol. 14, No. 6, pp. 1303-1313, 2014.
- [4] Zheng Zeng et al., "Fast-Transient Repetitive Control Strategy for a Three-phase LCL Filter-based Shunt Active Power Filter," *Journal of power Electronics*, Vol. 14, No. 2, pp. 392-401, 2014.
- [5] Yu Wang and Yun-Xiang Xie., "Adaptive DC-link Voltage Control for Shunt Active Power Filter," *Journal of power Electronics*, Vol. 14, No. 4, pp. 764-777, 2014.
- [6] Mohammad Monfared et al., "A New Synchronous Reference Frame-Based Method for Single-Phase Shunt Active Power Filters," *Journal of power Electronics*, Vol. 13, No. 4, pp. 692-700, 2013
- [7] Nitin Gupta, Singh S.P, and Bansal R.C, "Digital signal processor based performance evaluation of three-phase four-wire shunt active filter for harmonic elimination, reactive power compensation, and balancing of non-linear loads under non-ideal mains voltages," *Elect. Power Compon. Syst.*, Vol. 40, No. 10, pp. 1119-1148, July 2012.
- [8] Charles S, and Venkatesh Kumar P, "Modelling, simulation and implementation of optimization algorithm based shunt active filter for harmonics mitigation of nonlinear loads," *Aus. J. Elec. Electron Eng*, Vol, 9, No. 1, pp.77-87, 2012.
- [9] Patidar R.D, and Singh S.P, "Digital signal processor based shunt active filter controller for customer-

- generated harmonics and reactive power compensation,” *Elect. Power Compon. Syst.*, Vol. 38, No. 8, pp. 937-959, May 2010.
- [10] George S, and Agarwal V, “A DSP based optimal algorithm for shunt active filter under non sinusoidal supply and unbalanced load conditions,” *IEEE Trans. Power Electron.*, Vol. 22, pp. 593-601, 2007
- [11] Chen Z, and Xu D, “Delayless harmonic detection based on DSP with high-accuracy for active power filter,” *Proceedings of Appl. Power Electron. Conf. Expo*, 1817-1823, March 2005.
- [12] Berto S, Paccagnella A, Ceschia, M, Bolognani, S, and M. Zigliotto, “Potentials and pitfalls of FPGA application in inverter drives – A case study,” *Proceedings IEEE ICIT, Maribor, Slovenia*, 500-505, December. 2003.
- [13] Nascimento P, de Souza H, Neves S, and Limongi, L. R, “FPGA implementation of the generalized delayed signal cancelation phase locked loop method for detecting harmonic sequence components in three phase signals,” *IEEE Trans. Ind. Elect.*, Vol. 60, No. 2, pp. 645-658, 2013.
- [14] Yi Tang, Poh Chiang Loh, Peng Wang, Fook Hoong Choo, Feng Gao, and Blaabjerg F, “Generalized of high performance shunt active power filter with output LCL filter,” *IEEE Trans. Ind. Inform.*, Vol. 59, No. 3, pp. 1443-1452, 2012.
- [15] Junyi Liu, Zanchetta P, Degano, M, and Lavopa E, “Control design and implementation for high performance shunt active filters in aircraft power grids,” *IEEE Trans. on Power Deliv.*, Vol. 59, No. 9, pp. 3604-3613, 2012.
- [16] Monmasson, E., Idkhajine, L., Cirstea, M.N., Bahri, I., Tisan A, and Naouar M.W, “FPGAs in industrial control applications,” *IEEE Trans. Ind. Inform.*, Vol. 7, No. 2, pp. 224-243, 2011.
- [17] Atalik T, Deniz M, Koc E, Gercek C. O, Gultekin B, Ermis M, and Cadirc, I., “Multi-DSP and-FPGA based fully-digital control system for cascaded multi-level converters used in FACTS applications,” *IEEE Trans. Ind. Inform.*, Vol. 8, pp. 511-527, 2012.
- [18] Orlowska-Kowalska, and Kaminski M, “FPGA implementation of the multilayer neural network for the speed estimation of the two-mass drive system,” *IEEE Trans. Ind. Inform.*, Vol. 7, pp. 436-445, 2011.
- [19] Idkhajine L, Monmasson E, Naouar M, Prata, A, and Bouallaga K, “Fully integrated FPGA-based controller for synchronous motor drive,” *IEEE Trans. Indust. Electron.*, Vol. 56, pp. 4006-4017, 2009.
- [20] Guo-Ming Sung, Wei-Yu Wang, and Hsiang-Yuan Hsieh, “Chip implementation of digital scalar space-vector pulse width modulation for induction motor drive,” *Elect. Power Compon. Syst.*, Vol. 39, No. 16, pp. 1733-1747, 2011.
- [21] Lakka M, Koutroulis E, and Dollas A, “Development of an FPGA-based SPWM generator for high switching frequency DC/AC inverters,” *IEEE Trans. power Electron.*, Vol. 29, No. 1, pp. 356-365, 2013.
- [22] Bahri I, Idkhajine L, Monmasson E, and El Amine Benkhelifa, M., “Hardware/Software Codesign Guidelines for System on Chip FPGA-Based Sensorless AC Drive Applications,” *IEEE Trans. Ind. Infor.*, Vol. 9, No. 4, pp. 2165-2176, 2013.
- [23] Curkovic M, Jezernik K, and Horvat R, “FPGA-Based Predictive Sliding Mode Controller of a Three-Phase Inverter,” *IEEE Trans. Ind. Elect.*, Vol. 60, No. 2, pp. 637-644, 2013.
- [24] Sutikno T, Idris N, Jidin A, and Cirstea M.N., “An Improved FPGA Implementation of Direct Torque Control for Induction Machines,” *IEEE Trans. Ind. Elect.*, Vol. 9, No. 3, pp. 1280-1290, 2013.
- [25] Munoz J, Espinoza J, Espinosa E, Baier, C., and Melin P., “Systematic design comparison of discrete-time linear controllers for a DSTATCOM,” *Proceedings of IEEE ISIE.*, Vol. 4., 1103-1109, 2010
- [26] S. Bhattacharya and D. Divan, “Synchronous frame harmonic isolator using active series filter”, *In Proc. Eur. Power Electron. Conf.*, 1995, pp. 3030-3035.
- [27] B Singh and J. Solanki, “A comparison of control algorithms for DSTATCOM”, *IEEE Transactions on Industrial Electronics*, Vol. 56, No.7, pp. 2738-2745, 2009.
- [28] S. Hirve, K. Chatterjee, B. G. Fernandes, M. Imayavaramban, and S Dwari, “PLL - Less Active power filter based one cycle control for compensating Unbalanced Loads in Three Phase Four Wire System”, *IEEE Transactions on Power Delivery*, Vol. 22, No. 4, pp. 2457-2465, 2007.
- [29] Bhim Singh, K. Al-Haddad, A. Chandra, “A New Control Approach to Three-phase Active Filter for Harmonics and Reactive Power Compensation”, *IEEE Transactions on Power Systems*, Vol. 13, No. 1, pp. 133-138, 1998.
- [30] N. Dorairaj, Eric Shiflet and Mark Goosman, “Plan Ahead software as a platform for partial reconfiguration”, *Xcell Journal (Xilinx)*, Vol. 55, pp. 68-71, 2005.
- [31] Xilinx, “PlanAhead User Guide,” UG632 (v 11.4), 2009.
- [32] Roux le W, and Wyk Van J, “The effect of signal measurement and processing delay on the compensation of harmonics by PWM converters,” *IEEE Trans. Ind. Appl.*, Vol. 47, No. 2, pp. 297-304, 2000.
- [33] Zeliang Shu, Yuhua Guo, and Jisan Lian, “Steady-state and dynamic study of active power filter with efficient FPGA-based control algorithm,” *IEEE Trans. on Ind. Elect.* Vol. 55, No. 4, pp. 1527-1535, 2008.



Charles S He received his B.E. (2004) in electrical and electronics engineering and his M.E. (2006) in power electronics and drives from Anna University, India. Currently, he is an assistant professor in the Department of Electrical and Electronics Engineering, Sri Shakthi Institute of Engineering and Technology, Tamilnadu, India. He is currently working toward his Ph.D. at Anna University Chennai, India. He is a member of the IEEE. His current research interests include power electronics applications in distribution systems, real-time digital simulation and control, field-programmable gate array implementation, and active power filters for power conditioning.



Vivekanandan C He received his bachelor degree in electrical and electronics engineering and his master degree in applied electronics from Bharathiyar University in 1986 and 1988, respectively, and his Ph.D. from Anna University, Chennai, Tamilnadu, India, in 2009. Presently he is a professor and vice principal at S.N.S College of Engineering, Coimbatore, Tamilnadu, India. He is a life member of IEEE, a fellow of the Institute of Engineers (FIE), a life member in the Indian Society for Technical Education (MISTE), System Society of India (MSSI), and a member in the Association of Computer Electronics and Electrical Engineers (MACEEEE). His areas of interest include sliding-mode control, digital control systems, algorithm development, and embedded systems.