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Hybrid Cascaded MLI topology using Ternary Voltage Progression Technique with Multicarrier Strategy

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Abstract – A major problem in conventional multilevel inverter is that an increase in power semiconductor switches causes an increase in cost and switching losses of the inverter. The multicarrier strategy adopted for the multilevel inverters has become more popular due to reduced cost, lower harmonic distortion, and higher voltage capability than the conventional switching strategy applied to inverters. Various topologies and modulation strategies have been reported for utility and drive applications. Level shifted based pulse width modulation techniques are proposed to investigate the performance of the multilevel inverter. The proposed work focuses on reducing the utilized switches so that the cost and the switching losses of the inverter do not go up and the consistent efficiency could be achieved. This paper presents the detailed analysis of these topologies. The analysis is based on the number of switches, DC sources, output level, maximum voltage, and the efficiency. As an illustration, single phase cascaded multilevel inverter topologies are simulated using MATLAB/SIMULINK and the experimental results demonstrate the viability of these inverters.

Keywords: Multilevel inverter, Level shifting technique, Multicarrier strategy, Unequal DC sources

1. Introduction

Multilevel inverter (MLI) has offered the solution to increase the converter output voltage above the voltage limits of classical semiconductors [1-3]. The stepped approximation of the sinusoidal output waveform with higher levels reduces the harmonic distortion of output waveform. They finds applications mainly in industries such as Brushless DC motor, AC power supplies, renewable energy sources, drive systems, etc. The output voltage waveform of a multilevel inverter is composed of the number of voltage levels, obtained from capacitor voltage sources. The multilevel inverters are basically classified into three topologies namely, the flying capacitor inverter, the diode clamped inverter and the cascaded H-bridge inverter [4, 5]. All the topologies have same property of reducing the harmonics. The cascaded has disadvantage, it needs separate DC sources but circuit layout is compact and voltage sharing problem is absent. Due to these advantages, the cascaded inverter bridge has been widely applied to the applications such as HVDC, SVC, stabilizer, high power motor drive and so on [6, 7].

Prominence of this topology is attributable to its characteristics compared with diode clamped and capacitor clamped inverter. The cascaded multilevel inverter has multiple units of H-bridge. It provides a cost effective solution in low and medium voltage applications. By proper control, the number of levels at output voltage increases to yield a nearly sinusoidal waveform. The advantages get enhanced as the level increases to maximum. The symmetric cascaded multilevel inverter uses SDCSs to synthesize a desired voltage from several independent sources of DC voltages, which may be obtained from batteries, fuel cells, or solar cells. This configuration has recently become very popular in AC power supply and adjustable speed drive applications. Furthermore, asymmetric cascaded multilevel inverters use unequal DC sources [8] which increase the modularity of the circuit. In recent literature [9-12], a wide variety of control methods and designs have been developed. The major disadvantage associated with recent development with reduced number of switches, is their circuit complexity due to the bulky capacitor. Additional design complications might be imposed, especially regarding the design of device heat sinks.

Unfortunately, modulation technique does not serve the purpose with the increased number of auxiliary bridges. Moreover, a large number of auxiliary bridges have to be employed and large capacitor banks need to be included. An attempt has been made to find the performance of the cascaded multilevel inverter topologies [13-15]. Moreover, this topology has binary and ternary progression. This paper discusses the optimization of the utilization of switches and improving the output voltage resolution. To produce an output with higher number of levels and a minimum number of switches unequal DC sources are used to compare these configurations. Ternary progression [16] provides a higher number of output levels, lower number of components, and high modularity.

Modulation control of any type of multilevel inverter

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is quite challenging, and much of the reported research is based on the heuristic investigations. Modulation techniques to control the performance of multilevel inverter include Selected Harmonics Elimination, Space Vector PWM (SVPWM), Carrier-Based PWM (CBPWM) [17], Symmetrical step control and Optimization angle control techniques [18].

Various modulation strategies have been introduced for the cascaded multi level inverters to reduce the harmonic contents [19]. The concept of sinusoidal PWM modulation has been introduced in an attempt to reduce the harmonic contents at the output voltage [20, 21]. The Level shifted modulation technique gives better results compared with the phase shifting technique. Level shifting is done to reduce the harmonics at the output voltage [22, 23]. The use of power electronic converters at high-power levels usually demands a reduction in the switching frequency, to ensure that losses caused by the imperfect nature of practical switching devices do not significantly reduce the converter efficiency [24-27].

The simulated results have been experimentally verified, using a cascaded H-bridge topology, operating as an inverter. Multilevel inverter systems have been compared on the basis of overall performance and attempt is being made to adopt the best modulation strategy for one topology to other structures. Finally, a prototype is realized to verify the feasibility and desired performance and confirm the high dynamic performance of the inverter. The first section focuses on the research advances in developing cascaded multilevel inverter topologies. In Section 2, the suggested topology is well explained in terms of working principles, voltage steps, and DC supply selection. The proposed configuration is compared with its counterpart. Section 3 explicates the experimental set-up. The literature cited above, does not deal with the experimental verification of the MLI. In the proposed work a prototype is developed for all the topologies and presented.

2. Cascaded H-Bridge Structure and Operation

A cascaded multilevel inverter consists of a series of H bridges in each phase. For three level output, H-Bridge topology requires one DC source along with four MOSFET switches. The output voltage can have three values V_{dc}, $-V_{dc}$ and 0 depending on the status of the switches.

Table 1. Comparison of components required for cascaded multilevel inverter

Parameters	Symmetric	Ternary
Number of levels	2N+1	3^N
Number of switches	4N	4N
Number of DC Sources	N	N
$V_{0,Max[pu]}$	N	$(3^N-1)/2$

2.1 Symmetric multilevel topology

A single-phase 7-level configuration of such an inverter is shown in Fig. 1.

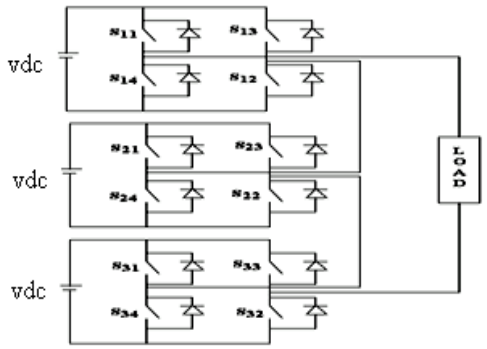


Fig. 1. Structure of Symmetric cascaded multilevel inverter

Each SDCS is associated with a single-phase full-bridge inverter. The AC terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S_1 - S_4, each inverter can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. The AC output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels is defined by

$$M = 2N+1 \quad (1)$$

Table 2 summarizes the number of levels, switches, DC sources and maximum output voltage for symmetrical cascaded multilevel inverter.

Table 2. Performance parameter of Symmetric topology

Parameters	Symmetric Inverter	Required components
Number of levels	2N+1	7
Switches Number	4N	12
DC source number	N	3
$V_{0,Max[pu]}$	N	3

2. 2 Ternary topology

To provide a large number of output levels without increasing the number of inverters, asymmetric multilevel inverters can be used. It is proposed to choose the DC-voltage sources according to a geometric progression with a factor of 2 or 3. Using these sources, the number of voltage levels and the maximum output voltage being binary and ternary DC voltage progression on Asymmetric Cascaded Multilevel Inverter (ACMLI) are generated. Advantage of this topology is that the control and protection requirements of each bridge are modular. Increasing the number of levels provides more steps; hence, the output voltage will be of enhanced resolution and the reference sinusoidal output voltage can be better achieved.

The structure introduced in this work is an Asymmetric cascaded multilevel inverter that uses unequal DC Sources. The general function of this multilevel inverter is the same as that of the other inverters. Asymmetric cascaded-inverter provides a large number of output voltage levels without increasing the number of full bridge units. Owing to the reduction in the number of DC Sources employed, the structure becomes more reliable, and the output voltage has higher resolution due to the increased number of steps. This configuration recently became very popular in AC power supply and adjustable speed drive applications. This inverter can avoid extra clamping diodes or voltage balancing capacitors [28].

As depicted in Fig. 2 an Asymmetric cascaded H-bridge inverter circuit is proposed. This is an unequal voltage progression with the amplitude of DC voltage having a ratio of 1:3:9:27; 81.... 3N and the maximum output voltage reaches $((3^N\text{-}1)/2)\ V_{dc}$. The ACMLI consists of 3-bridges, used to generate 27 level output for the DC Sources of 9:3:1 ratio. The output waveform has 27 levels as +13Vdc…….+1Vdc and zero. By different combinations of the 12 switches, S_1−S_{12}, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero.

For N of such cascade inverters, one can achieve the following distinct voltage levels

$$n = 3^N, \quad \text{if } V_{dc,j} = 3^{j-1}V_{dc}, \quad j = 1, 2, \ldots, N \tag{2}$$

The maximum output voltage of these N cascaded multilevel inverters is

$$V_{0,MAX} = \sum_{j=1}^{N} V_{dc,j} \tag{3}$$

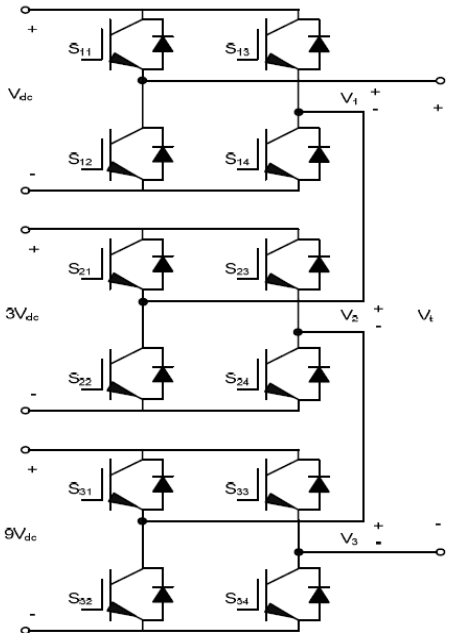


Fig. 2. Ternary asymmetric cascaded multilevel inverter

$$V_{0,MAX} = \left(\frac{3^N - 1}{2}\right) V_{dc} \tag{4}$$

if $V_{dc,j} = 3^{j-1}\ V_{dc}, \quad j = 1,2\ldots\ldots..N$

Table 3 summarizes the number of levels, switches, DC sources and maximum output voltage for asymmetrical cascaded multilevel inverter.

Table 3. Performance parameters of Ternary topology

Parameters	Asymmetric Inverter (Ternary)	Required components
Number of level	3^N	27
Number of Switches	4N	12
Number of DC source	N	3
$V_{0,Max[pu]}$	$(3^N\text{-}1)/2$	13

From Table 2 and 3, it is seen that for the same number of bridges, switches, asymmetric MLI provides, more number of levels and higher $V_{0,Max[pu]}$. Table 4 provides a brief comparison of the proposed topology with the conventional one of cascaded multilevel inverter. For ACMLI topology, 12 MOSFETs with 3 DC sources are required. With lesser number of components, the ACMLI topology provides higher number of levels. Also, the voltage and the current rating of the switches play an effective role in the cost of the system. Here the asymmetric topology employs unequal DC sources with Ternary progression. The proposed topology requires only 12 switches instead of 48 switches of the conventional topology. This attainment reduces the installation cost and the area of the proposed topology compared with the conventional inverter. In addition to it, the complexity

Table 4. Comparison of proposed topology with conventional topology

Output voltage level	Symmetric Topology		Asymmetric topology	
	No of Bridges	No of Switches	No of Bridges	No of switches
3	1	4	1	4
5	2	8	-	-
7	3	12	-	-
9	4	16	2	8
11	5	20	-	-
27	12	48	3	12

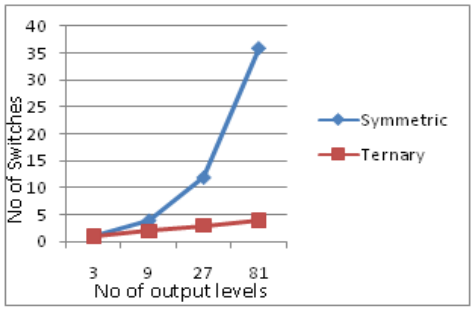


Fig. 3. Number of switches against number of output levels

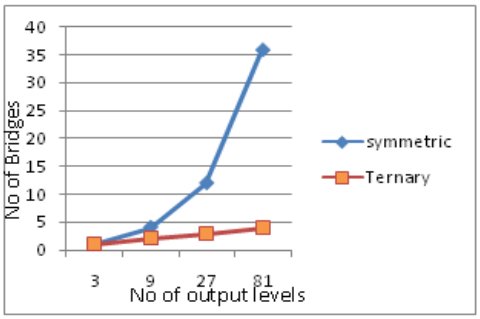


Fig. 4. Number of bridges against number of output levels

involved in the control circuit is also minimized. Comparison of the proposed topology like the number of bridges with the number of output levels and the number of switches with the number of output levels is shown in Fig. 3 and 4 respectively.

2.3 Multi carrier based PWM methods

Pulse width modulation refers to a method of carrying information on a train of pulses; the information is encoded in the width of each pulse. This technique helps in maintaining a constant voltage. In the carrier-based multilevel modulation, each level in a phase requires a carrier of its own. Carrier- based modulation schemes are mainly divided into two categories: level-shifted (LSPWM) and phase-shifted (PSPWM) methods. Both of these have several variations that differ by the allocation of the module carriers with respect to each other [29]. In all level-shifted PWM methods, the carriers of the modules have a frequency of $f_{car}=1/T_{sw}$. The frequency of the carrier signal is inversely proportional to the switching period of the device. The reference voltage, on the other hand, can have values in the range of $-MV_{dc}$ and MV_{dc}[30, 31]. To cover the entire voltage range, the triangular carrier waves with the same phase and peak to peak amplitude, are arranged vertically, so that the carrier of the first module covers the range from zero to Vdc, while the second covers the range from Vdc to 2Vdc [29]. The last module covers the voltage from (M−1) V_{dc} to MV_{dc}. This method is generally used in CMLI as it gives a reduced THD. Therefore, an inverter with *M*- modules in series is usually referred to as an *n*-level inverter and the number of levels can be calculated as given in Eq. (5).

$$n = 2M + 1 \ldots \quad (5)$$

Here, n is the number of DC sources. M is the number of levels. There are three kinds of level shifted modulation techniques, namely; Phase Opposition Disposition (POD, Alternative Phase Opposition Disposition (APOD), and Phase Disposition (PD). All the three modulation strategies have been simulated and the performance parameters are analyzed. Compared with the other modulation techniques, PD modulation gives lower harmonic indices.

PD modulation is harmonically superior, because it places harmonic energy directly into the carrier harmonic for each phase leg, and relies on the cancellation of the harmonic across phase legs as the line-to-line voltage is developed [26]. By using this fact, an effective new modulation strategy is proposed for Ternary based inverter which is also the modulation control approach with unequal voltage sources. The model is designed with remarkable architecture of proposed switching pattern to reduce the offset of the carrier signal. It differs from hybrid modulation, where the frequency of the positive rail differs from the negative one and from the discontinuous modulation; the reference waveform must split into sections. A new modulation control Scheme is developed to regulate the output voltage of the inverter by controlling the gate pulses applied to the switches of the inverter.

This section briefly describes the design of control strategies for an inverter. The basic structure of a 27 level inverter is used in this work. Sub-systems shown in Fig. 8 are used in the main circuit to ensure the minimal connections. As shown in Table 7, the carrier signals are generated into the required fashion to develop the new modulation scheme. As the proposed approach reduces harmonic contents, the quality of output waveform is improved. Compared with the conventional MCPWM schemes, performance of the system is enhanced with the developed approach.

The first stage of the design is the process of creating the switching pattern as per the control scheme. The generated patterns for ternary based inverter are depicted in Table 7. In quarter cycle of the waveform, each step is cracked based on the switching pattern given in the Table 7 and named correspondingly. From the output graph of the inverter, the patterns are created such that the modulation waveform generates the required steps. The HV side pulses are created by appending the pulses to the front and the LV side pulses are created by appending the pulses to the rear end of the original pulses generated by the inverter without modulation. The resultant waveform has a train of pulses at both the ends. Rules for the modulation scheme, to control the inverter output voltage are developed to improve the control performance.

Switches of the ternary inverter are driven as per the algorithm given below.

Step 1: For M level, M-1 carrier signals are generated and compared with the reference sinusoidal wave,

$$Rs >= Cs_{1\text{-}13} = A \text{ to } M \quad (6)$$

Step 2: Modulation steps are selected for the positive half cycle and the mold equations are marked

$$\overline{((\bar{A})+(B-D+E-G+H-J+K-M))} \quad (7)$$

From the above equation, it is easy to generate the signal

for the positive half of the switch S_1.

Step 3: The carrier signals are generated for the negative half of the Switch S_1

$$Rs <= Cs_{-1-13} = A \text{ to } M \quad (8)$$

Step 4: Modulation steps are selected for the negative half cycle and the mold equations are marked

$$\overline{((\bar{B})+(C-E+F-H+I-K+L))} \quad (9)$$

Using the above mentioned steps, the modulation scheme is developed. This method of modulation results in best switching transition as it avoids misfiring increases the efficiency and span of the inverter.

3. Results and Discussions

To ensure the feasibility of the proposed inverter, the power circuit is simulated using MATLAB / Simulink software and verified through the simulation results. Symmetric cascaded multilevel inverter that contains three H-Bridges with equal DC sources as shown in Fig. 5. Ternary asymmetric multilevel inverter contains three H-Bridges with unequal DC sources of 1:3:9 ratios as shown in Fig. 12. Hardware implementation is done for both the topologies. From Table 4, it is observed that ternary ACMLI is good from structure point of view. For the same number of bridges, the ACMLI gives more levels than symmetric MLI. For harmonic minimization, level shifted method is implemented only in ACMLI. From simulation results, it is seen that Phase Disposition (PD) technique has higher fundamental voltage and comparatively lesser THD content. Concept of applying multicarrier based modulation schemes on asymmetric voltage sources inverter is not reported in literature. In the proposed work, hardware realization is made to demonstrate the effectiveness of proposed ternary voltage progression with new modulation technique for hybrid ACMLI. Table 5 summarizes the rated data like range of DC sources, type of switches, type of controller and load parameter for both symmetric and Ternary MLI to implement in hardware.

Table 5. Experimental parameters as implemented in inverter

Parameters	Symmetric	Ternary
DC voltage sources	V1=V2=V3=24V	V1=4V V2=12V V3=36 V
Type of switch	MOSFET	MOSFET
Type of Controller	Atmel AT89C52	ARM NUC140XXCN

3.1 Symmetric cascaded MLI

The power circuit shown in Fig. 1 is simulated by using MATLAB/SIMULINK software and verified through the simulation results. Seven level symmetri cascaded MLI involves the usage of three H-Bridges with equal DC sources. In the simulation the switches are ideal. The single phase seven level output voltage is shown in Fig. 5 (a) and the harmonics spectrum is shown in Fig. 5 (b). THD content at output voltage is 25.09%. To validate, hardware is implemented and its prototype has been manufactured. A power circuit is fabricated by using 12 MOSFETs. The driving pulse required for the MOSFETs IRF540 is obtained from this microcontroller AT89C52 IC is used. The Atmel AT89C52 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

During the hardware implementation,the setup is tested for 24V with switching frequency f = 50 Hz. As illustrated in Fig. 1, the experimental setup is built for the generation of desired output voltage waveform. The output voltages

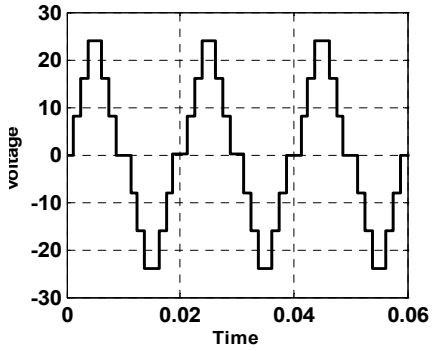


Fig. 5. (a) Simulated output voltage waveform of symmetric multilevel inverter

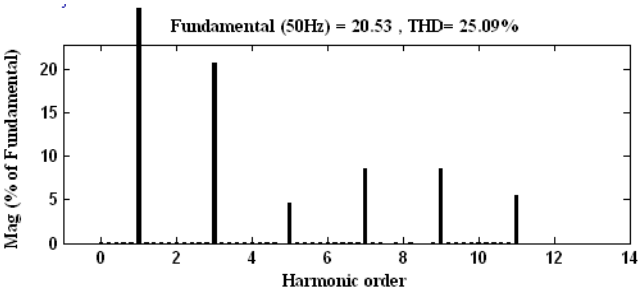


Fig. 5. (b) Harmonic spectrum of output voltage waveform

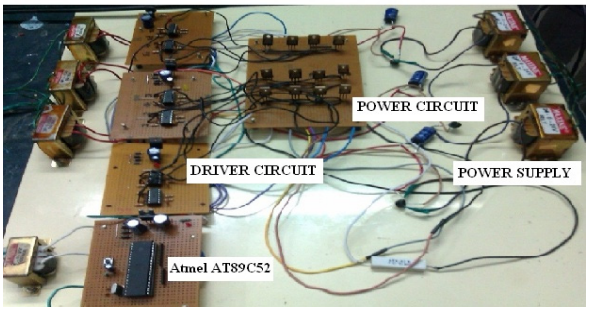


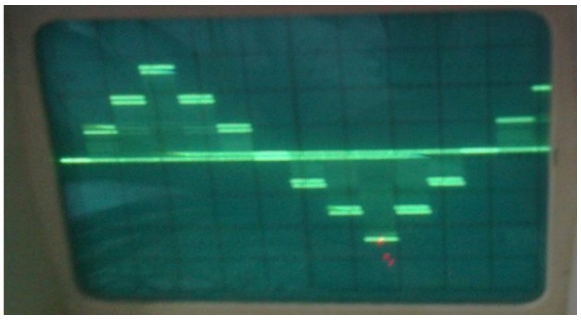
Fig. 6. Experimental setup for symmetric multilevel inverter

with seven-level stepped waveform can be clearly appreciated; the experimental setup is shown in Fig. 6. As depicted in Fig. 7, this waveform corresponds well with the simulated waveform obtained.

3. 2 Ternary ACMLI

The simulink model for twenty seven levels MLI is shown in Fig. 8. They are created with a separate sub system as shown in the simulink model. The pulses are generated with the developed pattern and given to the corresponding switches through the subsystems. The sub-systems and proposed pattern generation of driving pulse for switch S1 are shown in Fig. 9 and Fig. 10(c) respectively. The generated patterns for ternary based inverter and the key waveform for the design of gate pulses using presented pattern are shown in Fig. 10(b). To determine the harmonics in the proposed circuit, the FFT analysis is performed, and presented in Fig. 13(b). It is clear from the FFT analysis, that the harmonics are reduced to a greater extent in ACMLI compare with the symmetric topology. A new modulation strategy is employed in the circuit. In ternary MLI, total harmonic distortion (THD) is reduced and it is seen that harmonic profile is highly improved. The THD obtained for the output voltage waveform is 4.28%.

A power circuit is fabricated using 12 MOSFETs (IRF540), and it requires three individual DC sources of



Scale: X-axis 1CM=5mSec, Y-axis 1CM=8 Volts

Fig. 7. Output voltage waveform of symmetric multilevel inverter

Table 6. Switching state of the proposed multilevel inverter during positive half cycle

Level	Output voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	V_{dc}	1	1	0	0	0	1	0	1	0	1	0	1
2	$2V_{dc}$	0	0	1	1	1	1	0	0	0	1	0	1
3	$3V_{dc}$	0	1	0	1	1	1	0	0	0	1	0	1
4	$4V_{dc}$	1	1	0	0	1	1	0	0	0	1	0	1
5	$5V_{dc}$	0	0	1	1	0	0	1	1	1	1	0	0
6	$6V_{dc}$	0	1	0	1	0	0	1	1	1	1	0	0
7	$7V_{dc}$	1	1	0	0	0	0	1	1	1	1	0	0
8	$8V_{dc}$	0	0	1	1	0	1	0	1	1	1	0	0
9	$9V_{dc}$	0	1	0	1	0	1	0	1	1	1	0	0
10	$10V_{dc}$	1	1	0	0	0	1	0	1	1	1	0	0
11	$11V_{dc}$	0	0	1	1	1	1	0	0	1	1	0	0
12	$12V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	0
13	$13V_{dc}$	1	1	0	0	1	1	0	0	1	1	0	0

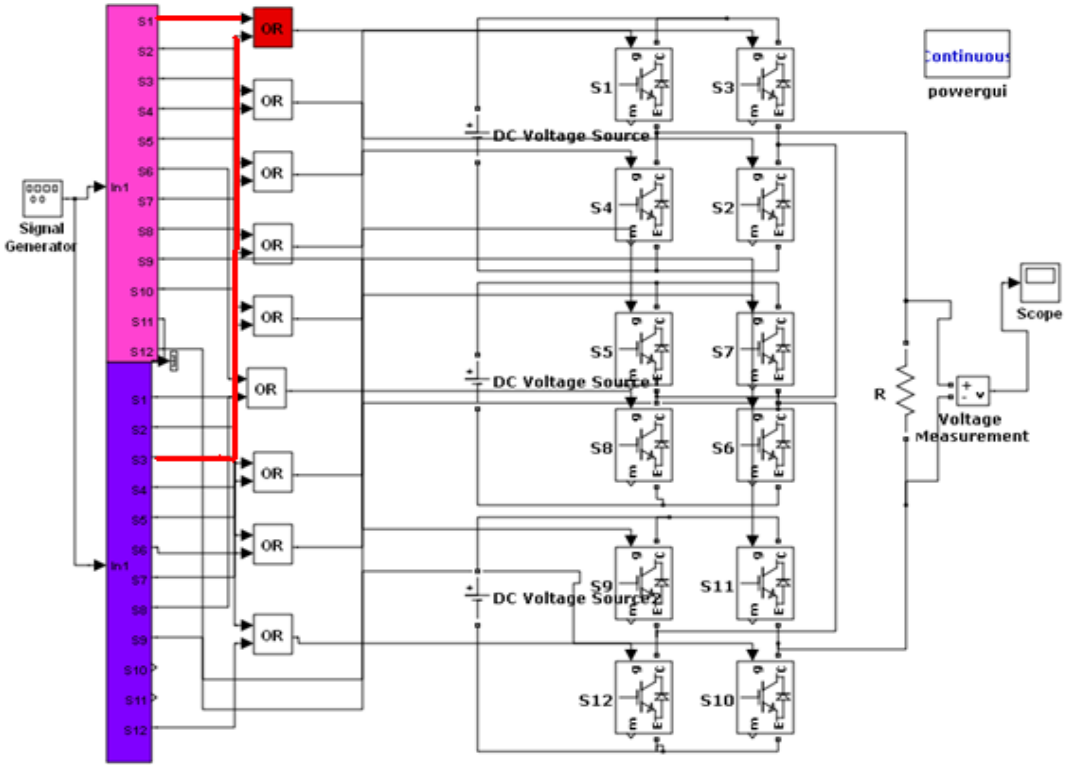


Fig. 8. Simulink model of ternary multilevel inverter

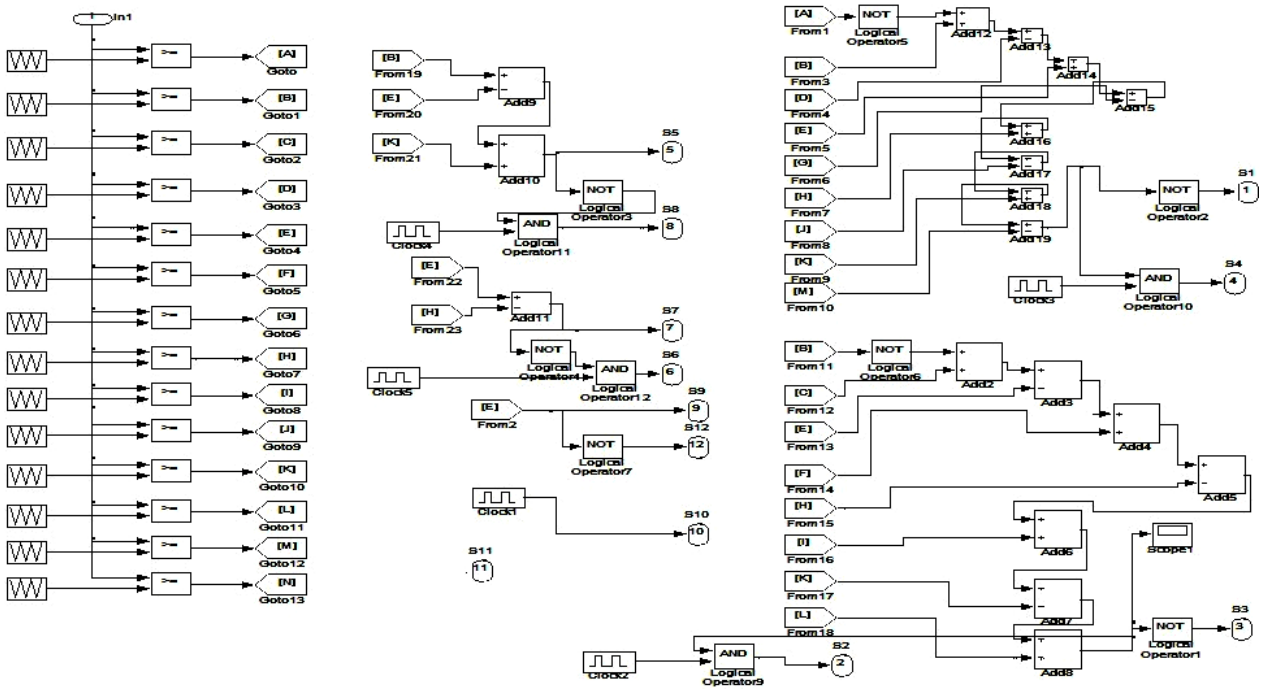


Fig. 9. Subsystem for generation of positive half of driving pulses

Table 7. Modified switching sequence for the proposed modulation Scheme

Level	Output voltage	Switching pattern for Positive Half cycle	Switching pattern for Negative Half- cycle
1	V_{dc}	[10,12,6,8,2] /{1}↔{4}	[10,12,6,8,4]/{3}↔{2}
2	$2V_{dc}$	[10,12,6]/{1,2,8}↔{3,4,5}	[12,10,8]/{4,3,6}↔{1,2,7}
3	$3V_{dc}$	[4,5,6,10,12]/{3}↔{2}	[8,7,2,12,10]/{1}↔{4}
4	$4V_{dc}$	[2,5,6,10,12]/{4}↔{1}	[8,7,4,12,10]/{2}↔{3}
5	$5V_{dc}$	[10]/{1,2,5,6,12}↔{3,4,7,8,9}	[12]/{8,7,4,3,10}↔{11,5,6,1,2}
6	$6V_{dc}$	[4,7,8,9,10]/{3}↔{2}	[12,11,5,6,2]/{1}↔{4}
7	$7V_{dc}$	[2,7,8,9,10]/{1}↔{4}	[12,11,4,5,6]/{2}↔{3}
8	$8V_{dc}$	[8,9,10]/{1,2,7}↔{3,4,6}	[12,11,6]/{4,3,5}↔{1,2,8}
9	$9V_{dc}$	[4,6,8,9,10]/{3}↔{2}	[12,11,8,6,2]/{1}↔{4}
10	$10V_{dc}$	[2,6,8,9,10]/{4}↔{1}	[12,11,4,8,6]/{2}↔{3}
11	$11V_{dc}$	[6,9,10]/{1,2,8}↔{3,4,5}	[12,11,8]/{4,3,6}↔{1,2,7}
12	$12V_{dc}$	[4,5,6,9,10]/{3}↔{2}	[12,11,8,7,2]/{1}↔{4}
13	$13V_{dc}$	[2,5,6,9,10]/{4}↔{1}	[4,8,7,12,11]/{2}↔{3}

Table 8. Comparison of performance parameters - Ternary asymmetric multilevel Inverter

Scheme/ Approach	Number of computational steps	Number of levels	Fundamental voltage in p.u	% of THD	Magnitude of h3 (as % of fundamental)	Magnitude of h5 (as % of fundamental)
Without Modulation	-	27	0. 804	12. 80	4. 81	1. 65
Optimization angle control Technique	26	27	0. 930	4. 73	1. 23	0. 83
Conventional Modulation	26	27	0. 994	4. 28	0. 22	0. 1
Proposed modulation scheme	13	27	0. 999	4. 28	0.01	0.01

an asymmetric ternary ratio. MOSFET with anti-parallel diodes are employed as switching devices. During the hardware implementation, the inverter is tested for 52V. Each inverter leg takes different voltages. During the implementation, the inverter input s ources are taken as V_{dc1} = 4 V, V_{dc2} = 12V and V_{dc3} = 36V with switching frequency f = 50 Hz. The prototype of this inverter thus includes the following; three DC supplies, three H-Bridge power circuits and embedded controller (ARM® Cortex™-M0 Core NUC140XXCN microcontroller) as shown in Fig. 12. The microcontroller is used to generate the driving pulses for the switches in the power circuit. Modulation is generally performed in any circuit to reduce the harmonic content at the output voltage. Power circuit remains the

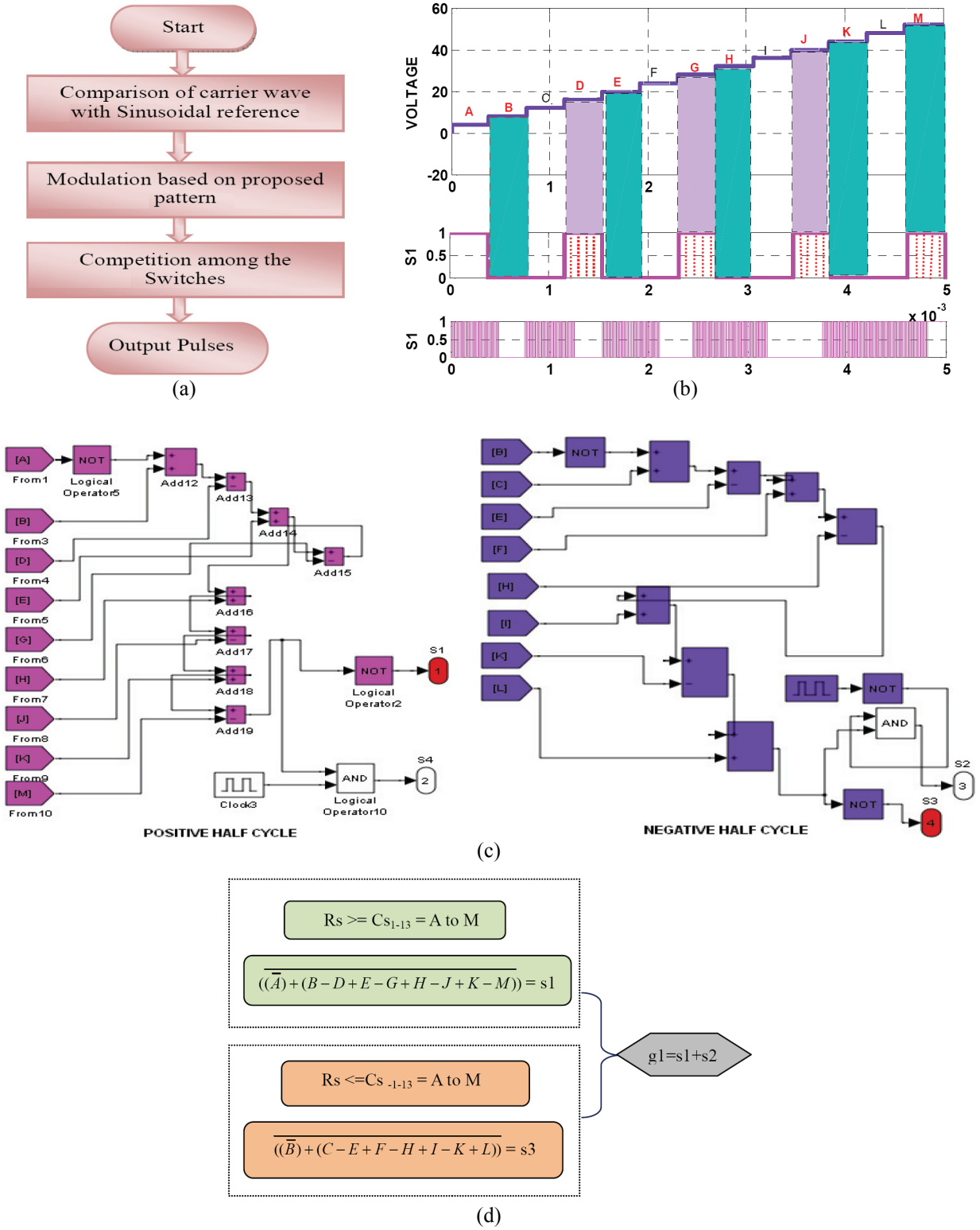


Fig. 10. (a) Design flow chart; (b) Key waveforms of proposed pattern; (c) Proposed pattern generation of driving pulse for switch S_1; (d) Statistical representation of driving pulse for switch S_1

same. The generation of modulated pulse remains distinct. This is the logical extension of the sine triangle PWM multilevel inverter, in which (n-1) carriers are needed for an n-level inverter. The preferred type of carrier generation is Phase disposition.

As discussed in section 2. 3, the design flowchart as depicted in Fig. 10(a) corresponds to the modulated pulse. Triangular waveform and reference sinusoidal waveform

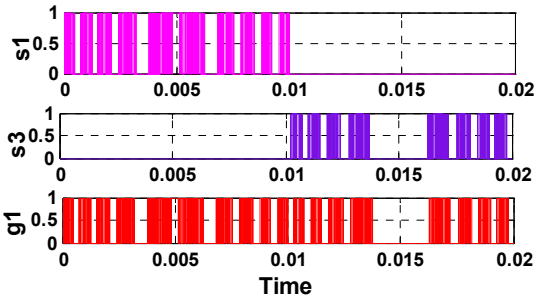


Fig. 11. Modulated driving pulse for Switch S_1

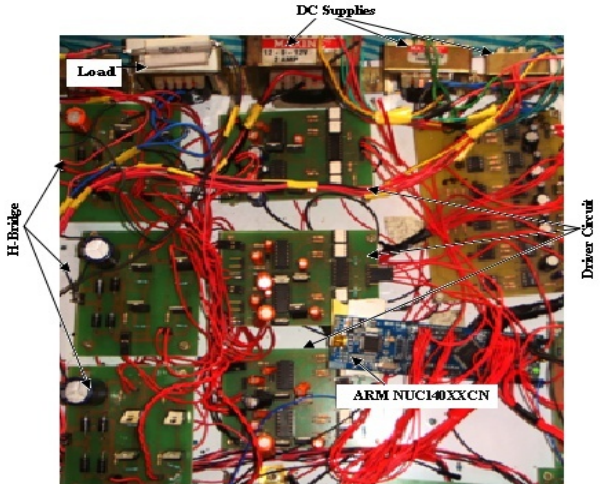


Fig. 12. Experimental setup of ternary multilevel inverter

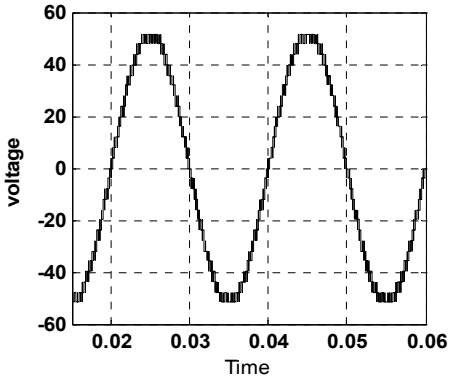


Fig. 13. (a) Simulated Output voltage waveform of ternary multilevel inverter

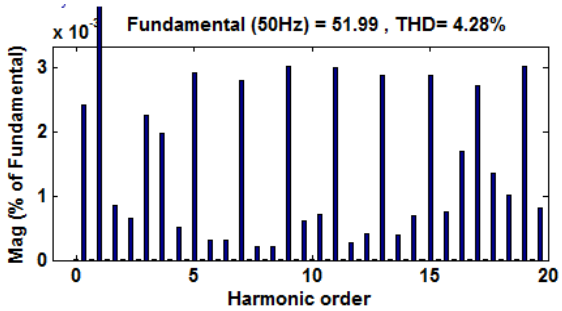


Fig. 13. (b) Harmonic spectrum of output voltage waveform

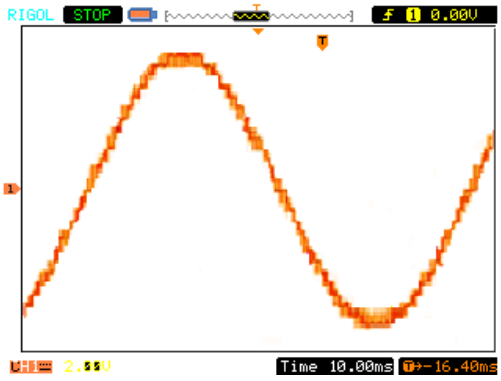


Fig. 14. Output waveform of Ternary Multilevel Inverter (X axis 1 CM = 10 ms, Y axis 1 CM = 20 V)

obtained from positive and negative half cycle are combined by logical OR and are used to drive the power semiconductor switches. Fig. 10(c) gives the statistical representation of driving pulse for switch S_1 and Fig. 11 depicts the modulated driving pulses exist for Switch S_1. The carriers are arranged in vertical shifts in continuous bands, defined by the levels of the inverter. Hence for a 27-level inverter, 26 carriers are used. Each carrier has the same frequency and amplitude. As illustrated in Fig. 2, the experimental set-up is built for the generation of desired output voltage waveform. In order to reach the 27 level, 3 unequal DC sources along with 12 switches are used. As depicted in Fig. 14, this waveform corresponds well with the simulated waveform obtained. Experimental set-up is built to the above discussed approach and the output waveforms are generated. The 27 level output voltage waveform with the modulation performed at 20 kHz switching frequency is recorded using RIGOL DS1052E type digital oscilloscope and presented in Fig. 14.

In optimization angle control techniques, firing angles will be given to the switches with a phase delay of 180° or to positive half cycle of sine wave. As the number of levels increases, the calculation of firing angle becomes complex. Practically, the implementation of this method requires memorizing all the firing angles. It leads to complexity in the control strategy and considerable computational costs. Mathematical solutions with limited computational costs are therefore preferably used for real-time applications. But in the proposed scheme, no such complicated calculations are carried out. The pattern is created only for the quarter cycle. This scheme is well suited for other multicarrier methods also.

A comparative study has been made to demonstrate the superiority of the proposed multilevel inverter over the conventional approaches and presented in Table 8.

From Table 8, it is observed that the number of computational steps needed to achieve the same number of voltage levels is the same except the proposed modulation. With proposed modulation scheme, the number of steps to achieve the same number of output voltage levels is halved and hence the computational efforts are reduced by 50%.

The magnitude of the fundamental voltage is higher and the magnitude of lower order harmonics, total harmonic distortion (THD) content at output voltage are lesser than that in other schemes.

4. Conclusion

In this paper, a Ternary cascaded multilevel inverter topology with an unequal DC source has been proposed. The suggested configuration is formed by cascading three H-bridges with unequal DC sources in the ratio of 1:3. Indeed, Symmetric and Ternary multilevel inverters have been compared to determine a most favorable arrangement with minimal semiconductor switching devices and optimal output voltage. To verify the performance of the cascaded topologies, both the symmetric and ternary configurations are simulated and tested experimentally using Atmel AT89C52 controller and ARM® Cortex™-M0 Core controller respectively.

A single phase 27-level asymmetric cascaded multilevel inverter with multicarrier strategy is implemented to demonstrate some of its advantages: excellent voltage waveforms reduced Total harmonic distortion (THD) and improved efficiency. The voltage harmonic of Ternary multilevel inverter using multicarrier strategy has been brought to less than 5%. It uses lesser number of switches and DC sources; thus by decreasing the complexity, installation area, cost of the circuit and an increase in the efficiency of an inverter by 88%. Obtained simulation and hardware results agree well with the desired output and hence, subsequent work in the future may include an extension to three-phase with some control techniques.

References

[1] Rodriguez, J, Jih-Sheng, L., Fang Zheng, P, 'Multilevel inverters: a survey of topologies, controls, and applications', IEEE Trans. Ind. Electron., Vol. 49, pp. 724-738, August 2002.

[2] M. N. A. Kadir, S. Mekhilef, H.W. Ping, "Voltage vector control of a hybrid three-stage 18-level inverter by vector decomposition", IET Power Electron, vol. 3, pp. 601-611, 2010.

[3] J. Holtz, "Pulse width modulation-a survey". 23rd Annual IEEE Power Electronics Specialists Conference, 1992, PESC '92 Record, vol. 1, pp. 11-184, 1992.

[4] Colak, E. Kabalci, R. Bayindir, "Review of multilevel voltage source inverter topologies and control schemes", Energy Convers. Manage., vol. 52, pp. 1114-1128, February 2011.

[5] L. Jih-Sheng, P. Fang Zheng, "Multilevel converters-a new breed of power converters". Conference Record of the 1995 IEEE Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS '95, vol. 3, pp. 2348-2356, November 1995.

[6] Czarkowski, Liu, Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters", in Proc. Industry Applications Annu. Meeting, pp. 1454-1461, 1998.

[7] Sakly, Delarue, Bausiere, "Rejection of undesirable effects of input DC-voltage ripple in single-phase PWM inverters", in Proc. 5th Eur. Conf. on Power Electronics and Applications, vol. 4, pp. 65-70, 1993.

[8] P. Wheeler, L. Empringham, D. Gerry, "Improved output waveform quality for multi-level H-bridge chain converters using unequal cell voltages". (IEE Conf. Publ. No. 475) Power Electronics and Variable Speed Drives, 2000. Eighth International Conference on, pp. 536-540, 2000

[9] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," IEEE Trans. Ind. Appl., vol. 41, pp. 655-664, Mar./Apr. 2005.

[10] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," IEEE Trans. Power Electron., vol. 23, pp. 2657-2664, November 2008.

[11] Nami, F. Zare, G. Ledwich, A. Ghosh, and F. Blaabjerg, "Comparison between symmetrical and asymmetrical single phase multilevel inverter with diode-clamped topology," in Proc. IEEE PESC 2008, pp. 2921-2926.

[12] J.Song-Manguelle, "Asymmetrical multilevel inverter for large induction machine drive," in Electrical Drives and Power Electronics International Conference, The High, Tatras, Slovakia, 2001.

[13] M. N. Abdul Kadir and Z. F. Hussein, "Asymmetrical multilevel inverter using ratio-three based sources," in Proc. IEEE PE Con 2004, pp. 137-142.

[14] S. Mariethoz and A. Rufer, "New configurations for the three-phase asymmetrical multilevel inverter," in Proc. IEEE 39th IAS Annu. Meeting, pp. 828-835, 2004.

[15] Zh. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, H. Li, and A. Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," in Proc. IEEE PESC 2006, pp. 1-6.

[16] S.Me khilef, M.N.A Kadir, 'Novel vector control method for three stage hybrid cascaded multilevel inverter', IEEE Trans. Ind. Electron, vol. 58, pp. 1339-1349,2011.

[17] J. Gayathri Monicka, V. Jamuna, "Optimal Switching Strategy of Level shifted Carrier based PWM Technique for Asymmetric Multilevel Inverter" Proceeding of the Intl.Conf.on Inter Discplinary Research in Engineering &Technology pp. 146-150, August 2014.

[18] Dhavalpatel, HimanshuN.Chaudhari, HinaChandwani andAnandDamle, "Analysis and Simulation of Asymmetrical Type Multilevel Inverter using Optimization

Angle Control Technique" International Journal of Advanced Electrical and Electronics Engineering, vol. 1, pp. 81-86, 2012.
[19] Grath, Holmes, "Multicarrier PWM strategies for multilevel inverters", IEEE Trans. Ind. Electron., vol. 49, 858-867, August 2002.
[20] M. S. A. Dahidah and V. G. Agelidis, "Single carrier sinusoidal PWM equivalent selective harmonic elimination for a five level voltage source inverter", Electr. Power Syst. Res vol. 78, pp. 1826-1836, November 2008.
[21] R. Naderi, and A. Rahmati, "Phase shifted carrier PWM technique for general cascaded inverters", IEEE Trans. Power Electron., vol. 23, pp. 1257-1269, May 2008.
[22] J. H. Kim, S. K. Sul, and P. N. Enjeti, "A carrier based PWM method optimal switching sequence for a multilevel four-leg voltage source inverter", IEEE Trans. Ind. Applic., vol. 44, pp. 1239-1248, 2008.
[23] C. Govindaraju and K. Baskaran, "Performance analysis of cascaded multilevel inverter with hybrid phase-shifted carrier modulation", Aust. J. Electr. Electron. Eng., vol. 7, pp. 121-132, June 2010.
[24] J. Napoles, A.J. Watson, J.J. Padilla, J.I. Leon, L.G. Franquelo, P.W. Wheeler, M.A. Aguirre, "Selective Harmonic Mitigation Technique for Cascaded H-Bridge Converters With Nonequal DC Link Voltages", IEEE Trans. on Industrial Electronics, vol. 60, pp. 1963-1971, May 2013.
[25] Chung-Ming Young, Neng-Yi Chu, Liang-Rui Chen, Yu-Chih Hsiao, Chia-Zer Li, "A Single-Phase Multilevel Inverter With Battery Balancing", IEEE Trans. on Industrial Electronics, vol. 60. pp. 1972-1978, May 2013.
[26] Y. Kumsuwan, S. Premrudeepreechacharn, V. Kinnares, "A Carrier-Based Unbalanced PWM Method for Four-Leg Voltage Source Inverter Fed Unsymmetrical Two-Phase Induction Motor", IEEE Trans. on Industrial Electronics,. Vol. 60, pp. 2031-2041, 2013
[27] N. Bodo, E. Levi, M. Jones, "Investigation of Carrier-Based PWM Techniques for a Five-Phase Open-End Winding Drive Topology", IEEE Trans. on Industrial Electronics, vol. 60, pp. 2054-2065, 2013.
[28] Loh, Holmes, Lipo, "Implementation and control of distributed PWM cascaded multilevel inverters with minimal harmonic distortion and common-mode voltage", IEEE Trans. Power Electron., vol. 20, pp. 90-99, January 2005.
[29] Tengfei Wang and Yongqiang Zhu, "Analysis and Comparison of Multicarrier PWM Schemes Applied in H-bridge Cascaded Multi-level Inverters", IEEE Conference on Industrial Electronics and Applications (ICIEA), pp. 1379-1383, 2010.
[30] Mahmoud M. Gaballah, "Design and Implementation of Space Vector PWM Inverter Based on a Low Cost", Arab J Sci Eng, December 2012.
[31] Weerapon kongnun, Apinan aurasopon, "A Novel Electronically Controllable of Current-Mode Level Shifted Multicarrier PWM Based on MO-CFTA", radio engineering, vol. 22, 2013.

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