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# Improved KY Converter

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**Abstract** – In this paper, an improved KY converter is presented, which is constructed mainly by one charge pump capacitor and one central-tapped coupling inductor. Besides, a passive clamping snubber is added to this converter to improve the efficiency above half load. As compared to the KY converter, the voltage conversion ratio of the proposed converter is upgraded significantly. In this paper, the basic operating principles and mathematical deductions of the proposed converter are described, along with some experimental results provided to demonstrate the feasibility and effectiveness of the proposed converter.

**Keywords**: High step-up converter, KY converter, Charge pump, Central-tapped coupling inductor

## Nomenclature

| | |
|---|---|
| $S_1$, $S_2$, $S_3$ | Switches |
| $D_b$ | Charge pump diode |
| $D_1$, $D_2$, $D_3$ | Body diodes for $S_1$, $S_2$, $S_3$ |
| $D_o$ | Output diode |
| $D_{sn}$ | Snubber diode |
| $L_p$ | Primary self-inductance |
| $L_s$ | Secondary self-inductance |
| $L_1$ | Inductance equal to $L_p$ |
| $L_2$ | Inductance equal to $L_p$ plus $L_s$ |
| $L_{LK}$ | Leakage inductance |
| $C_b$ | Charge pump capacitor |
| $C_o$ | Output capacitor |
| $C_{sn}$ | Snubber capacitor |
| $R_o$ | Output load resistor |
| $N_p$ | Primary turns |
| $N_s$ | Secondary turns |
| $n$ | Turns ratio equal to $N_s/N_p$ |
| $V_i$ | Input voltage |
| $V_o$ | Output voltage |
| $v_{ds3}$ | Voltage across $S_3$ |
| $v_{Dsn}$ | Voltage across $D_{sn}$ |
| $v_{gs1}$, $v_{gs2}$, $v_{gs3}$ | Gate-source signals for $S_1$, $S_2$, $S_3$ |
| $v_{Csn,max}$ | Maximum voltage across $C_{sn}$ |
| $v_{Csn,min}$ | Minimum voltage across $C_{sn}$ |
| $\Delta v_{Cb}$ | Voltage ripple on $C_b$ |
| $\Delta v_{Cb,max}$ | Maximum value of $\Delta v_{Cb}$ |
| $\Delta v_{Co}$ | Voltage ripple on $C_o$ |
| $\Delta v_{Co,max}$ | Maximum value of $\Delta v_{Co}$ |
| $i_{L1}$ | Current flowing through $L_1$ |
| $i_{L2}$ | Current flowing through $L_2$ |
| $i_{L2,peak}$ | Peak-to-peak value of $i_{L2}$ under BCM |
| $i_{LK}$ | Current in $L_{LK}$ |
| $\Delta i_{L2}$ | Current ripple in $L_2$ |
| $I_{LB}$ | Average current in $L_p$ under BCM |
| $I_{o,rated}$ | Rated output current |
| $I_{o,min}$ | Minimum output current |
| $I_{Cb,DTs}$ | Average value of $i_{Cb}$ during the turn-on period |
| $I_{Co,DTs}$ | Average value of $i_{Co}$ during the turn-on period |
| $I_{L1}$ | Average current in $L_1$ |
| $I_{L2}$ | Average current in $L_2$ |
| $I_{Lp,max}$ | Maximum value of $i_{Lp}$ |
| $I_{L1,max}$ | Maximum value of $i_{L1}$ |
| $I_{L2,max}$ | Maximum value of $i_{L2}$ |
| $T_s$ | Switching period |
| $D$ | Duty cycle |
| $\varphi$ | Flux in the central-tapped coupling inductor |
| $\Re$ | Flux resistance of the core |
| $f_s$ | Switching frequency |
| $L_{p\_s\text{-}short}$ | Primary inductance with secondary side shorted |
| $L_{s\_p\text{-}short}$ | Secondary inductance with primary side shorted |
| $K_{ps}$ | Coupling coefficient with primary side referred to secondary side |
| $K_{sp}$ | Coupling coefficient with secondary side referred to primary side |
| $K$ | Geometric average value of $K_{ps}$ and $K_{sp}$ |
| $E_{LK}$ | Energy stored in $L_{LK}$ |
| $M_1$, $M_2$, $M_3$ | Gate driving signals for $S_1$, $S_2$, $S_3$ |
| $R_{o,max}$ | Maximum value of output load resistor |

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## 1. Introduction

Because of the global warming, the demand of the green power has been increasing for decades. These kinds of green power facilities include solar cells, fuel cells, etc. In many applications, high voltage conversion converters play an important role in boosting the low output voltages of green power facilities to the high voltages which the loads need. Regarding the traditional non-isolated voltage-boosting converters [1, 2], such as the traditional boost

converter and buck-boost converter, their voltage gains are not high enough. Up to now, many kinds of voltage-boosting techniques have been presented, including several inductors which are magnetized and then pump the stored energy into the output with all inductors connected in series [3], coupled inductors with turns ratios [4-8, 10, 11, 15, 19], voltage superposition based on switching capacitors [9, 13-20], auxiliary transformers with turns ratios [12], etc. In [8] and [10], the output terminal is floating, thereby increasing application complexity. In [4-11, 16, 17, 19] and [20], these converters contain too many components, thereby making the converters relatively complicated.

Based on the mentioned above, a novel step-up converter is presented, which is based on charge pump capacitor and one central-tap coupling inductor so as to improve the voltage conversion ratio of the KY converter. In this converter, a passive clamping snubber is used to decrease the voltage spike on the switch, and hence the switch with low turn-on resistance can be used. In this paper, the basic operating principles and the mathematical deductions will be described and some experimental results are provided to verify the effectiveness of the proposed topology.

## 2. Overall System Configuration

Fig. 1 shows the proposed high step-up converter. This converter is constructed by three switches $S_1$, $S_2$ and $S_3$ along with the corresponding body diodes $D_1$, $D_2$ and $D_3$, one output diode $D_o$, one charge pump diode $D_b$, one charge pump capacitor $C_b$, one output capacitor $C_o$, one central-tapped coupling inductor established by one primary self-inductance $L_p$ and one secondary self-inductance $L_s$, and one output load resistor $R_o$.

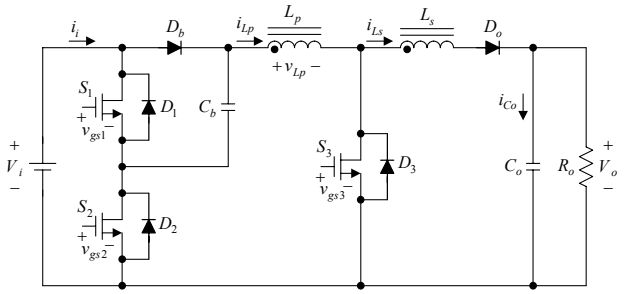


**Fig. 1.** Proposed high step-up converter.

## 3. Basic Operating Principles

Prior to this topic, there are some assumptions and symbols to be given:

(1) The voltage across the charge pump capacitor $C_b$ is equal to the input voltage $V_i$.
(2) The value of the output capacitor $C_o$ is larger enough to keep the output voltage constant $V_o$ at some value.
(3) The input current is signified by $i_i$, the current in $C_b$ is denoted by $i_b$, the current in $L_p$ is represented by $i_{Lp}$, the current in $L_s$ is indicated by $i_{Ls}$, and the current in $C_o$ is described by $i_{Co}$.
(4) The flux in the central-tapped coupling inductor is represented by $\varphi$.
(5) The primary-side and secondary-side turns are signified by $N_p$ and $N_s$, respectively, and $n$ is defined to be $N_s$ over $N_p$.
(6) The gate driving signals for $S_1$, $S_2$ and $S_3$ are $v_{gs1}$, $v_{gs2}$ and $v_{gs3}$, respectively.
(7) The switching period is $T_s$.
The blanking times between $S_1$ and $S_2$ are negligible.
(8) As the converter operates in the continuous conduction mode (CCM) and the boundary conduction mode (BCM), the turn-on interval for $S_1$ and $S_3$ is $DT_s$, whereas the turn-on interval for $S_2$ is $(1-D)T_s$.
(9) As the converter operates in the discontinuous conduction mode (DCM), the time required by $L_p$ or $L_s$ to release the stored energy to zero is denoted by $\Delta_1 T_s$, and the time interval without any current in $L_p$ or $L_s$ is indicated by $\Delta_2 T_s$, equal to $(1-D)T_s - \Delta_1 T_s$.
(10) All components, including the switches, diodes, capacitors and central-tapped coupling inductor, are considered to be ideal.

Figs. 2 and 3 show the key waveforms for the converter operating in CCM and DCM, respectively.

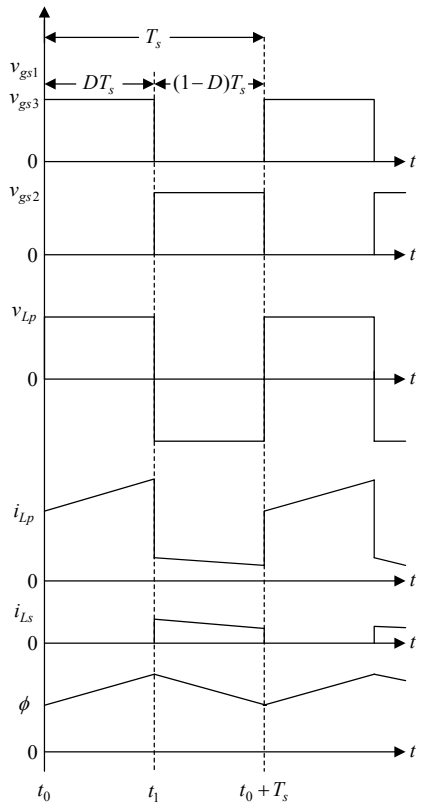


**Fig. 2.** Illustrated waveforms for the converter operating in CCM.

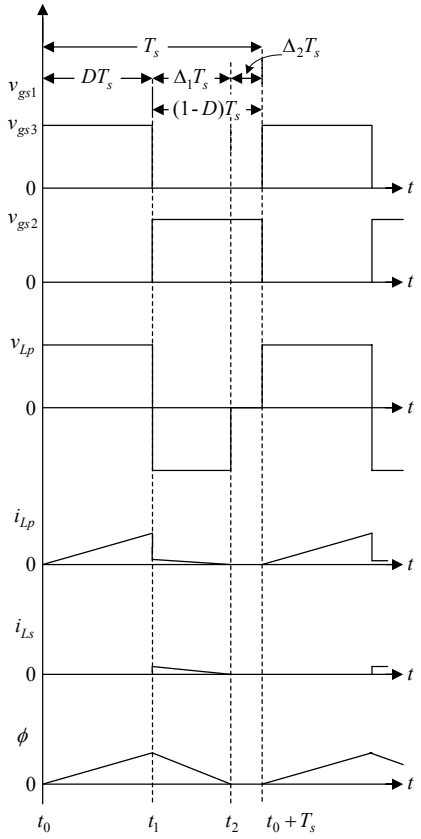


**Fig. 3.** Illustrated waveforms for the converter operating in DCM.

### 3.1 Equivalent coupling inductor parameters

In the proposed converter, the currents in $L_p$ and $L_s$, $i_p$ and $i_s$, are pulsating for any operating mode, due to the discontinuity in $i_p$ and $i_s$. Accordingly, for analysis convenience, some modifications to the parameters and currents of the coupling inductor are presented. First of all, let $L_p$ be $L_1$, and then during the turn-off period of $S_3$, let the equivalent inductance $L_2$ be $L_p$ plus $L_s$, as shown in Fig. 4. Therefore,

$$\begin{cases} L_1 = L_p \\ L_2 = (n+1)^2 L_p = (n+1)^2 L_1 \end{cases} \tag{1}$$

It is noted that how to determine which mode operates in is based on the flux in the central-tapped coupling inductor, $\varphi$, or based on $N_p$, $N_s$, $i_p$ and $i_s$. Also, it is noted that the turns ratio $n$ is equal to $N_s$ divided by $N_p$. Accordingly, the following equations can be obtained :

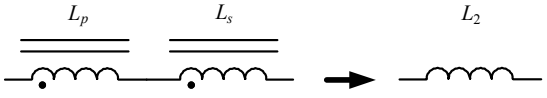


**Fig. 4.** Equivalent inductance $L_2$ equal to $L_p$ plus $L_s$ during the turn-off period.

$$\begin{cases} i_{Lp} = \dfrac{\varphi \times \Re}{N_p} & , \ t_0 < t < t_1 \\ i_{Lp} = \dfrac{\varphi \times \Re}{N_p + N_s} = \dfrac{\varphi \times \Re}{(n+1)N_p} & , \ t_1 < t < t_0 + T_s \end{cases} \tag{2}$$

where $\Re$ is the flux resistance of the core.

Based on the above mention, as shown in Fig. 5, if the number of turns during the magnetizing and demagnetizing periods is $N_p$, then the continuous current $i_{L1}$ can be obtained. Likewise, if the number of turns during the magnetizing and demagnetizing periods is $N_p$ plus $N_s$, then the continuous current $i_{L2}$ can be obtained. The following equations show the results:

$$\begin{cases} i_{L1} = \dfrac{\varphi \times \Re}{N_p} \\ i_{L2} = \dfrac{\varphi \times \Re}{N_p + N_s} = \dfrac{\varphi \times \Re}{(n+1)N_p} \end{cases} \tag{3}$$

From (2) and (3), the relationship between $i_{Lp}$, $i_{L1}$ and $i_{L2}$

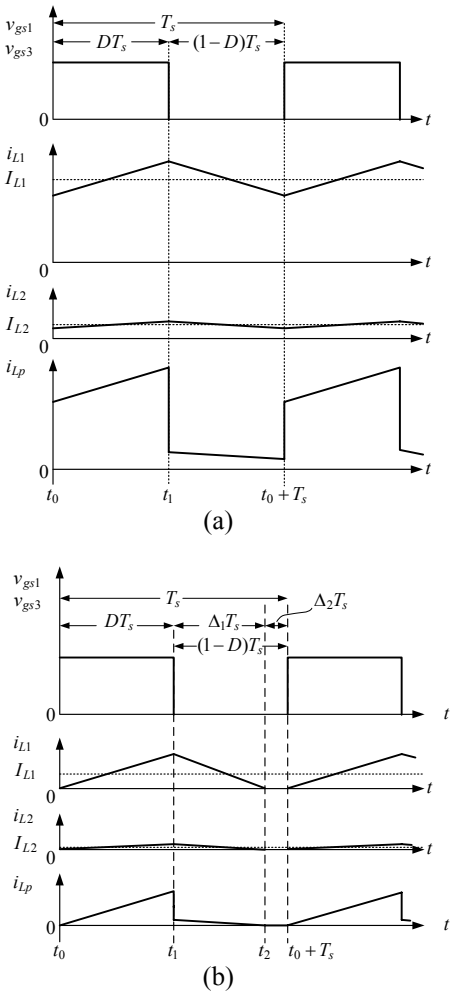


**Fig. 5.** Relationship between $i_{L1}$, $i_{L2}$ and $i_{Lp}$: (a) CCM; (b) DCM.

can be expressed to be

$$\begin{cases} i_{Lp} = i_{L1}, & t_0 < t < t_1 \\ i_{Lp} = i_{L2}, & t_1 < t < t_0 + T_s \end{cases} \tag{4}$$

In addition, in Fig. 5, $I_{L1}$ and $I_{L2}$ are the average currents of $i_{L1}$ and $i_{L2}$, respectively.

And, the relationship between $i_{L1}$ and $i_{L2}$, and the relationship between $I_{L1}$ and $I_{L2}$ can be represented by

$$\begin{cases} i_{L1} = (n+1) i_{L2} \\ I_{L1} = (n+1) I_{L2} \end{cases} \tag{5}$$

### 3.2 Steady-state analysis

After the above modifications mentioned in Sec. 3.1, the steady-state analysis, based on the small ripple approximation, follows.

#### *3.2.1 State 1 ($t_0 < t \le t_1$)*

As shown in Fig. 6, $S_1$ and $S_3$ are turned on but $S_2$ is turned off. During this interval, $D_b$ and $D_o$ are reverse-biased. At the same time, the voltage across $L_p$ is the input voltage plus the voltage across $C_b$, namely, $2V_i$, thereby causing $L_p$ to be magnetized. Also, the energy required by the output is provided by $C_o$. Therefore, the corresponding equations can be obtained to be

$$\begin{cases} v_{Lp} = 2V_i \\ i_{Co} = -\dfrac{V_o}{R_o} \end{cases} \tag{6}$$

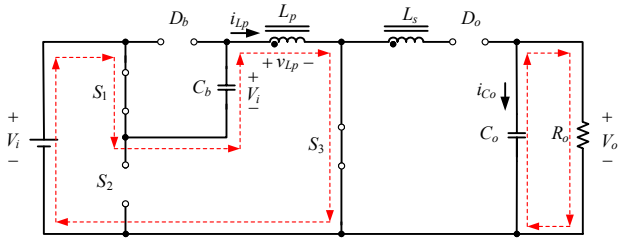


**Fig. 6.** Current flow for mode 1.

#### *3.2.2 State 2 ($t_1 < t \le t_0 + T_s$)*

As shown in Fig. 7, $S_1$ and $S_3$ are turned off but $S_2$ is turned on. During this interval, $D_b$ and $D_o$ are forward-biased. At the same time, the voltage across $L_2$ is the input voltage minus the output voltage, namely, $V_i - V_o$. Hence, the voltage across $L_p$ is equal to $V_i$ minus $V_o$ divided by ($n$+1), thereby causing $L_p$ to be demagnetized. Also, the energy required by the output is provided by the central-tapped coupling inductor which releases the stored energy.

Therefore, the corresponding equations can be obtained based on the small ripple approximation to be

$$\begin{cases} v_{Lp} = \dfrac{v_{L2}}{n+1} = \dfrac{V_i - V_o}{n+1} \\ i_{Co} = i_{Lp} - \dfrac{V_o}{R_o} = i_{L2} - \dfrac{V_o}{R_o} = I_{L2} - \dfrac{V_o}{R_o} \end{cases} \tag{7}$$

By applying the voltage-second balance to $L_p$, one can obtain

$$2V_i D + \frac{V_i - V_o}{n+1}(1-D) = 0 \tag{8}$$

Rearranging (8) yields the voltage conversion ratio:

$$\frac{V_o}{V_i} = \frac{1 + D(2n+1)}{1-D} \tag{9}$$

Applying the current-second balance to $C_o$, one can obtain

$$(-\frac{V_o}{R_o}) + (1-D) I_{L2} = 0 \tag{10}$$

Rearranging (10) yields the expression of $I_{L2}$:

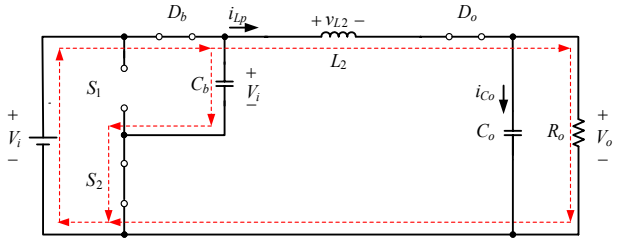


**Fig. 7.** Current flow for mode 2.

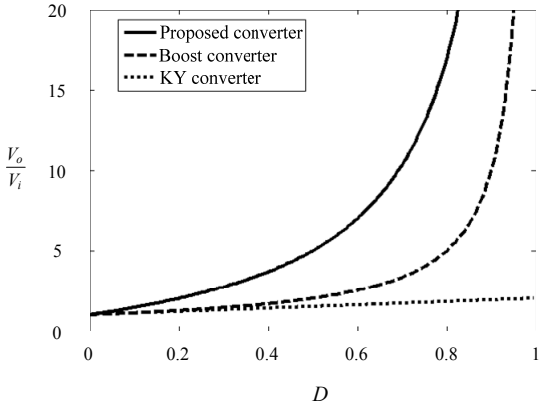


**Fig. 8.** Voltage conversion ratio comparison of three types of converters.

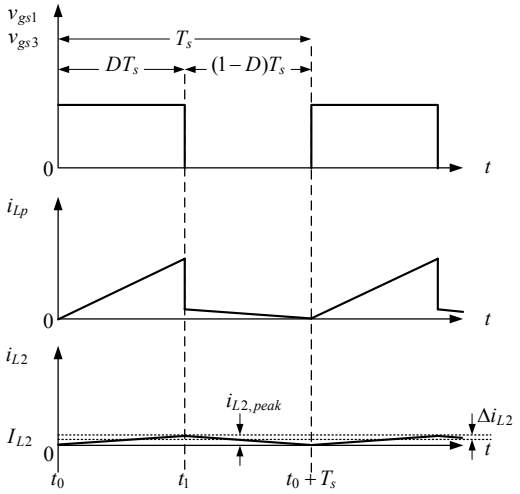


**Fig. 9.** Inductor current waveforms in BCM.

$$I_{L2} = \frac{1}{1-D}\frac{V_o}{R_o} \tag{11}$$

Via (9) under the same duty cycle, it is noted that in Fig. 8, the proposed high step-up converter with a turns ratio set to one has a higher voltage conversion ratio than the other two, the traditional boost converter and the KY converter.

### 3.3 Boundary conduction mode condition

Fig. 9 shows the key waveforms for the converter operating in the boundary conduction mode (BCM). For this mode, the average current flowing through $L_2$, $I_{LB}$, can be expressed to be

$$I_{LB} = \frac{1}{1-D}\frac{V_o}{R_o} \tag{12}$$

From state 2 mentioned in Sec. 3.2, since the current in $L_2$, $i_{L2}$, corresponds to the current flowing through $L_p$ plus $L_s$ during the turn-off period of $S_1$, the half value of $i_{L2,peak}$, $\Delta i_{L2}$, can be expressed to be

$$\begin{aligned}\Delta i_{L2} &= \frac{1}{2} i_{L2,peak} \\ &= \frac{(1-D)T_s}{2L_2}(V_o - V_i)\end{aligned} \tag{13}$$

where $i_{L2,peak}$ is the peak-to-peak value of $i_{L2}$ under BCM.

Substituting (1) into (13) yields

$$\Delta i_{L2} = \frac{(1-D)T_s}{2(n+1)^2 L_p}(V_o - V_i) \tag{14}$$

If $I_{LB}$ is equal to than $\Delta i_{L2}$, then the converter operates in BCM. Accordingly, the following equation can be obtained to be

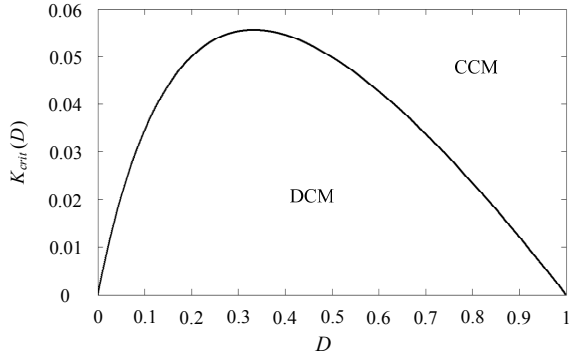


**Fig. 10.** Boundary condition of the proposed converter with turns ratio n equal to one.

$$\begin{aligned} & I_{LB} = \Delta i_{L2} \\ \Rightarrow & \frac{1}{(1-D)R_o}V_o = \frac{(1-D)T_s}{2(n+1)^2 L_p}(V_o - V_i) \\ \Rightarrow & \frac{L_p}{R_o T_s} = \frac{D(1-D)^2}{(n+1)[1+D(2n+1)]} \end{aligned} \tag{15}$$

Let

$$\begin{cases} K = \dfrac{L_p}{R_o T_s} \\ K_{crit}(D) = \dfrac{D(1-D)^2}{(n+1)[1+D(2n+1)]} \end{cases} \tag{16}$$

Substituting (16) into (15), (15) can be rewritten to be

$$K = K_{crit}(D) \tag{17}$$

Based on (17), if $K < K_{crit}(D)$, then the converter will operate in DCM; if $K > K_{crit}(D)$, then the converter will operate in CCM. Fig. 10 shows the boundary condition of the proposed converter with turns ratio $n$ equal to one.

### 3.4 Passive clamping snubber

As generally recognized, the central-tapped coupling inductor inherently has the leakage inductance $L_{LK}$, since the coupling coefficient is not equal to one. Therefore, the voltage spike will be imposed on the switch. In the case, a passive clamping snubber, composed of one snubber diode $D_{sn}$ and one snubber capacitor $C_{sn}$, is used herein to suppress such a voltage spike. Fig. 11 shows the proposed converter with this passive clamping snubber. There are two operating states for the passive clamping snubber, to be described briefly as follows.

#### *3.4.1 State 1*

As $S_3$ is turned off, the energy stored in $L_{LK}$ forces $D_{sn}$ and $D_o$ to be turned on, as shown in Fig. 11. At the same time, $C_{sn}$ is charged. As soon as the energy stored is

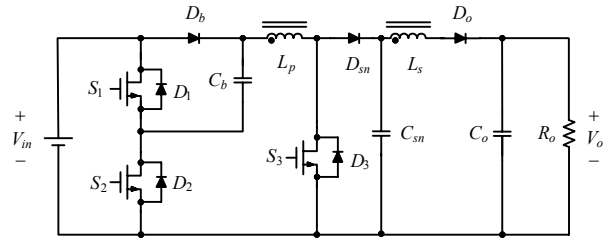


**Fig. 11.** Proposed converter with a passive clamping snubber.

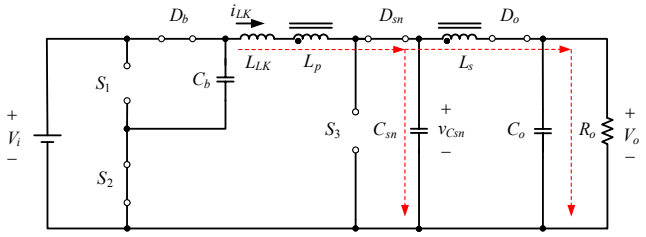


**Fig. 12.** Current flow of the passive clamping snubber in state 1.

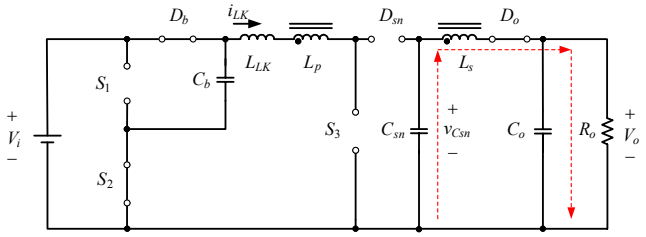


**Fig. 13.** Current flow of the passive clamping snubber in state 2.

released entirely, the operating state goes to state 2.

#### *3.4.2 State 2*

As $D_{sn}$ is turned off and $D_o$ is turned on, $C_{sn}$ is discharged as shown in Fig. 13. As soon as the voltage across $C_{sn}$, $v_{Csn}$, is reduced to the minimum value, $v_{Csn,min}$, which is equal to $V_i + \frac{V_o - V_i}{n+1}$, $D_{sn}$ is turned on, and this state comes to the end.

Fig. 14 shows the overall system configuration of the proposed converter. The feedback control loop contains one voltage divider, one analog-to-digital converter (ADC), one FPGA which is the control kernel, and three gate drivers. Besides, the gate driving signals $M_1$, $M_2$ and $M_3$ are created by FPGA and used to drive the switches $S_1$, $S_2$ and $S_3$, respectively, after gate drivers.

Prior to designing the main power stage in Fig. 14, there are some specifications to be given as follows: (i) the input voltage $V_i$ is 5V; (ii) the output voltage $V_o$ is 48V; (iii) the rated output current $I_{o,rated}$ is 1A; (iv) the minimum output current $I_{o,min}$ is 0.15A, which makes the converter operate in BCM; (v) the switching frequency $f_s$ is 50kHz; and (vi) the turns ratio is five.

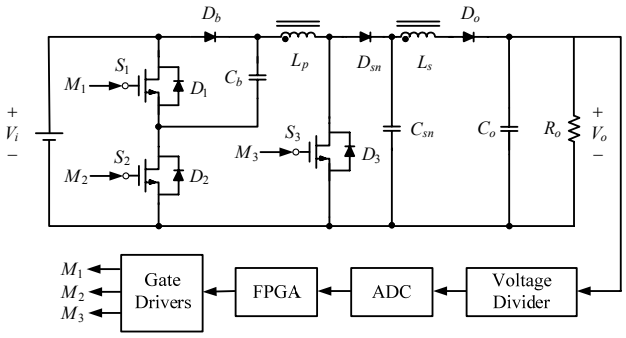


**Fig. 14.** Overall system configuration.

### 3.5 Design of coupling inductor

According to the above specifications, the calculated duty cycle $D$ can be obtained to be 0.417 as follows:

$$D = \frac{\frac{V_o}{V_i} - 1}{2n + 1 + \frac{V_o}{V_i}} = \frac{\frac{48}{5} - 1}{(2 \times 5) + 1 + \frac{48}{5}} \cong 0.417 \tag{18}$$

From the mention at the end of Sec. 3.3, if the converter operates in CCM above the minimum output current $I_{o,min}$, the primary-side inductance of the coupling inductor $L_p$ must satisfy the following inequality:

$$\begin{aligned} L_p &\geq \frac{D(1-D)^2}{(n+1)[1+D(2n+1)]} R_{o,max} T_s \\ \Rightarrow L_p &\geq \frac{D(1-D)^2}{(n+1)[1+D(2n+1)]} \frac{V_o}{I_{o,min}} \frac{1}{f_s} \end{aligned} \tag{19}$$

Substituting the given specifications into (19), the value of $L_p$ is calculated to be larger than 27.06μH:

$$\begin{aligned} L_p &\geq \frac{0.417(1-0.417)^2}{(5+1)[1+0.417(2\times 5+1)]} \frac{48}{0.15} \frac{1}{50\times 10^3} \\ \Rightarrow L_p &\geq 27.06\,\mu\text{H} \end{aligned} \tag{20}$$

Finally, the value of $L_p$ is chosen to be about 30μH. At the same time, the value of the secondary-side inductance $L_s$ is calculated to be 750μH, as shown in the following equation:

$$L_s = n^2 L_p = 5^2 \times 30 \times 10^{-6} = 750\,\mu\text{H} \tag{21}$$

Eventually, one PTS40/27/I 3C92 core, made by Ferroxcube Co., is chosen for the coupling inductor.

### 3.6 Design of charge pump capacitor

According to the basic formula for the capacitor, the

relationship between voltage ripple and capacitance during the discharge interval $\Delta t$ can be expressed to be

$$\Delta v_{Cb} = i_{Cb} \frac{\Delta t}{C_b} \tag{22}$$

where $\Delta v_{Cb}$ is the voltage ripple on $C_b$ and $i_{Cb}$ is the current flowing through $C_b$.

Under the rated conditions, the average current during the turn-on period, $I_{Cb,DTs}$ is equal to $I_{L1,rated}$, namely

$$\Delta v_{Cb,max} = I_{Cb,DTs} \frac{DT_s}{C_b} = I_{L1,rated} \frac{DT_s}{C_b} \tag{23}$$

where $\Delta v_{Cb,max}$ is the maximum value of $\Delta v_{Cb}$.

If $\Delta v_{Cb,max}$ is smaller than 3% of $V_i$, then the inequality of the value of $C_b$ can be obtained as follows:

$$\begin{aligned} 5\times 3\% > \Delta v_{Cb,max} &\Rightarrow 0.15 > I_{L1,rated} \frac{DT_s}{C_b} \\ &\Rightarrow C_b > I_{L1,rated} \frac{DT_s}{0.15} \\ &\Rightarrow C_b > (n+1)(\frac{1}{1-D}) I_{o,rated} \frac{D}{0.15\times f_s} \\ &\Rightarrow C_b > 572\,\mu\text{F} \end{aligned} \tag{24}$$

Eventually, one 680μF Rubycon capacitor is chosen for $C_b$.

### 3.7 Design of output capacitor

By the same way mentioned in Sec. 3.6, under the rated conditions, the average current during the turn-on period, $I_{Co,DTs}$ is equal to $I_o$, namely

$$\Delta v_{Co,max} = I_{Co,DTs} \frac{DT_s}{C_o} = I_{o,rated} \frac{DT_s}{C_o} \tag{25}$$

where $\Delta v_{Co,max}$ is the maximum value of $\Delta v_{Co}$.

If $\Delta v_{Co,max}$ is smaller than 0.2% of $V_i$, then the inequality of the value of $C_o$ can be obtained as follows:

$$\begin{aligned} &48\times 0.2\% > \Delta v_{Co,max} \\ &\Rightarrow 0.096 > I_{o,rated} \frac{DT_s}{C_o} \\ &\Rightarrow C_o > I_{o,rated} \times \frac{D}{0.096\times f_s} \\ &\Rightarrow C_o > 869\,\mu\text{F} \end{aligned} \tag{26}$$

Finally, one 1000μF Rubycon capacitor is chosen for $C_o$.

### 3.8 Design of $C_{sn}$ in passive snubber

Prior to taking up this section, the primary-side leakage inductance $L_{LK}$ must be figured out first, the data shown in Table 1 is obtained based on a LCR meter, and hence the coupling coefficient of the primary side to the secondary side, $k_{ps}$, can be obtained to be

**Table 1.** Measurements of the central-tapped coupling inductor

| | |
|---|---|
| $N_p$ | 6Turns |
| $N_s$ | 30Turns |
| $L_p$ with the secondary side opened | 29.8μH |
| $L_{p\_s\text{-}short}$ with the secondary side shorted | 0.16μH |
| $L_s$ with the primary side opened | 746μH |
| $L_{s\_s\text{-}short}$ with the primary side shorted | 5.5μH |

$$k_{ps} = \sqrt{1-\frac{L_{p\_s-short}}{L_p}} = \sqrt{1-\frac{0.16}{29.8}} \cong 0.997 \tag{27}$$

By the similar way, the coupling coefficient of the secondary side to the primary side, $k_{sp}$ can be obtained:

$$k_{sp} = \sqrt{1-\frac{L_{s\_p-short}}{L_s}} = \sqrt{1-\frac{5.5}{746}} \cong 0.996 \tag{28}$$

Hence, the coupling coefficient of the central-tapped coupling inductor, $k$, can be calculated out to be

$$k = \sqrt{0.997\times 0.996} \cong 0.996 \tag{29}$$

Accordingly, the primary-side leakage inductance $L_{LK}$ can be worked out to be

$$L_{LK} = (1-k)L_p = (1-0.996)\times 29.8\times 10^{-6} \cong 0.12\,\mu\text{H} \tag{30}$$

Sequentially, the value of the snubber capacitor $C_{sn}$ will be calculated out in the following. Under the condition that the converter operates at rated load, as soon as $S_1$ is turned off, the energy stored in $L_{LK}$ can be expressed to be

$$E_{LK} = \frac{1}{2} L_{LK} I_{Lp,max}^2 \tag{31}$$

where

$$\begin{aligned} I_{Lp,max} &= I_{L1,max} \\ &= (n+1) I_{L2,max} \\ &= (n+1)[\frac{1}{1-D} I_{o,rated} + \frac{(1-D)}{2(n+1)^2 L_p f_s}(V_o - V_i)] \\ &\cong 11.68\text{A} \end{aligned} \tag{32}$$

Based on the (31) and (32), the value of $E_{LK}$ is $8.19\,\mu\text{J}$.

Since $E_{LK}$ is to be released to $C_{sn}$ from the minimum voltage across $C_{sn}$, $v_{Csn,min}$, to the maximum voltage across $C_{sn}$, $v_{Csn,max}$, $E_{LK}$ also can be expressed to be

$$E_{LK} = \frac{1}{2} C_{sn} (v_{Csn,\max}^2 - v_{Csn,min}^2) \quad (33)$$

Also,

$$v_{Csn,min} = V_i + \frac{V_o - V_i}{n+1} = 5 + \frac{48-5}{5+1} \cong 12.17\text{V} \quad (34)$$

Assuming that $v_{Csn,max}$ is smaller than 20V, substituting the calculated values of $E_{LK}$ and $v_{Csn,max}$ into (33), the inequality of the value of $C_{sn}$ can be obtained as follows:

$$C_{sn} \geq \frac{2E_{LK}}{(v_{Csn,\max}^2 - v_{Csn,min}^2)} = \frac{2 \times 8.19 \times 10^{-6}}{20^2 - 12.17^2} \cong 65\,\text{nF} \quad (35)$$

Finally, one 68nF ceramic capacitor is chosen for $C_{sn}$.

## 4. Experimental Results

At light load, Fig. 15 shows the gate driving signals $v_{gs1}$, $v_{gs2}$ and $v_{gs3}$ for $S_1$, $S_2$ and $S_3$, respectively, and the voltage across $C_b$, $v_{Cb}$; Fig, 16 shows the gate driving signals $v_{gs1}$ and $v_{gs2}$ for $S_1$ and $S_2$, respectively, the current through $L_p$, $i_{Lp}$, and the current through $L_s$, $i_{Ls}$; Fig. 17 shows the gate driving signals $v_{gs1}$ and $v_{gs2}$ for $S_1$ and $S_2$, respectively, the voltage across $S_3$, and the voltage across $D_{sn}$. At half load, Figs. 18 to 20 show the same measured items as Figs. 15 to 17; at rated load, Figs. 21 to 23 show the same measured items as Figs. 15 to 17. In addition, Fig. 24 shows the curves of efficiency versus load current, with and without a passive snubber.

From Figs. 15, 18 and 21, it can be seen that the voltages across the energy-transferring capacitor $C_b$ are kept near at 5V. The differences between them are due to the voltage drops of parasitic components. From Figs. 16, 19 and 22, it can be seen that the more the load is, the higher the currents $i_{Lp}$ and $i_{Ls}$. From Figs. 17, 20 and 23, it can be seen that the more the load is, the higher the voltage spike, particularly at rated load, up to 20V. From Fig. 24, it can be seen that the efficiency is above 90.38% all over the load range and can be up to 92.29%. Besides, the efficiency below the load current of 0.4A, the converter with the passive snubber has lower efficiency than the converter without the passive snubber. This is because the former has

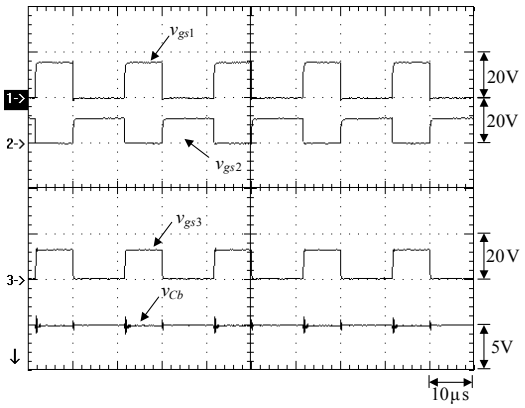


**Fig. 15.** Measured waveforms at light load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{gs3}$; (4) $v_{Cb}$.

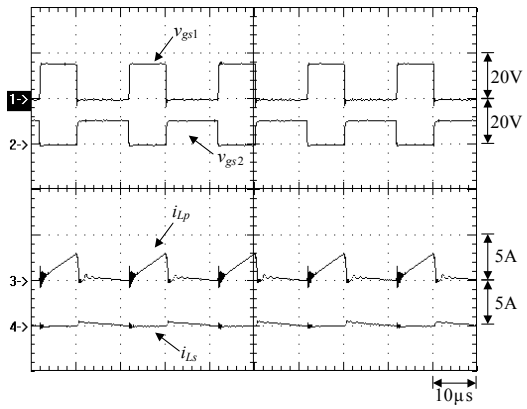


**Fig.16.** Measured waveforms at light load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $i_{Lp}$; (4) $i_{Ls}$.

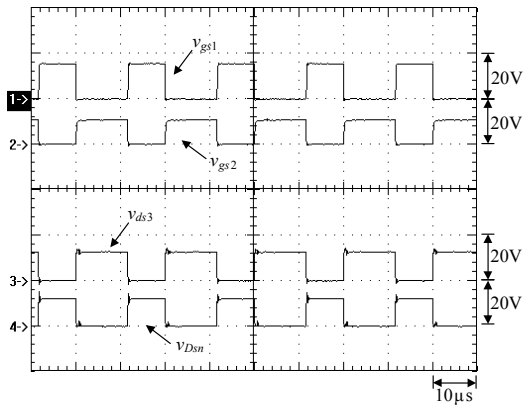


**Fig. 17.** Measured waveforms at light load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{ds3}$; (4) $v_{Dsn}$.

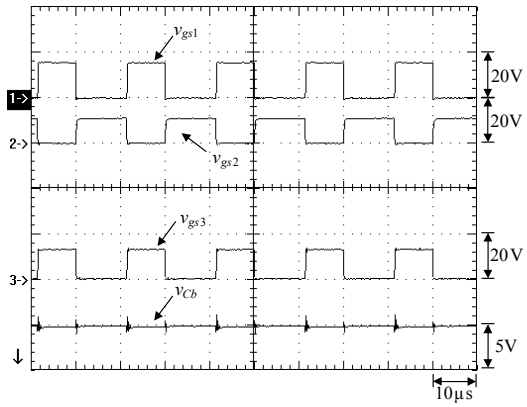


**Fig. 18.** Measured waveforms at half load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{gs3}$; (4) $v_{Cb}$.

additional conduction loss due to the diode $D_{sn}$. However, as the load is from light load to rated load, the former has better performance of efficiency than the latter. This is because the voltage stress in the former is lower than that in the latter. Hence, the turn-on resistance of the switch $S_3$ of the former is lower than that of the latter, implying that the former has lower conduction loss than the latter.

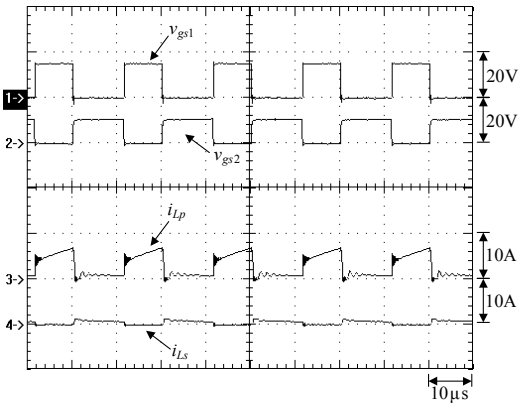


**Fig. 19.** Measured waveforms at half load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $i_{Lp}$; (4) $i_{Ls}$.

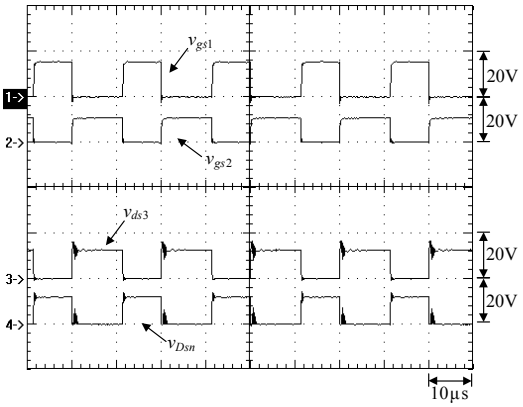


**Fig. 20.** Measured waveforms at half load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{ds3}$; (4) $v_{Dsn}$.

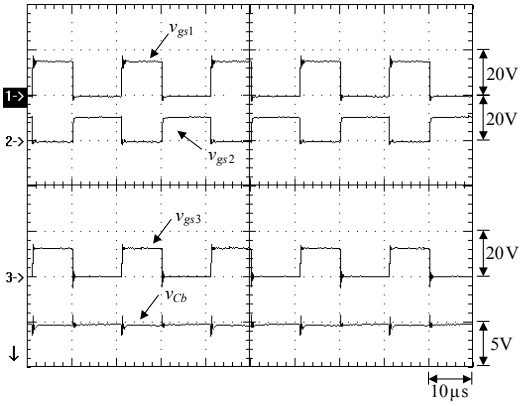


**Fig. 21.** Measured waveforms at rated load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{gs3}$; (4) $v_{Cb}$.

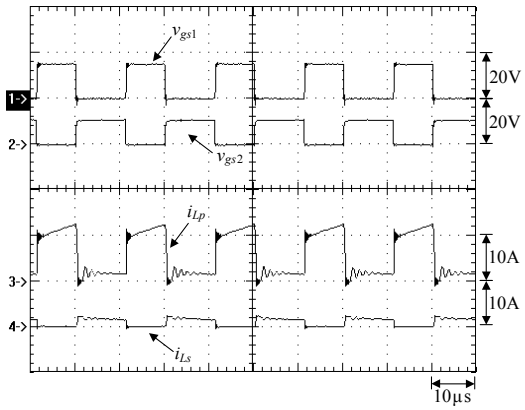


**Fig. 22.** Measured waveforms at rated load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $i_{Lp}$; (4) $i_{Ls}$.

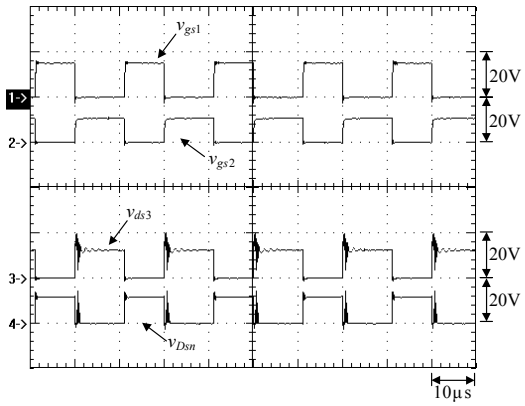


**Fig. 23.** Measured waveforms at rated load: (1) $v_{gs1}$; (2) $v_{gs2}$; (3) $v_{ds3}$; (4) $v_{Dsn}$.

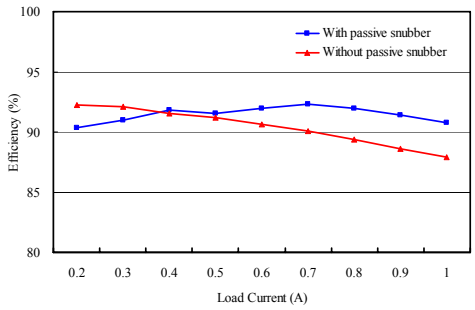


**Fig. 24.** Efficiency versus load.

## 5. Conclusion

A novel step-up converter is presented herein, which is based on coupling inductor and one central-tap coupling inductor so as to improve the voltage conversion ratio of the KY converter. In the proposed converter, a passive clamping snubber is used to decrease the voltage spike on the switch so as to increase the efficiency of this converter above half load. Besides, such a converter is simple in structure and easy to control, and hence suitable for

**Table 3.** Comparison between the proposed converter and the converters shown in the References, in terms of voltage conversion ratio, component number, switch voltage stress, output inductor and floating output

| Ref. | Voltage conversion ratio | Component number | Switch voltage stress | Output inductor | Floating output |
|---|---|---|---|---|---|
| [3] | $\frac{1}{(1-D)^2}$ | 8 | $V_{ds1}=\frac{V_i}{1-D}$, $V_{ds2}=V_{ds3}=\frac{V_i}{(1-D)^2}$ | No | No |
| [4] | $\frac{1+n}{1-D}$ | 10 | $V_{ds1}=nV_i$, $V_{ds2}=\frac{nD}{1-D}V_i$ | No | No |
| [5] | $\frac{2+n}{1-D}$ | 10 | $V_{ds1}=\frac{V_i}{1-D}$ | No | No |
| [6] | $\frac{1+n}{1-D}$ | 15 | $V_{ds1}=\frac{V_i}{1-D}$ | No | No |
| [7] | $\frac{2}{1-D}+nD$ | 13 | $V_{s1}=V_{s2}=\frac{V_o}{2}-\frac{nDV_i}{2}$ | No | No |
| [8] | $\frac{1+D+nD}{1-D}$ | 9 | $V_{ds1}=\frac{V_i}{1-D}$ | No | Yes |
| [9] | $\frac{2(1+nD)}{1-D}$ | 10 | $V_{ds1}=\frac{1+nD}{1-D}V_i$ | No | Yes |
| [10] | $\frac{2+nD}{1-D}$ | 14 | $V_{ds1}=\frac{V_i}{1-D}$ | No | No |
| [11] | $1+D$ | 6 | $V_{ds1}=2V_i$, $V_{ds2}=V_i$ | Yes | No |
| [12] | $\frac{2-D}{1-D}$ | 8 | $V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$ | Yes | No |
| [13] | $\frac{2-D}{1-D}$ | 8 | $V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$ | Yes | No |
| [14] | $\frac{2}{1-D}+n$ | 8 | $V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$ | No | No |
| [15] | Type 1: $\frac{3-D}{1-D}$<br>Type 2: $\frac{2}{1-D}$<br>Type 3: $\frac{3-2D}{1-D}$ | 10 | Type 1: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{1+D}{1-D}V_i$<br>Type 2: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{1+D}{1-D}V_i$<br>Type 3: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{2-D}{1-D}V_i$ | No | No |
| [16] | $\frac{2nD}{1-D}+1$ | 11 | $V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=(\frac{3D-1}{1-D})V_i$ | No | No |
| [17] | Type 1: 2D<br>Type 2: 2D | 8 | Type 1: $V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=V_i$, $V_{ds4}=V_i$<br>Type 2: $V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=V_i$, $V_{ds4}=V_i$ | Yes | No |
| [18] | $\frac{n+1}{1-D}$ | 10 | $V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$ | No | No |
| [19] | $\frac{2n+1}{1-D}$ | 11 | $V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$ | No | No |
| Proposed | $\frac{2+n-D}{(1-D)^2}$ | 10 | $V_{ds1}=[\frac{2+n-D}{(1-D)^2}]V_i$ | No | No |

industrial applications.

## Appendix

Table 2 makes a comparison between some converters shown in the references in terms of voltage conversion ratio, component number, and switch voltage stress. From this table, it can be seen that the proposed converter a relatively good voltage conversion ratio with a reasonable component number and acceptable switch voltage stresses.

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