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High Step-Up Converter with Hybrid Structure Based on One Switch

K. I. Hwu† and T. J. Peng*

Abstract – A novel high step-up converter is presented herein, which combines the conventional buck-boost converter, the charge pump capacitor and the coupling inductor. By doing so, a quite high voltage conversion ratio due to not only the turns ratio but also the duty cycle, so as to increase design feasibility. It is noted that the denominator of the voltage conversion ratio is the square of one minus duty cycle. Above all, there is no voltage spike across the switch due to the leakage inductance and hence no passive or active snubber is needed, and furthermore, the used switch is driven without isolation and hence the gate driving circuit is relatively simple, thereby upgrading the industrial application capability of this converter. In this paper, the basic operating principles and the associated mathematical deductions are firstly described in detail, and finally some experimental results are provided to demonstrate the effectiveness of the proposed high step-up converter.

Keywords: High step-up converter, Charge pump, Coupling inductor, One switch

1. Introduction

As generally recognized, the boost converter is widely used in the renewable energy system, in the standby power source, in the car power source, in the 3C (Computer, Communication, Consumer-Electronics) product, etc. The purpose of the boost converter is used to transfer the low voltage level to the stable high voltage level, so as to stabilize the overall system. Therefore, the traditional boost converter is used as a power stage, which boosts the input voltage to a 400V dc voltage to feed the standby power source, or to generate a grid-connected 220V ac voltage via the DC-AC inverter. However, the traditional boost converter has the voltage conversion ratio about four. This is because the non-ideal properties due to parasitic components make the voltage conversion ratio deteriorated [1, 2].

Consequently, many kinds of voltage-boosting techniques have been presented, including several inductors which are magnetized and then pump the stored energy into the output with all inductors connected in series [3], coupled inductors with turns ratios [4-8, 9, 10, 14, 18, 19], voltage superposition based on switching capacitors [12-17], auxiliary transformers with turns ratios [11], etc. In [8] and [9], the output terminal is floating, thereby increasing application complexity. In [6, 7] and [10], these converters contain too many components, thereby making the converters relatively complicated. In [3-10, 14-16, 18] and [19], the output currents are pulsating, thus causing the output voltage ripples to tend to be large. In [11-13] and [17], even though the output currents are non-pulsating, their voltage conversion ratios are not high enough.

Therefore, a novel high step-up converter is presented herein, which combines the traditional buck-boost converter, the charge pump and the coupling inductor. This converter possesses relatively high voltage conversion ratio, the designer can use the turns ratio to vary the voltage conversion ratio so as to make the circuit design relatively elastic. Above all, the used power switch is not floating, so as to make the gate driving circuit quite simple. Furthermore, there is no voltage spike across the switch due to the leakage inductance. In this paper, the basic operating principles and the associated mathematical deductions are firstly depicted in detail, and eventually some experimental results are provided to verify the effectiveness of the proposed high step-up converter.

2. Overall System Configuration

Fig. 1 shows the proposed high step-up converter, which is constructed by the traditional buck-boost converter, and the coupling inductor and charge pump capacitor circuit. The traditional buck-boost converter contains one switch S_1, two diodes D_1 and D_4, one inductor L_1, and one energy-

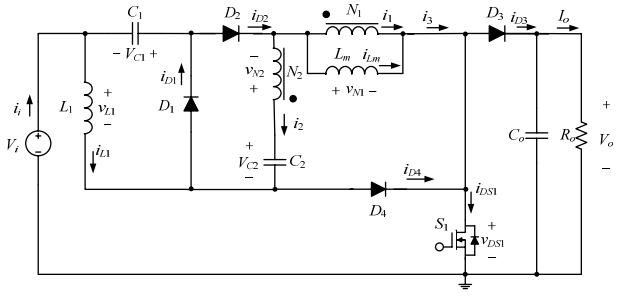

Fig. 1. Proposed high step-up converter with variables added.

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transferring capacitor C_1. The coupling inductor and charge pump capacitor circuit contains one switch S_1, three diodes D_2, D_3 and D_4, one charge pump capacitor C_2, one output capacitor C_o, and one coupling inductor with turns ratio of N_1:N_2, where N_1 and N_2 are the primary-side turns and the secondary-side turns, respectively. It is noted that the coupling inductor is built up by one magnetizing inductor L_m and one ideal transformer.

3. Basic Operating Principles

Prior to taking up this section, there are some assumptions and symbols to be given as follows in Fig. 1: (i) the coupling coefficient k is equal to one, that is, the primary and secondary leakage inductances are negligible; (ii) the dc input and output voltages are defined to be V_i and V_o, respectively; (iii) the dc input and output currents are signified by I_i and I_o, respectively; (iv) the current in S_1 is indicated by i_{DS1}; (v) the currents in D_1, D_2, D_3 and D_4 are denoted by i_{D1}, i_{D2}, i_{D3} and i_{D4}, respectively; (vi) the values of C_1 and C_2 are large enough to keep the voltages across themselves constant at some values, equal to V_{C1} and V_{C2}, respectively; (vii) the current flowing through L_1 is expressed by i_{L1}; (viii) the currents in the N_1 and N_2 windings are signified by i_1 and i_2, respectively; (ix) the current in L_m is indicated by i_{Lm}; (x) i_3 is the sum of i_1 and i_m; (xi) the gate driving signal for S_1 is denoted by v_{gs1}; (xii) the voltages on S_1 is represented by v_{DS1}; (xiii) the voltage across L_1 is expressed by v_{L1}; (xiv) the voltage across L_m or the voltage across the N_1 winding is expressed by v_{N1}; (xv) the voltage on the N_2 winding indicated by v_{N2}; (xvi) the turns ratio of n is equal to N_2/N_1; and (xvii) the duty cycle D is the quiescent dc duty cycle created from the controller.

3.1 CCM Operation

Since the converter operates in the continuous conduction mode (CCM), there are two operating states with the illustrated waveforms as shown in Fig. 2.

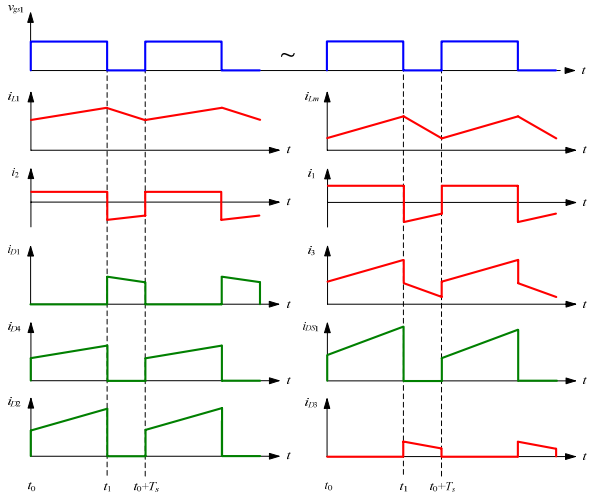


Fig. 2. Illustrated waveforms related to the proposed converter.

3.1.1 *State 1* ($t_0 \le t \le t_1$)

As shown in Fig. 3(a), S_1 is turned on. Hence, the voltage across L_1 is equal to V_i, thereby causing L_1 to be magnetized. At the same time, D_1 and D_3 are turned off, but D_2 and D_4 are turned on. Accordingly, the voltage across L_m, v_{N1}, is equal to the input voltage V_i plus the voltage across C_1, V_{C1}, thereby causing L_m to be magnetized. In addition, C_2 is charged by $V_i + V_{C1} + v_{N2}$. Therefore,

$$\begin{cases} v_{L1} = V_i \\ v_{N1} = V_{C1} + V_i \end{cases} \tag{1}$$

3.1.2 *State 2* ($t_1 \le t \le t_0 + T_s$)

As shown in Fig. 3(b), S_1 is turned off. Hence, D_2 and D_4 are turned off, but D_1 and D_3 are turned on. At the same time, the voltage across L_1, v_{L1}, is equal to $-V_{C1}$, thereby causing L_1 to be demagnetized and to energize the output, whereas the voltage across L_m, v_{N1}, is equal to $V_i + V_{C1} + V_{C2} - v_{N2} - V_o$, thereby causing L_m to be demagnetized. Therefore,

$$\begin{cases} v_{L1} = -V_{C1} \\ v_{N1} = -v_{N2} + V_{C2} + V_{C1} + V_i - V_o \end{cases} \tag{2}$$

Since the turns ratio n is equal to N_2/N_1, (2) can be rewritten to be

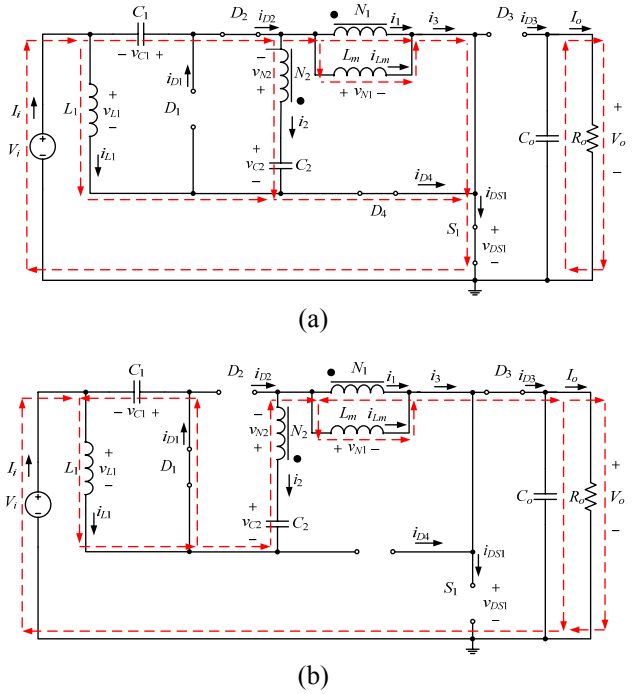


Fig. 3. Current flows in: (a) state 1; (b) state 2.

$$\begin{cases} v_{L1} = -V_{C1} \\ v_{N1} = \dfrac{V_{C2} + V_{C1} + V_i - V_o}{1+n} \end{cases} \tag{3}$$

Applying the voltage-second balance to L_1, we can obtain the following equation:

$$V_i \times D + (-V_{C1}) \times (1-D) = 0 \tag{4}$$

Eq. (4) can be rewritten to be

$$V_{C1} = \frac{D}{1-D} \times V_i \tag{5}$$

By applying the voltage-second balance to L_m, we can obtain the following equation:

$$(V_{C1} + V_i) \times D + \frac{V_{C2} + V_{C1} + V_i - V_o}{1+n} \times (1-D) = 0 \tag{6}$$

where

$$V_{C2} = (1+n) \times (V_i + V_{C1}) \tag{7}$$

Substituting (5) and (7) into (6) yields the voltage conversion ratio of the proposed high step-up converter:

$$\frac{V_o}{V_i} = \frac{2+n-D}{(1-D)^2} \tag{8}$$

3.2 Comparison of flyback, forward and proposed converters

As generally acknowledged, the duty cycle of the flyback converter does not approach to one due to the parasitic parameters of components, whereas the duty cycle of the forward converter also does not approach to one due to a suitable time slot needed to reset the magnetizing inductance. Based on the aforementioned, the comparison in voltage conversion ratio between the flyback converter, the forward converter and the proposed converter is under the condition that each converter operates in the continuous conduction mode (CCM) with the turns ratio set to 3 and the duty cycle set at 0.75. Therefore, the voltage conversion ratios for the flyback converter, the forward converter and the proposed converter are 2.25, 9, and 68, respectively. That is, the proposed converter has a quite high voltage conversion ratio as compared with the flyback converter and forward converter.

3.3 CCM with leakage inductance considered

By considering the leakage inductance L_{lk} as shown in Fig. 4, in state 1, the corresponding equation of v_{N1} expressed by (1) will be modified to

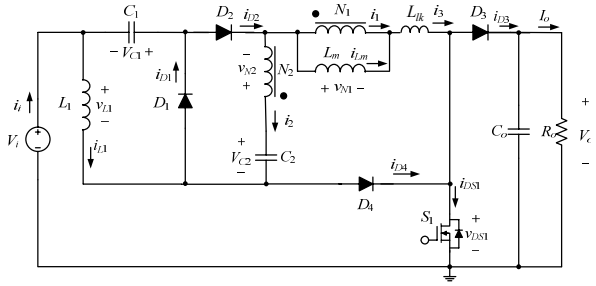


Fig. 4. Proposed high step-up converter with leakage inductance considered.

$$v_{N1} = (V_i + V_{C1}) \times \frac{L_m}{L_m + L_{lk}} = k(V_i + V_{C1}) \tag{9}$$

where $k=L_m/(L_m+L_{lk})$.

And, in state 2, the corresponding equation of v_{N1} will be modified to

$$\begin{aligned} v_{N1} &= (-V_{N2} + V_{C2} + V_{C1} + V_i - V_o) \times \frac{L_m}{L_m + L_{lk}} \\ &= k[\frac{(L+nk)(V_{C1} + V_i) - V_o}{1+n}] \end{aligned} \tag{10}$$

By applying the voltage balance to the magnetizing inductor based on (9) and (10), the resulting voltage conversion ratio can be obtained to be

$$\frac{V_o}{V_i} = \frac{2+n(D+k-Dk)-D}{(1-D)^2} \tag{11}$$

From (11), as the value of k is close to one, the voltage conversion ratio is retrieved to (8).

3.3 BCM operation

Since there are two inductors L_1 and L_m in the proposed high step-up converter, the corresponding boundary conduction mode (BCM) conditions will be discussed in the following, so as to make design of L_1 and L_m relatively easy. It is assumed that there is no power loss, i.e., the input power is equal to the output power.

3.3.1 BCM Condition for L_1

Based on (8), the dc input current I_i can be expressed as

$$I_i = \frac{2+n-D}{(1-D)^2} \times I_o \tag{9}$$

where

$$I_o = \frac{V_o}{R_o} \tag{10}$$

Substituting (10) into (9) yields

$$I_i = \frac{2+n-D}{(1-D)^2} \times \frac{V_o}{R_o} \tag{11}$$

Since the dc current in L_1, I_{L1}, is equal to I_i, (11) can be rewritten to be

$$I_{L1} = \frac{2+n-D}{(1-D)^2} \times \frac{V_o}{R_o} \tag{12}$$

Also, the current ripple of i_{L1}, denoted by Δi_{L1}, can be expressed to be

$$\Delta i_{L1} = \frac{v_{L1}\Delta t}{L_1} = \frac{V_i D T_s}{L_1} \tag{13}$$

Hence, the condition for L_1 operating in BCM is

$$\begin{aligned} & 2I_{L1} = \Delta i_{L1} \\ \Rightarrow & \frac{2\times(2+n-D)}{(1-D)^2}\frac{V_o}{R_o} = \frac{V_i D T_s}{L_1} \\ \Rightarrow & \frac{2L_1}{R_o T_s} = D\left(\frac{(1-D)^2}{2+n-D}\right)^2 \\ \Rightarrow & K_1 = K_{crit1}(D) \end{aligned} \tag{14}$$

where

$$K_1 = \frac{2L_1}{R_o T_s} \tag{15}$$

and

$$K_{crit1}(D) = D\left(\frac{(1-D)^2}{2+n-D}\right)^2 \tag{16}$$

Thus, if K_1 is larger than $K_{crit1}(D)$, then L_1 operates in CCM; if K_1 is smaller than $K_{crit1}(D)$, then L_1 operates in DCM.

3.3.2 BCM Condition for L_m

The dc portion of the current in the magnetizing inductor L_m, denoted by I_{Lm}, can be represented by

$$I_{Lm} = \frac{1+n}{1-D} \times I_o \tag{17}$$

Substituting (10) into (17) yields

$$I_{Lm} = \frac{1+n}{1-D} \times \frac{V_o}{R_o} \tag{18}$$

Also, the current ripple of i_{Lm}, denoted by Δi_{Lm}, can be expressed to be

$$\Delta i_{Lm} = \frac{v_{N1}\Delta t}{L_m} = \frac{(V_{C1}+V_i)\times D T_s}{L_m} \tag{19}$$

Substituting (5) into (19) yields

$$\Delta i_{Lm} = \frac{D\times V_i \times T_s}{(1-D)\times L_m} \tag{20}$$

Hence, the condition for L_m operating in BCM is

$$\begin{aligned} & 2I_{Lm} = \Delta i_{Lm} \\ \Rightarrow & 2\left(\frac{1+n}{1-D}\times\frac{V_o}{R_o}\right) = \frac{D\times V_i \times T_s}{(1-D)\times L_m} \\ \Rightarrow & \frac{2(1+n)L_m}{R_o T_s} = \frac{D(1-D)^2}{2+n-D} \\ \Rightarrow & K_2 = K_{crit2}(D) \end{aligned} \tag{21}$$

$$K_2 = \frac{2(1+n)L_m}{R_o T_s} \tag{22}$$

$$K_{crit2}(D) = \frac{D(1-D)^2}{2+n-D} \tag{23}$$

Accordingly, K_2 is larger than $K_{crit2}(D)$, then L_m operates in CCM; if K_2 is smaller than $K_{crit1}(D)$, then L_m operates in DCM.

3. Design Considerations

Prior to taking up this section, there are some system specifications and key components to be given as follows: (i) the range of the dc input voltage V_i is from 20V to 28V with 24V rated; (ii) the rated dc output voltage V_o is 400V; (iii) the rated dc output power $P_{o,rated}$ is 200W, i.e., the rated dc output current $I_{o,rated}$ is 0.5A; (iv) the minimum dc output power $P_{o,min}$ is 40W, i.e., the minimum dc output current $I_{o,min}$ is 0.1A; (v) the switching frequency f_s is 50kHz, i.e., the switching period T_s is 20μs; and (vi) the product name of the control IC is MC34060A. It is noted that the proposed converter operates in CCM above the minimum dc output current. In addition, Tables 1 and 2 show the voltage and current stresses of the switch and diodes, and the specifications for the components used in the main power stage of the proposed converter.

Table 1. Voltage and current stresses of the switch and diodes

	S_1	D_1	D_2	D_3	D_4
Voltage stress (V)	400	68.1	234	400	342
Current stress (A)	15.5	8.91	4.87	1.68	11.3

Table 2. Components used in the main power stage of the proposed converter

Components	Specifications
S_1	STP30NM50, V_{DS}=500V, I_D=27A, R_{on}=115mΩ at 14A
D_1	V40100C, V_R=100V, V_F=0.38V at I_F=5A
D_2, D_4	ETH3006, V_R=600V, V_F=2V at I_F=30A
D_3	STPSC806D, V_F=1.4V at I_F=8A
L_1	CC4220/JPP44A, 38 turns, 1.622mm air-gap
L_m	CC4220/JPP44A, N_1=N_2=48 turns, 0.628mm air-gap
C_1	RUBYCON, 2200μF
C_2	NICHICON, 220μF
C_o	RUBYCON, 150μF*2 paralleled

Sequentially, the energy-storing components, such as L_1, L_m, C_1, C_2 and C_o, are taken into account, under the condition that the converter operates in CCM and the turns ratio of the coupling inductor, n, is set to one.

4.1 Design of L_1

Fig. 5(a) shows the waveforms related to L_1. In addition, (8) can be rewritten to be

$$V_o D^2 + (V_i - 2V_o)D + V_o - (2+n)V_i = 0 \tag{24}$$

From (24), the duty cycle D can be obtained as

$$D = \frac{2V_o - V_i - \sqrt{V_i^2 + 4\times(1+n)V_i V_o}}{2V_o} \tag{25}$$

Therefore, according to (25), the minimum duty cycle D_{min} occurs at the maximum dc input voltage $V_{i,max}$, and the maximum duty cycle D_{max} occurs at the minimum dc input voltage $V_{i,min}$.

Sequentially, based on Fig. 5(a), Δi_{L1} can be expressed to be

$$\Delta i_{L1} = \frac{v_{L1}\Delta t}{L_1} = \frac{V_i D T_s}{L_1} \tag{26}$$

Therefore, the maximum value of Δi_{L1}, signified by $\Delta i_{L1,max}$, can be expressed to be

$$\Delta i_{L1,max} = \frac{V_{i,max} D_{min} T_s}{L_1} \tag{27}$$

In order to make sure that L_1 operates in CCM, the following inequality must be obeyed:

$$I_{L1,min} \geq \frac{\Delta i_{L1,max}}{2} \tag{28}$$

where $I_{L1,min}$ is the minimum dc current in L_1.

Also, if the efficiency of the overall system is assumed to be equal to 100%, then the following equation can be obtained to be

$$I_{L1,min} = I_{i,min} = \frac{P_{o,min}}{V_{i,max}} \tag{29}$$

Based on (27) to (29), the inequality for L_1 can be obtained to be

$$L_1 \geq \frac{V_{i,max}^2 D_{min} T_s}{2P_{o,min}} = \frac{28^2 \times 0.589 \times 20\mu}{2\times 40} \cong 115.4\mu\text{H} \tag{30}$$

Therefore, the value of L_1 is larger than 115.4μH so as to make sure that L_1 operates in CCM. Furthermore, considering the efficiency performance, the higher the value of L_1 is, the smaller the peak current in L_1 and hence the lower the conduction loss and core loss. Eventually, the value of L_1 is chosen to be 225μH, which is about double the calculated value. Also, the core, named CC4220/JPP44A, is selected to construct L_1 along with the corresponding turns of 38 and the required air-gap of 1.622mm.

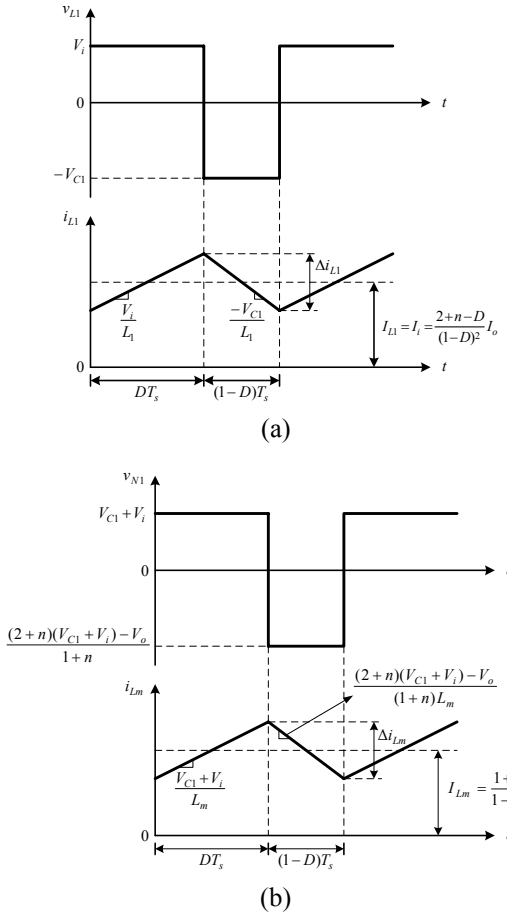


Fig. 5. Waveforms related to: (a) L_1; (b) L_m.

4.2 Design of L_m

Fig. 5(b) shows the waveforms related to L_m. In addition, Δi_{Lm} can be expressed as

$$\Delta i_{Lm} = \frac{v_{N1}\Delta t}{L_m} = \frac{(V_{C1} + V_i)DT_s}{L_m} \tag{31}$$

According to (5) and (31) can be rewritten as

$$\Delta i_{Lm} = \frac{DV_iT_s}{(1-D)L_m} \tag{32}$$

Therefore, it can be seen that the maximum value of Δi_{Lm}, signified by $\Delta i_{Lm,max}$, can be expressed to be

$$\Delta i_{Lm,max} = \frac{D_{min}V_{i,max}T_s}{(1-D_{min})L_m} \tag{33}$$

In order to make sure that L_m operates in CCM, the following equation must be obeyed:

$$I_{Lm,min} \geq \frac{\Delta i_{Lm,max}}{2} \tag{34}$$

where $I_{Lm,min}$ is the minimum dc current in L_m and can be expressed to be

$$I_{Lm,min} = \frac{(1+n)P_{o,min}}{(1-D_{min})V_o} \tag{35}$$

Based on (33) to (35), the inequality for L_m can be obtained as

$$\begin{aligned} L_m &\geq \frac{D_{min}V_{i,max}V_oT_s}{2\times(1+n)P_{o,min}} \\ &= \frac{0.589\times 28\times 400\times 20\mu}{2\times(1+1)\times 40} \\ &\cong 824.6\mu\text{H} \end{aligned} \tag{36}$$

Hence, the value of L_m is larger than 824.6μH, so as to make sure that L_m operates in CCM. Furthermore, considering the limitation of winding area, the value of L_m is chosen to be 900μH, which is about 1.1 times of the calculated value. Also, the core, named CC4220/JPP44A, is selected to construct L_m along with the corresponding N_1 turns of 48 and the required air-gap of 0.628mm. In addition, since n is set at one, the corresponding N_2 turns are also 48.

4.3 Design of C_1

From Fig. 6(a), the voltage ripple on C_1, called Δv_{C1}, is composed of the voltage ripple Δv_{C1_ESR} created from the current flowing through the equivalent series resistor ESR_{C1}, and the voltage ripple Δv_{C1_cap} created from the charging and discharging of C_1. Therefore, Δv_{C1} can be expressed to be

$$\Delta v_{C1} = \Delta v_{C1\_ESR} + \Delta v_{C1\_cap} \tag{37}$$

Also, Δv_{C1_ESR} can be represented by

$$\Delta v_{C1\_ESR} = \Delta i_{C1}ESR_{C1} \cong \frac{(1+n)ESR_{C1}I_o}{D(1-D)^2} \tag{38}$$

where

$$ESR_{C1} = \frac{\tan\delta_{C1}}{2\pi f_sC_1} \tag{39}$$

where $\tan\delta_{C1}$ is the dissipation factor of C_1.

In addition, Δv_{C1_cap} can be signified by

$$\Delta v_{C1\_cap} = \frac{i_{C1\_(1-D)}\Delta t}{C_1} \approx \frac{(I_{L1} - \frac{I_{Lm}}{1+n})(1-D)T_s}{C_1} = \frac{(1+n)I_oT_s}{(1-D)C_1} \tag{40}$$

where $i_{C1\_(1-D)}$ is the current flowing through C_1 during the turn-off period.

By assuming the value of Δv_{C1} is set at 1% of the rated dc output voltage V_o, substituting (8), (38), (39) and (40) into (37) yields the following rearranged equation:

$$C_1 = \frac{[2\pi D(1-D) + \tan\delta_{C1}](1+n)I_oT_s}{0.02\times\pi D^2(1-D)V_i} \tag{41}$$

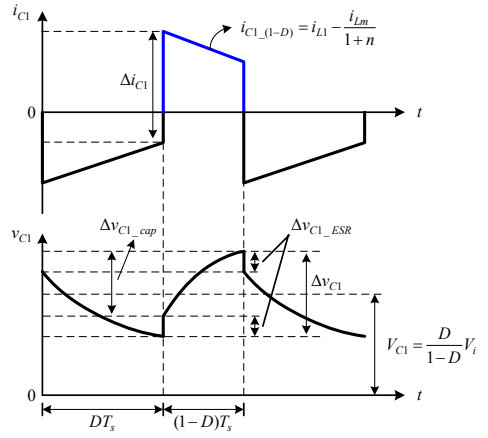
Based on (25) and (41), the minimum value of C_1 occurs under the conditions of the rated dc output power and the minimum dc input voltage. In addition, under the given switching period T_s, the value of $\tan\delta_{C1}$ is about 13.13 based on the datasheet of Rubycon ZLH series capacitors. Hence, the minimum value of C_1 can be calculated to be 1563μF as follows:

$$\begin{aligned} C_1 &\geq \frac{[2\pi D_{max}(1-D_{max}) + \tan\delta](1+n)I_{o,rated}T_s}{0.02\times\pi D_{max}^2(1-D_{max})V_{i,min}} \\ &= \frac{[2\times 3.1415\times 0.658\times(1-0.658)+13.13]\times(1+1)\times 0.5\times 20\mu}{0.02\times 3.1415\times 0.658^2\times(1-0.658)\times 20} \\ &\cong 1563\mu\text{F} \end{aligned} \tag{42}$$

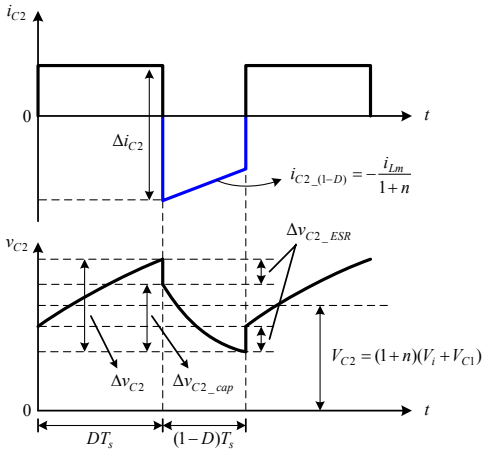
Finally, one 2200μF Rubycon capacitor is chosen for C_1.

4.4 Design of C_2

From Fig. 6(b), the voltage ripple on C_2, called Δv_{C2}, is composed of the voltage ripple Δv_{C2_ESR} created from the current flowing through the equivalent series resistor



(a)



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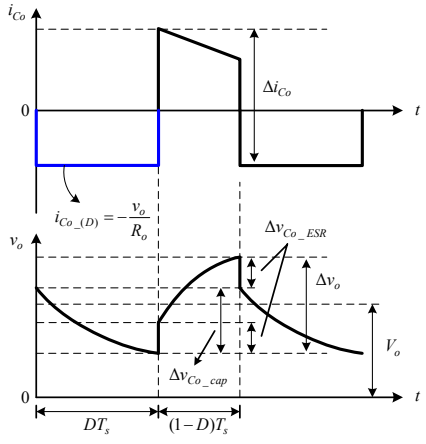

(c)

Fig. 6. Waveforms pertaining to: (a) C_1; (b) C_2; (c) C_o.

ESR_{C2}, and the voltage ripple Δv_{C2_cap} created from the charging and discharging of C_2. Therefore, Δv_{C2} can be expressed to be

$$\Delta v_{C2} = \Delta v_{C2\_ESR} + \Delta v_{C2\_cap} \tag{43}$$

Also, Δv_{C2_ESR} can be represented by

$$\Delta v_{C2\_ESR} = \Delta i_{C2} ESR_{C2} \cong \frac{ESR_{C2} I_o}{D(1-D)} \tag{44}$$

where

$$ESR_{C2} = \frac{\tan\delta_{C2}}{2\pi f_s C_2} \tag{45}$$

where $\tan\delta_{C2}$ is the dissipation factor of C_2.

Moreover, Δv_{C2_cap} can be signified by

$$\Delta v_{C2\_cap} = \frac{i_{C2\_(1-D)} \Delta t}{C_2} \approx \frac{V_o T_s}{R_o C_2} = \frac{I_o T_s}{C_2} \tag{46}$$

where $i_{C2\_(1-D)}$ is the current flowing through C_2 during the turn-off period.

By assuming that the value of Δv_{C2} is set at 0.5% of the rated dc output voltage V_o, substituting (8), (44), (45) and (46) into (43) yields the following rearranged equation:

$$C_2 = \frac{[2\pi D(1-D) + \tan\delta_{C2}] I_o T_s}{0.01 \times \pi D(1+n) V_i} \tag{47}$$

Based on (25) and (47), the minimum value of C_2 occurs under the conditions of the rated dc output power and the minimum dc input voltage. In addition, under the given switching period T_s, the value of $\tan\delta_{C2}$ is about 6.22 based on the datasheet of Nichicon CS series capacitors. Hence, the minimum value of C_2 can be worked out to be 92.3μF as follows:

$$\begin{aligned} C_2 &\geq \frac{[2\pi D_{max}(1-D_{max}) + \tan\delta_{C2}] I_{o,rated} T_s}{0.01 \times \pi D_{max}(1+n) V_{i,min}} \\ &= \frac{[2 \times 3.1415 \times 0.658 \times (1-0.658) + 6.22] \times 0.5 \times 20\mu}{0.01 \times 3.1415 \times 0.658 \times (1+1) \times 20} \\ &\cong 92.3\mu\text{F} \end{aligned} \tag{48}$$

Eventually, one 220μF Nichicon capacitor is selected for C_2.

4.5 Design of C_o

From Fig. 6(c), the voltage ripple on C_o, called Δv_o, is composed of the voltage ripple Δv_{Co_ESR} created from the current flowing through the equivalent series resistor ESR_{Co}, and the voltage ripple Δv_{Co_cap} created from the charging and discharging of C_o. Therefore, Δv_o can be expressed to be

$$\Delta v_o = \Delta v_{Co\_ESR} + \Delta v_{Co\_cap} \tag{49}$$

Also, Δv_{C2_ESR} can be represented by

$$\Delta v_{Co\_ESR} = \Delta i_{Co} ESR_{Co} \cong \frac{ESR_{Co} I_o}{1-D} \tag{50}$$

where

$$ESR_{Co} = \frac{\tan\delta_{Co}}{2\pi f_s C_o} \tag{51}$$

where $\tan\delta_{Co}$ is the dissipation factor of C_o.

Besides, Δv_{Co_cap} can be signified by

$$\Delta v_{Co\_cap} = \frac{i_{Co\_(D)}\Delta t}{C_o} \approx \frac{V_o D T_s}{R_o C_o} = \frac{I_o D T_s}{C_o} \tag{52}$$

where $i_{Co\_(D)}$ is the current flowing through C_o during the turn-on period.

By assuming that the value of Δv_o is set at 0.1% of the rated output voltage V_o, substituting (8), (50), (51) and (52) into (49) yields the following rearranged equation:

$$C_o = \frac{[2\pi D(1-D) + \tan\delta_{Co}]I_o T_s}{0.002\times\pi(1-D)V_o} \tag{53}$$

Based on (25) and (53), the minimum value of C_o occurs under the conditions of the rated dc power and the minimum dc input voltage. In addition, under the given switching period T_s, the value of $\tan\delta_{Co}$ is about 14.14 based on the datasheet of Rubycon CXW series capacitors. Hence, the minimum value of C_o can be figured out to be 180.9μF as follows:

$$\begin{aligned} C_o &\geq \frac{[2\pi D_{max}(1-D_{max}) + \tan\delta_{Co}]I_{o,rated}T_s}{0.002\times\pi(1-D_{max})V_o} \\ &= \frac{[2\times 3.1415\times 0.658\times(1-0.658)+14.137]\times 0.5\times 20\mu}{0.002\times 3.1415\times(1-0.658)\times 400} \\ &\cong 180.9\mu\text{F} \end{aligned} \tag{54}$$

At last, two 150μF Rubycon capacitors, one 0.33μF plastic capacitor and one 22nF plastic capacitor are chosen for C_o and paralleled together.

4.6 Switch utilization

Like the traditional boost converter, the higher the voltage conversion ratio is, the lower the switch utilization *SU* [2], which is defined to be

$$SU = \frac{P_o}{V_{ds,max}\cdot I_{ds,max}} \tag{55}$$

where

$$P_o = 200\text{W} \tag{56}$$

$$V_{DS1,peak} = V_o = 400\text{V} \tag{57}$$

$$\begin{aligned} I_{DS1,peak} &= \frac{1+n}{D_{max}(1-D_{max})}I_o + \frac{V_{i,min}D_{max}T_s}{2\times(1-D_{max})L_m} \\ &\quad + \frac{P_o}{V_{i,min}} + \frac{V_{i,min}D_{max}T_s}{2L_1} \\ &= \frac{1+1}{0.658\times(1-0.658)}\times 0.5 + \frac{20\times 0.658\times 20\mu}{2\times(1-0.658)\times 900\mu} \\ &\quad + \frac{200}{20} + \frac{20\times 0.658\times 20\mu}{2\times 225\mu} \\ &\cong 15.5\text{A} \end{aligned} \tag{58}$$

Therefore, based on (55), the switch utilization of the proposed converter is about 0.032. This value is quite low due to the corresponding voltage conversion ratio is ultra high, about 20.

5. Experimental Results

On the one hand, Fig. 7 shows the waveforms relevant to the input voltage of 24V at rated load. Fig. 7 depicts the gate driving signal for S_1, v_{gs1}, and the current in L_1, i_{L1}; Fig. 8 shows the gate driving signal for S_1, v_{gs1}, the current i_3 with the sum of the current in N_1, i_1, and the current in L_m, i_{Lm}, and the current in N_2, i_2; Fig. 9 depicts the gate driving signal for S_1, v_{gs1}, the current in D_4, i_{D4}, and the current in S_1, i_{DS1}; Fig. 10 shows the gate driving signal for S_1, v_{gs1}, and the voltages on C_1 and C_2, v_{C1} and v_{C2}; Fig. 11 depicts the gate driving signal for S_1, v_{gs1}, and the output voltage ripple Δv_o; Fig. 12 shows the gate driving signal for S_1, v_{gs1}, and the voltage on S_1, v_{DS1}. From these figures, it can be seen that the proposed converter can operate well to some extent and the output voltage ripple is about 360mV, i.e., 0.09% of V_o, smaller than 0.1% of V_o. Furthermore, it can be seen that from Fig. 12, the voltage across S_1 has no voltage spike.

The following is used to further explain the current

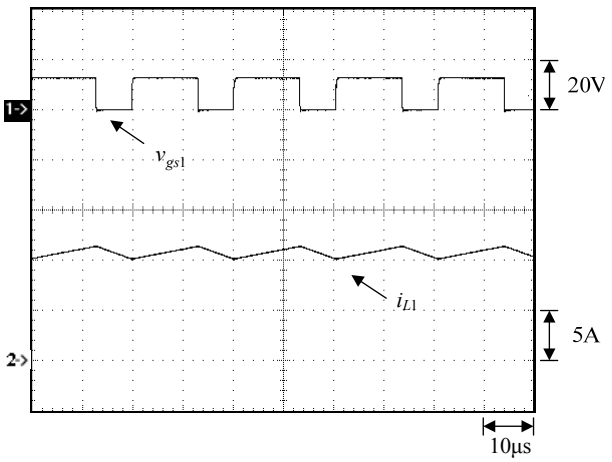

Fig. 7. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) i_{L1}.

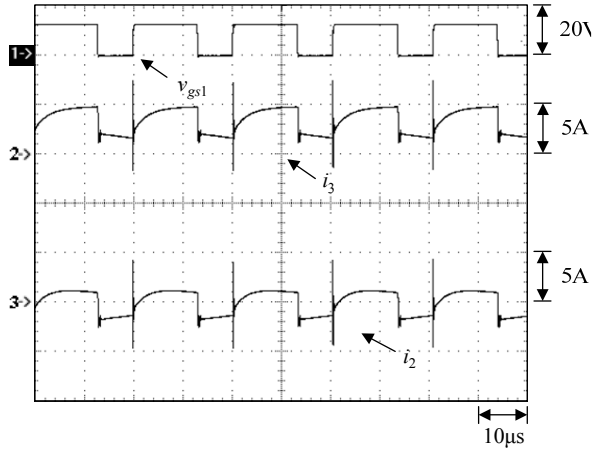

Fig. 8. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) i_3; (3) i_2.

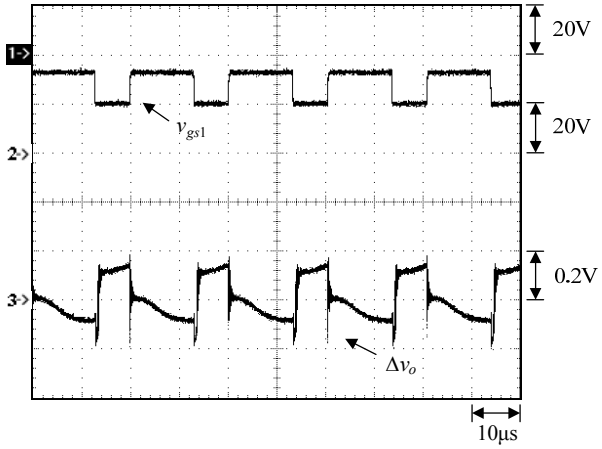

Fig. 11. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) Δv_o.

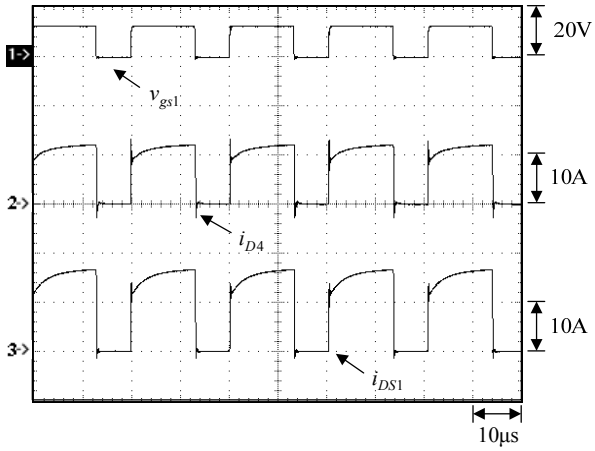

Fig. 9. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) i_{D4}; (3) i_{DS1}.

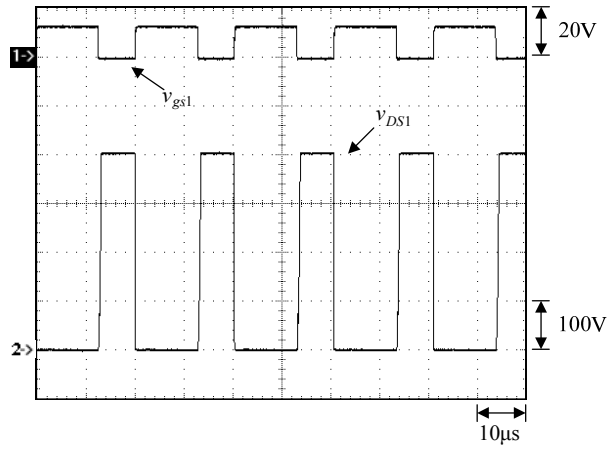

Fig. 12. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) v_{DS1}.

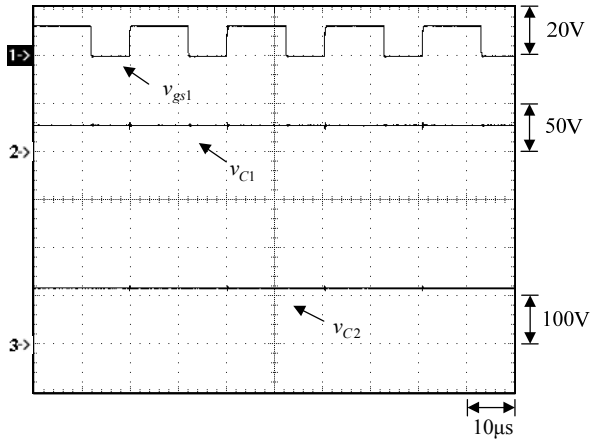

Fig. 10. Measured waveforms under the input voltage of 24V at rated load: (1) v_{gs1}; (2) v_{C1}; (3) v_{C2}.

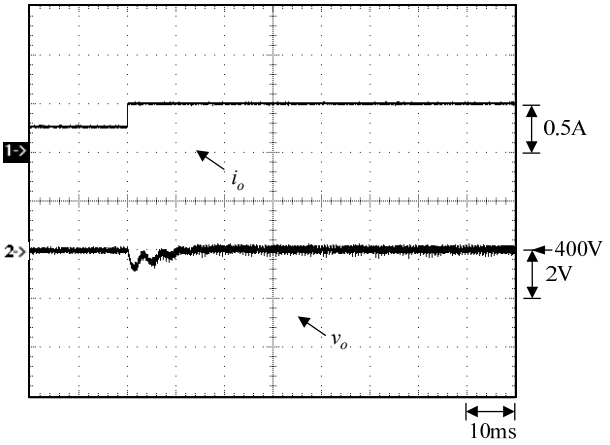

Fig. 13. Load transient response due to step load change from 50% to 100% load under the rated input voltage.

spikes on i_2 and i_3 shown in Fig. 8. Since the proposed converter operates in CCM, the reverse recovery currents created from the diodes are indispensible. Aside from this, in order to reduce the primary and secondary leakage inductances, the bifilar winding technique is adopted, thereby causing the equivalent parasitic capacitance in the transformer to be increased. Furthermore, since the

proposed converter is an ultra high step-up converter, the voltage across the transformer is relatively large during the turn-off period, implying that the energy stored in the equivalent parasitic capacitance in the transformer is relatively large. Therefore, based on the mentioned above, high current spikes occur as soon as the switch is turned on. This phenomenon can be seen in the traditional boost converter operating in CCM with a high output voltage. As generally acknowledged, these current spikes will create EMI noises. However, the EMI problem should be taken into account from many aspects, such as EMI choke design, shielding design, layout, etc. Consequently, in this paper, it is very hard to discuss the effects of these current spikes on the EMI problem.

Besides, Figs. 13 and 14 are used to show load transient responses due to step load change from 50% to 100% load and 100% and 50%, respectively. From these figures, it can be seen that the values of two recovery times are both about 1.2V, and the values of the undershoot and overshoot are both within 16ms. And, Fig. 15 shows a photo of the experimental setup.

Finally, Table 3 makes a comparison between the proposed converter and the converters shown in the References, in terms of voltage conversion ratio, com-

Table 3. Comparison between the proposed converter and the converters shown in the References, in terms of voltage conversion ratio, component number, switch voltage stress, output inductor and floating output

Ref.	Voltage conversion ratio	Component number	Switch voltage stress	Output inductor	Floating output
[3]	$\frac{1}{(1-D)^2}$	8	$V_{ds1}=\frac{V_i}{1-D}$, $V_{ds2}=V_{ds3}=\frac{V_i}{(1-D)^2}$	No	No
[4]	$\frac{1+n}{1-D}$	10	$V_{ds1}=nV_i$, $V_{ds2}=\frac{nD}{1-D}V_i$	No	No
[5]	$\frac{2+n}{1-D}$	10	$V_{ds1}=\frac{V_i}{1-D}$	No	No
[6]	$\frac{1+n}{1-D}$	15	$V_{ds1}=\frac{V_i}{1-D}$	No	No
[7]	$\frac{2}{1-D}+nD$	13	$V_{s1}=V_{s2}=\frac{V_o}{2}-\frac{nDV_i}{2}$	No	No
[8]	$\frac{1+D+nD}{1-D}$	9	$V_{ds1}=\frac{V_i}{1-D}$	No	Yes
[9]	$\frac{2(1+nD)}{1-D}$	10	$V_{ds1}=\frac{1+nD}{1-D}V_i$	No	Yes
[10]	$\frac{2+nD}{1-D}$	14	$V_{ds1}=\frac{V_i}{1-D}$	No	No
[11]	$1+D$	6	$V_{ds1}=2V_i$, $V_{ds2}=V_i$	Yes	No
[12]	$\frac{2-D}{1-D}$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	Yes	No
[13]	$\frac{2-D}{1-D}$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	Yes	No
[14]	$\frac{2}{1-D}+n$	8	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	No	No
[15]	Type 1: $\frac{3-D}{1-D}$ Type 2: $\frac{2}{1-D}$ Type 3: $\frac{3-2D}{1-D}$	10	Type 1: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{1+D}{1-D}V_i$ Type 2: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{1+D}{1-D}V_i$ Type 3: $V_{ds1}=V_{ds2}=V_i$, $V_{ds3}=\frac{2-D}{1-D}V_i$	No	No
[16]	$\frac{2nD}{1-D}+1$	11	$V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=(\frac{3D-1}{1-D})V_i$	No	No
[17]	Type 1: 2D Type 2: 2D	8	Type 1: $V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=V_i$, $V_{ds4}=V_i$ Type 2: $V_{ds1}=V_i$, $V_{ds2}=V_i$, $V_{ds3}=V_i$, $V_{ds4}=V_i$	Yes	No
[18]	$\frac{n+1}{1-D}$	10	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	No	No
[19]	$\frac{2n+1}{1-D}$	11	$V_{ds1}=V_{ds2}=\frac{V_i}{1-D}$	No	No
Proposed	$\frac{2+n-D}{(1-D)^2}$	10	$V_{ds1}=[\frac{2+n-D}{(1-D)^2}]V_i$	No	No

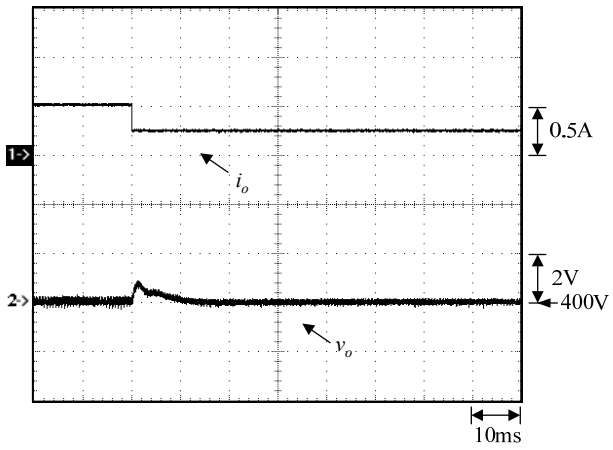

Fig. 14. Load transient response due to step load change from 100% to 50% load under the rated input voltage.

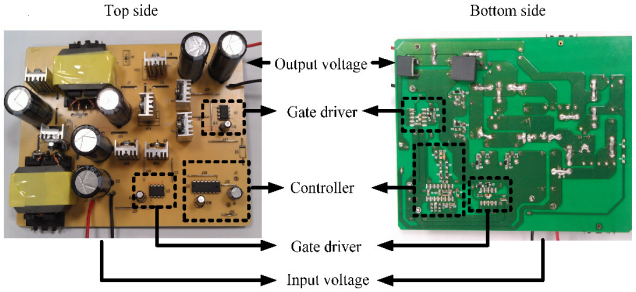

Fig. 15. Photo of the experimental setup.

ponent number, switch voltage stress, output inductor and floating output. From Table 3, it can be seen that the denominator of the voltage conversion ratio of the proposed converter is the square of one minus duty cycle, and hence, under a given duty cycle and turns ratio, the proposed converter has a higher voltage conversion ratio than all the other references do, but the corresponding voltage stress is higher than all the other voltage stresses. Also, the number of the components is 10, which is acceptable as compared to those used in the References.

6. Conclusion

A high step-up converter is presented herein, which combines the traditional buck-boost converter, the charge pump capacitor and the coupling inductor, so as to make the circuit design relatively elastic. Above all, the leakage inductance energy can be recycled to the output, and hence no voltage spike on the switch occurs. In addition, the used power switch is not floating, so as to make the gate driving circuit quite simple. Based on the mentioned above, this converter is very suitable for the green energy applications.

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