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Optimal Shunt Compensation for Improving Voltage Stability and Transfer Capability in Metropolitan Area of the Korean Power System

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Abstract – This paper deals with shunt compensation to eliminate voltage violation and enhance transfer capability, which is motivated towards implementation in the Korean power system. The optimal shunt compensation algorithm has demonstrated its effectiveness in terms of voltage accuracy and reducing the number of actions of reactive power compensating devices. The main shunt compensation devices are capacitor and reactor. Effects of control devices are evaluated by cost computations. The control objective at present is to keep the voltage profile of a key bus within constraints with minimum switching cost. A robust control strategy is proposed to make the control feasible and optimal for a set of power-flow cases that may occurs important event from system. Case studies with metropolitan area of the Korean power system are presented to illustrate the method.

Keywords: Shunt compensation, Voltage stability, Transfer capability, Optimization, Key bus

1. Introduction

Shunt compensation system is used to improve frequency and voltage quality, reduce transmission line loss, and realize the efficiency of generating equipment. Electrical loads both generate and absorb reactive power. Since the transmitted load varies considerably from one hour to another, the reactive power balance in a grid varies as well. The result can be unacceptable voltage amplitude variations, a voltage depression, or even a voltage collapse.

A slowly operating capacitor can discretely provide the reactive power required to control static voltage swings under various system conditions and thereby improve the power system transmission and distribution performance.

Installing a capacitor at one or more suitable points in the network will increase transfer capability through enhanced voltage stability, while maintaining a smooth voltage profile under different network conditions. In addition, capacitor can mitigate active power oscillations through voltage amplitude modulation.

In order to maintain power quality and to minimize transmission losses, grid operator controls voltage and reactive power. Although this voltage and reactive power control problem has been important in power system operation, it has become difficult to handle voltage and reactive power because system more and more complex. From this reason, the consequence is that efficient operate system is needed [1-3].

The purpose of voltage control in distribution network is to compensate for load variations and events in the transmission system, such that all customer supply voltages are kept within certain bounds. Many countries have implemented the automatic voltage regulation based on the hierarchical control system in order to appropriate voltage profile control. The hierarchical control system is organized in a three levels structure, which are primary voltage regulation, secondary voltage regulation, and tertiary voltage regulation. This system controls the terminal voltage of the generator by Automatic Voltage Regulator (AVR) in the generation level, whereas controls the key bus voltage by control generators in a control regional level. The concept of the key bus and the control area are based on interrelation between a load bus and another load buses by electrical distance [4-9].

The on-line voltage control using full SCADA information is implemented in the bulk power system. It can only deal with a steady state power system because the SCADA is being updated in every few minutes. If a system condition is going to emergency, it cannot control the system. For preventing this situation, a control scheme of discrete type devices such as capacitor and reactor is proposed [10-12]. It is based on the SCADA measurement and selects device having the lowest cost to maintain the voltage profile. This scheme has been implemented in Korean power system since September 2010 [12].

The main goal of this paper is the control strategies adopted at the bulk power system for shunt compensation. It optimizes bus voltages, which is the control target, capacitor and reactor switching under constraint of voltage limit and reactive power balance for local system voltage stability. The method uses the optimization of various cost penalties to control the key bus. The paper describes the main characteristics and performances of the mention control apparatuses, the progress of their application in

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metropolitan area of the Korean power system, and significant analysis results are also shown.

2. Calculation of the Interface Flow Margin

Shunt compensation using capacitor banks can increase the maximum transfer limit of real power [1]. The power system becomes more unstable when it is close to the collapse point. More shunt compensation has to be added to keep the voltage within stable limits as the load power increases [2]. The power system can collapse even at normal operating voltage levels due to over-compensation. It is therefore necessary to consider generators as major voltage control devices for more secure operation.

Eq. (1) shows the compensation amount of the reactive power according to shunt compensation. V_{LV} is the low-side voltage and B is the shunt capacitor capability.

$$Q = BV_{LV}^2 \tag{1}$$

In order to consider the effect of a transfer capability increase in a metropolitan area according to the insertion of shunt capacitors, it is calculated by taking into account an interface flow margin using F-V curve analysis [13].

F-V analysis is used to judge the system stability by calculating the active power margin from area 1 to area 2 such as Fig. 1. P-V analysis utilizes the method of continuously active power load increase for finding the limit of the system operation, whereas F-V analysis is used to define the limit of the system operation point by using the generation shift method. In other words, area 2 can receive active power generation from area 1 by using a method that results in a generation decrease in area 2 and a generation increase in area 1. This is illustrated as the concept of the interface flow margin in Fig. 2.

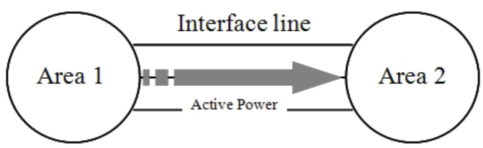

Fig. 1. Areas interconnected through an interface line

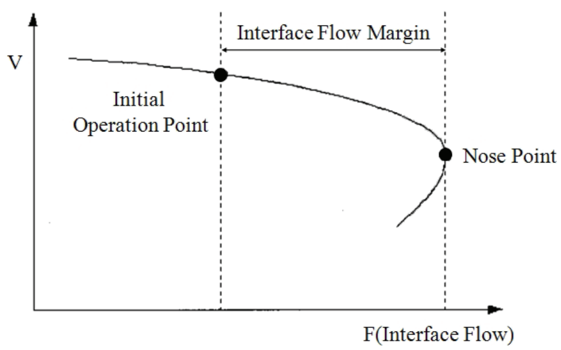

Fig. 2. Concept of the interface flow margin

The interface flow margin is the difference between the limit of the system operation point and the initial operation point, as indicated in Eq. (2).

$$F_{margin} = B_{operation\_limit} - V_{current} \tag{2}$$

3. Determination of the Key Bus

Given a Jacobian matrix of power flow equation:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = J \begin{bmatrix} \Delta \delta \\ \Delta V \end{bmatrix} \tag{3}$$

with,

$$J = \begin{bmatrix} J_{11} & J_{12} \\ J_{21} & J_{22} \end{bmatrix} = \begin{bmatrix} \frac{\partial P}{\partial \delta} & \frac{\partial P}{\partial V} \\ \frac{\partial Q}{\partial \delta} & \frac{\partial Q}{\partial V} \end{bmatrix} \tag{4}$$

To consider the system configuration, the sensitivity between the variation of the reactive load and the generation at each machine from the equation is computed.

$$[\Delta Q] = \left[\frac{\partial Q}{\partial V}\right][\Delta V] \tag{5}$$

According to the generally accepted formula from Stott's simplifications [14], the linear system equations can be represented in the form.

$$[\Delta Q] = [B][\Delta V] \tag{6}$$

where, B is the symmetric matrix of the susceptance of the transmission grid in p.u.

$$\begin{aligned} [\Delta Q_G] &= -[B_{GG}][\Delta V_G] - [B_{GL}][\Delta V_L] \\ [\Delta Q_L] &= -[B_{LG}][\Delta V_G] - [B_{LL}][\Delta V_L] \end{aligned} \tag{7}$$

The voltage variation via the reactive power variation of load buses from (7) which is described as equation that is as follows:

$$\Delta V_L = -B_{LL}^{-1} B_{LG} \cdot \Delta V_G - B_{LL}^{-1} \cdot \Delta Q_L \tag{8}$$

If the system is steady state $(\Delta V_G = 0)$, define the identical equation from (8).

$$S_L = -B_{LL}^{-1} = \frac{\Delta V_L}{\Delta Q_L} \tag{9}$$

According to this equation, the voltage variation via the reactive power variation of load buses is the sensitivity matrix of S_L. The diagonal terms of the sensitivity matrix indicate what the robust is. The bus having the smallest value in the diagonal terms is the most robust because that the bus is insensitive to a change in the injected reactive power.

The key bus should be selected in order that the effect owing to the voltage deviations for whole of load buses. For example, the key bus must reflect the voltage level in the entire system and should not be changed due to any disturbances. In this reason, we can select the ascending order of the coefficient SL as the key bus. The bus which has the minimum value of S_L is affected by the reactive power change of another load buses and therefore coincides with the former conditions.

4. Optimization Algorithm

The objective of the proposed method is to regulate the key bus voltage. The key bus should be maintained with the voltage in the voltage stability point of view. The algorithm selects the discrete control devices by a cost function. The cost function consists of a voltage penalty, a switching value, an active power loss, and an interface flow. The formulation of the cost function is written as follows:

$$Minimize\begin{bmatrix} w_n\sum_{i=1}^{n}\left[|x_i|S_i\right]+ \\ \sum_{m=1}^{M}\left[f_m(x_i)+w_{m1}P_{loss}(x_i)-w_{m2}F_{flow,m}(x_i)\right]\end{bmatrix} \tag{10}$$

$$s.t.\sum_{i=1}^{n}|x_i|\le 1,$$

$$x_i=\{x_i \| x_i|\le 1, i\in n\}$$

$$P_{loss}=\sum_{i=1}^{n}\sum_{j=1}^{n}\left[V_i^2G_{ij}+V_j^2G_{ij}-2V_iV_jG_{ij}\cos\left(\delta_i-\delta_j\right)\right] \tag{11}$$

In this place, n is the number of control device, m is the number of load bus, S_i is the switching value of i_{th} control device, f_m is the penalty function, x_i is the status of i_{th} control device, P_{loss} is the penalty of active power loss, F_{flow} is the gain of the interface flow margin, and w_n, w_{m1}, w_{m2} represents the weighting factor of the switching value, the active power loss, and the gain of the interface flow, respectively. The x_i has three values: '-1', '0', and '+1'. '-1' signifies that a bank of capacitors and reactors should be opened, '0' signifies that the device should not be switched on, and '+1' signifies that a bank of capacitors and reactors should be closed. The weighting factors of the switching value, the active power loss, and the gain of the interface flow are different from those of the system characteristics. They are as follows:

$$S_{penalty}=\frac{SC/SR_{capacity}}{BASE_{system}}$$

$$P_{loss\_penalty}=\frac{P_{loss\_current}}{BASE_{system}}$$

$$F_{flow\_gain}=\frac{\left(F_{margin\_base}-F_{margin\_current}\right)}{BASE_{system}} \tag{12}$$

The maximum bank of capacitors and reactors is required for effective system voltage control. If there is a low voltage bus, our proposed algorithm will consider not closing the bank of capacitors, but opening a bank of reactors instead. To include this control scheme in the formulation of the cost function, each device is considered to have a different S_i and the cost of switching on is considered to be greater than that of switching off. The control device is selected by using Eq. (10), which has minimum cost at this stage. This is an objective of the proposed algorithm.

Penalty factors represent scale values for getting out of the threshold. A demerit order is a disadvantage. Thus, a voltage penalty is the disadvantage of voltage violation that is reflected in the switching devices.

$$f(v)=\begin{cases} 0 & ,V_1<v<V_2 \\ f_m & ,v>\alpha V_2 \\ f_m & ,\beta V_1<v \\ \dfrac{f_m}{V_2(\alpha-1)}v-\dfrac{f_m}{(\alpha-1)} & ,V_2<v<\alpha V_2 \\ -\dfrac{f_m}{V_1(1-\beta)}v+\dfrac{f_m}{(1-\beta)} & ,\beta V_1<v<V_1 \end{cases} \tag{13}$$

where,

v represents the current voltage of the load bus,

V_1 and V_2 are the target voltages of the load buses, which are generally nominal voltages,

f_m is a constant value, and

α and β are the constant gains of the cost function, which is $0<\beta<1<\alpha<2$.

After switching, first check if any bus with voltage outside the preset limits exists. If so, penalty functions are calculated for all the voltage violating buses, and the maximum value is treated as the penalty cost. Each of the control devices has a switching cost. The capacitor switching cost is X_{cap}, while the switching cost of the reactor is X_{rea}. X_{cap} and X_{rea} are fixed heuristic methods. For deciding the value of a decision, it is necessary for the system operator to have experience. The control order of the control devices is listed in Table 1.

Table 1. Control order of control devices

order	Low voltage	High voltage
1	Switch off reactor 0	Switch off capacitor 0
2	Switch on capacitor X_{cap}	Switch on reactor X_{rea}

5. Overview of Control Schemes

The procedure for the proposed algorithm is shown as follows (also see Fig. 3). The central controller reads the SCADA/EMS power system data. It then runs the power flow calculation to check the key bus voltage. From this result, it calculates the cost function with respect to the discrete devices. Thereafter, it compares the voltage, which is to be regulated in the system, with the reference voltage. If there is voltage violation, it proceeds to the next step, while if there is no voltage violation, it terminates the algorithm. The controller then reads the information data of all discrete control devices. It then checks whether discrete devices are available or not. If discrete devices are available, the controller will move on to the next step. However, if there are none available devices, it will stop. Finally, the controllers will select the feasible devices by the cost function and then return to the step where the key bus voltage is compared to the reference voltage. Starting next steps are the same.

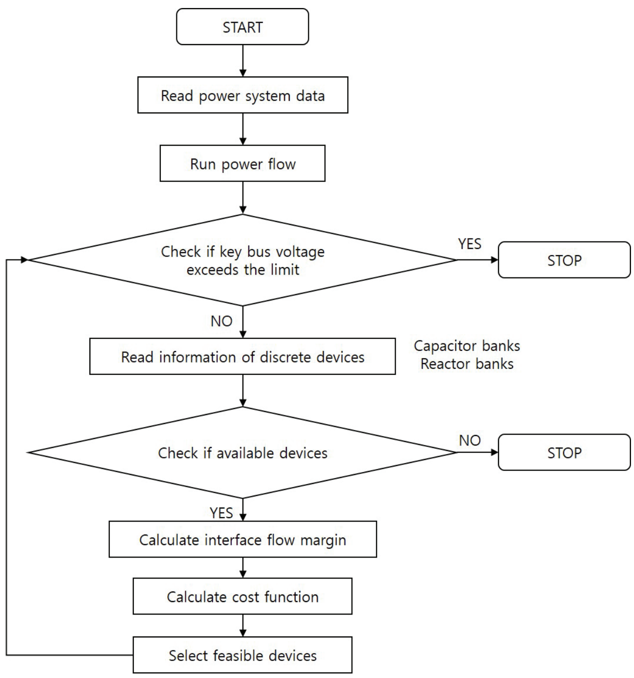

Fig. 3. Flow chart of the proposed algorithm

6. Case Study

The Korean power system has about 260 generators and 1400 load buses. Approximately 40% of the total load is concentrated in the metropolitan area, whereas most of the generators are located in the non-metropolitan areas. Furthermore, most power plants in the non-metropolitan areas have low generating cost. For this reason, a large amount of active power is transmitted from the non-metropolitan areas to the metropolitan area via interface lines in order to make the operations of the Korean power system more economical. This transfer of power is defined as an interface flow in the Korean power system. However, any increase in transfer power may lead to voltage instability due to the lack of reactive power support in the metropolitan areas [15]. Therefore, it is important that the reactive power reserves of power plants in the metropolitan area be accurately defined. The Korean power system is summarized in Table 2.

Table 2. Summary of the Korean power system

Area	Active Power [MW]		Reactive Power [MVAR]	
	Gen	Load	Gen	Load
Metropolitan	13,779	22,034	3,701	10,474
Non-Metropolitan	45,089	31,435	10,112	14,222

As shown in Table 2, the load level of the metropolitan area is similar to that of the non-metropolitan area, while the generation gap between the two areas corresponds to a factor of three. As a result, the metropolitan area could receive active power from the non-metropolitan area because there were very few installed high-capacity plants such as a nuclear power plant. Table 3 indicates the key buses of the Korean power system and the sensitivity values according to Eq. (9).

Table 3. Key buses in the Korean power system

Area	Key bus(345kV)	Sensitivity
Metropolitan	Sinsungnam	0.349
	Sinbupyong	0.220
Non-Metropolitan	Bukbusan	0.210
	Cheongyang	0.240
	Sinseosan	0.180
	Ulju	0.139
	Sinnamwon	0.260
	Sintaebaek	0.244
	Singwangju	0.115
	Sinyongju	0.108

Table 4 shows the shunt capacitors installed in the important 154 kV buses of the metropolitan area. In particular, these represent every available control capacitor.

Table 4. Control capacitor lists

Bus Name	Capacitor		Status
	Capacity	Bank	
Yangju	50	8	OFF
Migeum	50	7	OFF
Yeongseo	50	3	OFF
Dongseoul	50	2	OFF
Sinsiheung	50	2	OFF
Hwasung	50	2	OFF
Seoseoul	50	1	OFF
Sinyongin	50	4	OFF

Voltage violations in the metropolitan area according to contingencies are identified and control locations and amounts of shunt capacitors needed for interface flow maximization are determined. The key buses in the metropolitan area are Sinsungnam and Sinbupyung from Table 3. The contingency scenarios are as follows (can see in Table 5):

Table 5. Interface flow contingency lists

No	Contingency	
	Line	Circuit
1	Singapyeong-Sintaebaek	1
2	Sinansung-Sinseosan	1
3	Hwasung-Asan	1,2
4	Seoseoul-Sinonyang	1,2
5	Sinyongin-Sinjincheon	1,2
6	Konjiam-Sinjechon	1,2

Table 6 and Table 7 show the simulation test results for the Korean power system. The most severe contingency among the six line faults is Hwasung-Asan, in which the interface flow margin dramatically decreased from 2607.5 MW to 776.1 MW. As a result, we targeted the contingency as Hwasung-Asan. The capacitors installed in Dongseoul and Migeum were selected by the proposed algorithm, and the key bus voltage violation was removed after 5 banks capacitors are inserted step by step. The voltage criterion is from 0.95 to 1.05 in p.u.

Table 6. Interface flow margin of contingencies

Contingency	Interface Flow Margin [MW]
Base	2607.5
Singapyeong-Sintaebaek	1761.8
Sinansung-Sinseosan	1991.6
Hwasung-Asan	776.1
Seoseoul-Sinonyang	1492.6
Sinyongin-Sinjincheon	2444.6
Konjiam-Sinjechon	1406.8

Table 7. Result of the control algorithm

Key Bus		Order	Switch On Capacitor [MVAR]
Name	Voltage (p.u)		
Sinsungnam	0.9325	1	Dongseoul 50MVAR
Sinsungnam	0.9359	2	Dongseoul 50MVAR
Sinsungnam	0.9391	3	Migeum 50MVAR
Sinsungnam	0.9422	4	Migeum 50MVAR
Sinsungnam	0.9492	5	Migeum 50MVAR
Stable	-	-	-

From the results, the interface flow margin increased by approximately 244 MW after the Hwasung-Asan fault when the total 250 MVAR capacitors of the selected bus, Dongseoul, and Migeum, were inserted as follows:

If did not reflect F_{flow} gain at the formulation of the cost function, the total 250 MVAR capacitors at the Sinsiheung, Hawsung, and Seoseoul buses were selected as control devices. The results showed that F_{flow} gain could increase the active power margin by approximately 103 MW more than the results of the not reflecting it.

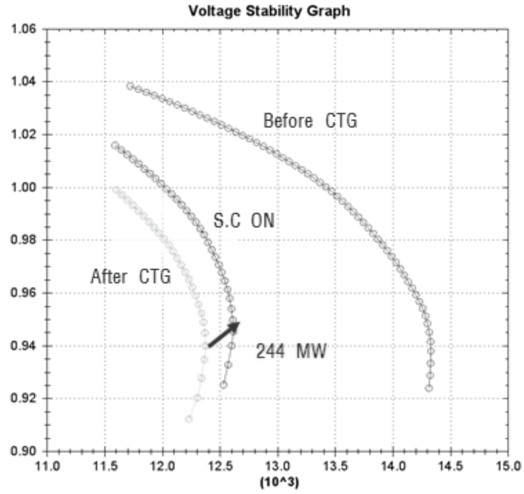

Fig. 4. Interface flow margin with F_{flow} gain

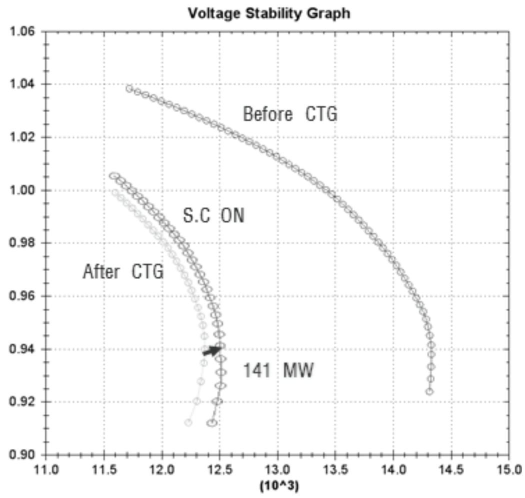

Fig. 5. Interface flow margin without F_{flow} gain

7. Conclusion

The optimal shunt compensation algorithm was found to be effective in terms of voltage accuracy and reducing the number of actions of reactive power compensating devices. When the algorithm was applied to the Korean power system, the test results showed that it eliminated voltage violations and enhanced transfer capability with interface flows. The simulation results reflected the gain of the interface margin and showed that active power margin increased more than it would have otherwise.

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