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The Influence of Silicon Doping on Electrical Characteristics of Solution Processed Silicon Zinc Tin Oxide Thin Film Transistor

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Effect of silicon doping into ZnSnO systems was investigated using solution process. Addition of silicon was used to suppress oxygen vacancy generation. The transfer characteristics of the device showed threshold voltage shift toward the positive direction with increasing Si content due to the high binding energy of silicon atoms with oxygen. As a result, the carrier concentration was decreased with increasing Si content.

Keywords: Oxide, Thin film transistor (TFT), Solution process

1. INTRODUCTION

Employment of amorphous oxide semiconductors (AOSs) provides the opportunity to develop superior electrical properties for display technology and other applications. These oxide semiconductors have transparency in the visible region and higher mobility compared with a-Si: H. Among the emerging semiconductor technologies, AOSs have attracted significant attention due to their high functional properties, including high mobility, high flexibility and low-temperature fabrication process. The promising functional materials for high performance thin film transistors (TFTs), such as indium-gallium-zinc oxide (IGZO) and zinc-tin-oxide (ZTO), exhibited high field effect mobility even in the amorphous phase because of the large edge-sharing structure of the s-orbitals [1-3]. Thus far, various materials, including Zn-Sn-O (ZTO), In-Zn-O (IZO), and In-Ga-Zn-O (IGZO), have been employed for the fabrication of oxide TFTs, and have been reported to show acceptable device performance for flat panel display (FPD) backplane applications. There are many vacuum synthesis technologies for TFTs, including physical vapor deposition (PVD), chemical vapor deposition (CVD), and pulsed laser deposition (PLD)[4-7]. However, these methods require expensive equipment due to inclusion of the vacuum process, thus resulting in high processing cost. Solution process has many advantages compared to the traditional deposition processes. First, it does not require vacuum processing and can be used for large area deposition. Furthermore, solution processes also allows much variation simply by controlling the compositions of the precursor ratio. Recently, the solution fabrication method was found to be suitable for flexible and large area flat panel displays, because such devices require room temperature processing and large size deposition. In the present study, we demonstrate variation of the threshold voltage of SZTO TFTs with incorporation of Si fabricated using solution process. Si has a lower standard electrode potential (SEP) than those of Sn and Zn, and thus can degenerate oxygen vacancy. [8-9] As a result, Si can act as a carrier suppressor in the SZTO system, and making it possible to control the threshold voltage through variation of the Si content.

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2. EXPERIMENTS

Heavily doped p-type silicon wafer was used as the substrate. Device fabrication started with a typical ultrasonic wafer cleaning process. A 0.5 M precursor solution of SZTO was prepared by the solution method, by dissolving a mixture of zinc acetate dehydrate [Zn $(CH_3COO)_2 \cdot 2H_2O$], tin chloride [$SnCl_2$] and silicon tetraacetate [Si $(OCOCH_3)_4$] in 2-methoxyethanol [$C_3H_8O_2$]. Monoethanolamine [C_2H_7NO] was then used as a solution stabilizer, and the mixture was stirred at 60℃. The mole ratio of Zn: Sn was fixed at 4:6, and silicon was added from 0.1 to 1. The solution was then stirred at room temperature for 12 h to form SZTO precursor. The precursor solution was filtered through a 0.2 μm syringe filter, and then spin-coated on silicon wafer at 3,000 rpm. The baking process was performed on a hot plate for 5 min under ambient air conditions, and annealing was carried out at 500℃ for 2 h under N_2. Channel and electrode patterning was formed by photolithography and the wet etching process. The bottom-gate and top-electrodes were fabricated on SiO_2 (200 nm)/heavily doped p-type Si wafer, where 70 nm electrodes of Ti/Au were deposited. The width and length of the active channel layer were 250 and 50 lm, respectively. The annealing process was performed at 500℃ for 2 h to improve the film quality.

Figure 1 shows a schematic of the SZTO TFT structure with the bottom gate and top contact electrode. Examination of the structural properties of SZTO thin films was carried out by X-ray diffraction (XRD). The electrical characteristics were measured with a semiconductor parameter analyzer.

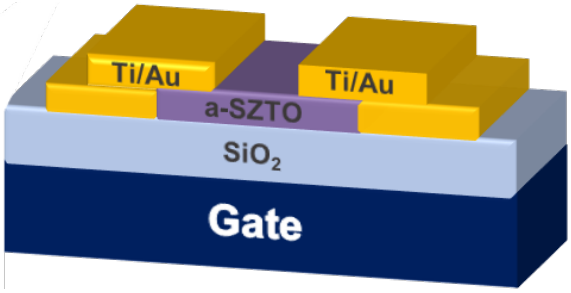

Fig. 1. Schematic representation of the TFT structure.

3. RESULTS AND DISCUSSION

Figure 2 shows the electrical properties of SZTO TFT with increase of the Si ratio. The threshold voltage was shifted toward the positive direction, and the on-current was decreased with increasing Si content. In order to explain the effect of Si doping of solution processed TFTs, we applied the creation mechanism for the formation of different vacancies in the SZTO and ZTO. The oxygen vacancies in such systems are produced via dihydroxylation of M-OH and the alloy mechanism. Si has high binding energy with oxygen due to its low SEP. As a result, a decrease in the number of free electrons associated with decreased oxygen vacancy can be observed. In addition, the field effect mobility is decreased with increasing Si ratio from 0.1 to 1. The μFE was calculated using the following equation:

$$I_{DS} = \left(\frac{\mu_{FE} C_I W}{2L}\right)(V_{GS} - V_{th})^2$$

where C_i is the capacitance per unit area of the gate insulator, W and L are the channel width and length, and V_{GS} and V_{th} are the gate bias and the threshold voltage, respectively. A summary of the

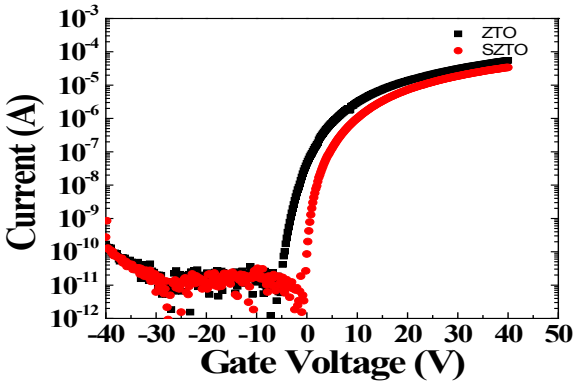

Fig. 2. Transfer characteristics of ZTO and SZTO TFTs.

Table 1. Electrical characteristics of the ZTO and SZTO TFTs, including threshold voltage, on-to-off ratio, and μ_{FE}.

Si : Zn : Sn	V_{th} (V)	$I_{on/off}$ current ratio	μ_{FE} ($cm^2 V^1 S^{-1}$)	Subthreshold swing (V/decade)
0 : 1 : 1	-1.2	6.51×10^6	1.76	0.56
0.1 : 1 : 1	0.8	1.66×10^7	0.70	0.28

TFT performance parameters according to the Si ratio is provided in Table 1, which includes the field effect mobility (μ_{FE}), threshold voltage (V_{th}), on-current (I_{on}), carrier concentration, and on-to-off current ratio ($I_{on/off}$). The ZTO TFT annealed at 500℃ displayed high performance, with the field effect mobility of 1.76 cm^2/ V s and threshold voltage of -1.2 V, while the SZTO TFT annealed at 500℃ exhibited the field mobility of 0.7 cm^2/ V s and threshold voltage of 0.8 V. Upon increase of the Si content, decreased μ_{FE} was observed in proceeding from ZTO to SZTO. As mentioned above, the oxygen vacancies in such systems are produced via dihydroxylation of M-OH and the alloy mechanism. The crystallinity of the SZTO films with different amounts of Si were next investigated via examination of the XRD patterns. As shown in Fig. 3, the broad peak revealed the solution processed SZTO films to be in the amorphous phase. No sharp peaks were observed in the XRD spectra. The amorphous phase of an active channel layer is an important point, because carrier transport in the channel layer of TFTs is considerably affected by the phase structure of the channel layer. The (n-1) d10ns0 electronic configuration of the metal elements in oxide semiconductors, such as ZnO, In-ZnO, and Si-In-ZnO, enables the formation of electron transport paths through the series of s orbitals [10]. Figure 4 shows the tapping-mode AFM images of 30-nm-thick ZTO and SZTO films on Si/SiO_2 substrates. These films exhibited rms roughness values of 0.66 nm and 0.58 nm, respectively. The important transistor characteristic for TFT application is the device subthreshold swing.

$$S = \frac{\partial V_{GS}}{\partial \log I_{DS}}$$

As in previous articles, the decrease in the subthreshold swing may be attributed to the interface and bulk trap density of the TFTs [11]. In general, charge trapping is characterized by the total trap density (N_t), including the bulk trap density (N_b) of the channel layer and the interface trap density (N_{it}) between the dielectric/channel. The decrease in the SS value can be attributed to the existing trap density in deep level states in the channel layer, including interface trap and bulk trap density. The addition of

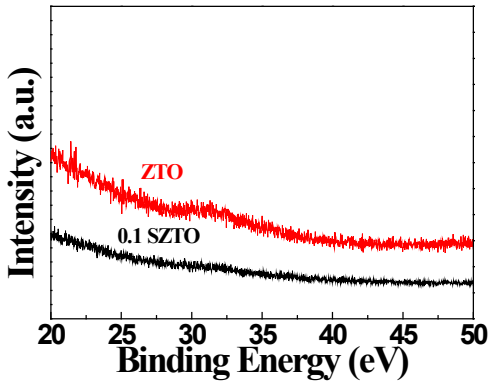

Fig. 3. XRD results of the ZTO and SZTO thin films annealed at 500℃.

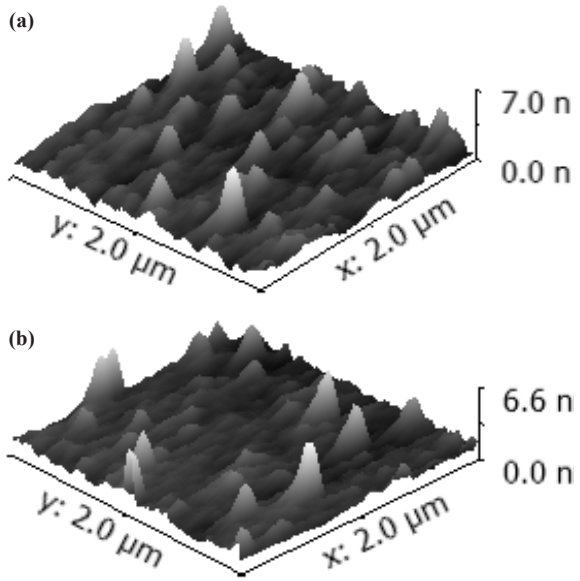

Fig. 4. AFM images of 30-nm-thick ZTO and SZTO films deposited on 200 nm thermal SiO_2.

silicon atoms to the SZTO active layer causes the degeneration of oxygen vacancies since silicon can act as a carrier suppressor, consequently leading to a decrease in the on-current of the TFTs with increasing silicon content. The SS value also provides important information about the quality of a TFT. It is related to the N_{it} near the semiconductor/gate dielectric interface, by the equation:

$$N_{it} = \left[\frac{S\log(e)}{kT/q} - 1\right]\frac{C_i}{q}$$

where Ci, q, and k are the gate dielectrics capacitance per area, elementary charge, and the Boltzmann constant, respectively. In the case of SZTO channel TFTs, the trap site is observed near the conduction band edge, and is related to the doubly ionized oxygen vacancies [12-14]. The addition of silicon reduced the oxygen vacancy concentration in the SZTO channel. As a result, the N_{it} was considerably decreased, which contributed to improvement of the subthreshold swing characteristics. The N_t in the SZTO systems was decreased from 4.39×10^{12} to 1.45×10^{11} through its relation with the oxygen vacancy, which could be controlled by the addition of silicon to the SZTO system. Moreover, the SZTO TFTs are also suitable for fast switching devices due to their low S.S value of 0.28 V/decade.

4. CONCLUSIONS

In summary, SZTO thin film transistors were fabricated using the solution process. The incorporation of Si reduced the oxygen vacancies, acting as an oxygen binder. The Si acted as a carrier suppressor, allowing the SZTO TFT to achieve the following electrical properties: V_{th} = 0.8 V, μ_{FE} = 0.70 cm^2 / V^1 s^1, S.S = 0.28 V/decade, and $I_{on/off} = 1.66 \times 10^7$. The annealing temperature of the solution processed oxide channel layer was high, at over 500℃. Moreover, with optimized semiconductor interfaces, the solution processed metal oxide device performance was enhanced to levels comparable to vacuum-deposited polysilicon or optimized metal oxide films.

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