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전기 자동차 배터리 충전장치용 3상 3스위치 전류형 정류기의 전류 왜곡 감소를 위한 펄스 폭 변조 스위칭 기법

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Reduced Current Distortion of Three-Phase Three-Switch Buck-Type Rectifier using Carrier Based PWM in EV Traction Battery Charging Systems

Beomseok Chae[1], Taewon Kang[1], Tahyun Kang[1], and Yongsug Suh†

Abstract

This study investigates an economic and highly efficient power-converter topology and its modulation scheme for 60 kW rapid EV charger system. The target system is a three-phase three-switch buck-type rectifier topology. A new carrier-based PWM scheme, which is characterized by simple implementation using logic gates, is introduced in this paper. This PWM scheme replaces the diode rectifier equivalent switching state with an active switching state to produce the same effective current flowing path. As a result, the distortion of input current during the polarity reversal of capacitor line voltage can be mitigated. The proposed modulation technique is confirmed through simulation verification. The proposed modulation technique and its implementation scheme can expand the operation range of the three-phase three-switch buck-type rectifier with high-quality AC input and capacitor ripple current.

Key words: Three-phase three-switch buck-type rectifier, Current distortion, Carrier based PWM, Current source converter

1. Introduction

With recent worldwide interest in green energy, various research projects on eco-friendly vehicles, typically electric vehicles (EVs) have gained much interest. EVs do not emit any harmful gasses locally, which has positive impact on air quality in the urban environment and public health as well[1]. Furthermore, EVs are more energy efficient in terms of kWh/km. In EVs and PHEVs, a battery is used as the main power source, so that battery charger is treated as the core technology[1,2]. Various topologies and control methods have been developed for EVs chargers. Among these circuit topologies, three-phase three-switch buck-type rectifier is one candidate topology for EV chargers that has just one switch per leg, and single stage structure. Due to the reduced switch count, this structure has the advantage of low cost. In addition, the step-down output dc voltage level generated by three-phase three-switch buck-type rectifier is suitable for EV battery charging system connected to the standard ac grid. This topology can regulate the dc-link current to achieve various charging modes, i.e. CC or CV, etc. These characteristics of three-phase three-switch buck-type rectifier make this topology one of many feasible candidates for EV charging systems.

Three-phase three-switch buck-type rectifier consists of 4 diodes and one switch per leg[3]. This switch drives converter input current in bi-directional flow. For this reason, three-phase three-switch

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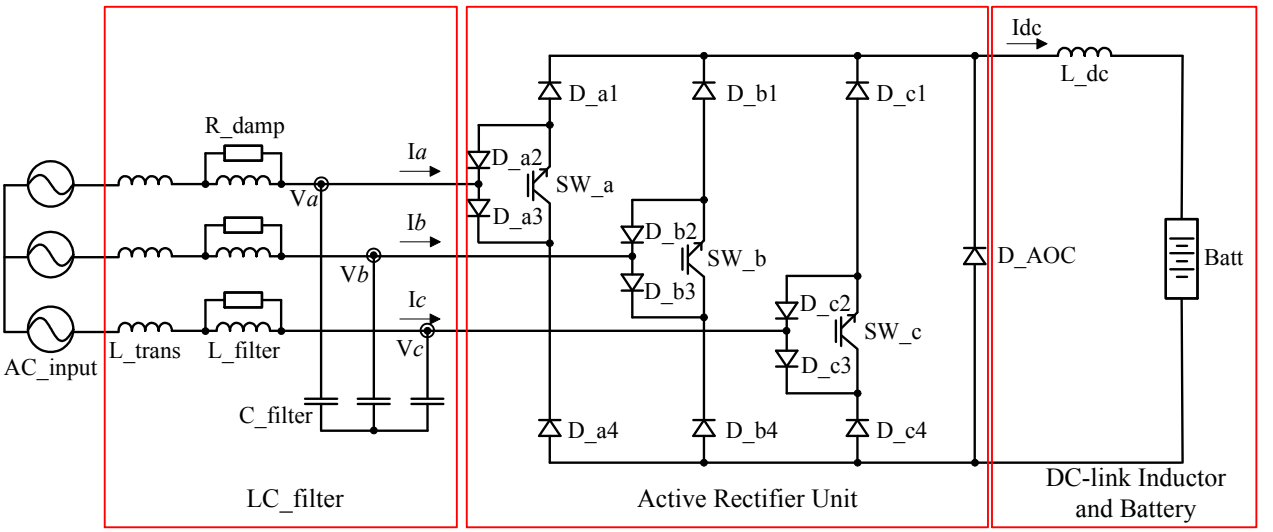

Fig. 1. Schematic of three-phase three-switch buck-type rectifier for EV charging system.

buck-type rectifier needs a different modulation method from those of conventional two-level voltage source rectifiers. Operation of three-phase three-switch buck-type rectifier depends on various PMW scheme such as Carrier Based PWM (CBPWM) and Space Vector PWM (SVPWM)[4,5]. However, in the actual realization of the SVPWM algorithms, memory consumption is deliberately sacrificed to achieve a reduction in the computation time of the algorithm as compared to CBPWM[6]. Conventional CBPWM scheme designed for three-phase three-switch buck-type rectifier has a limited operation range with respect to the power factor angle[4]. This conventional modulation scheme gives an affordable switching action only under the operation of unity power factor. However, when the power factor departs from unity, the conventional CBPWM scheme starts to generate switching harmonics and distortion of input current which poses a serious problem in the practical application of three-phase three-switch buck-type rectifier in EV charging systems.

This paper proposes the advanced modulation strategy based on CBPWM. Proposed modulation strategy has a more improved current THD than conventional CBPWM strategy under out-of-phase conditions. CBPWM scheme is implemented in this paper with simple digital logic functional blocks. Proposed modulation strategy has a wider operation range than conventional modulation strategy. This wider operating range effectively reduces the distortion of grid current and converter input current of EV charging systems. Therefore, the proposed modulation strategy results in low-cost and high-performance EV rapid charging systems. This paper is structured as the following. In section 2, the operating characteristics of three-phase three-switch buck-type rectifier are described. Section 3 and section 4 present the conventional modulation strategy and proposed modulation strategy. In section 5, the characteristics of the proposed modulation method are verified by simulation results.

2. Operation of three-phase three-switch buck-type rectifier

In the basic operation of the circuit, the three switches can exercise complete control over the conduction of all the respective branches. There are three states of current commutation, i.e. *Freewheeling mode*, *Two-switch turn-on mode*, and *Diode rectifier mode* (all switches are turn-on)[7]. *Freewheeling mode* corresponds to the case when just one switch is turned on or all switches are turned off. In this mode, the current path is not connected to ac side resulting in a zero switching vector with zero converter input currents. Second, *Two-switch turn-on mode* implies the case when two out of three active switches are turned on. During this mode the effective current path is determined by the polarity of line voltages across the input capacitors. That is, the phase with larger supply voltage is connected to the positive bar and the phase with smaller supply voltage to the negative bar of the dc link. Third,

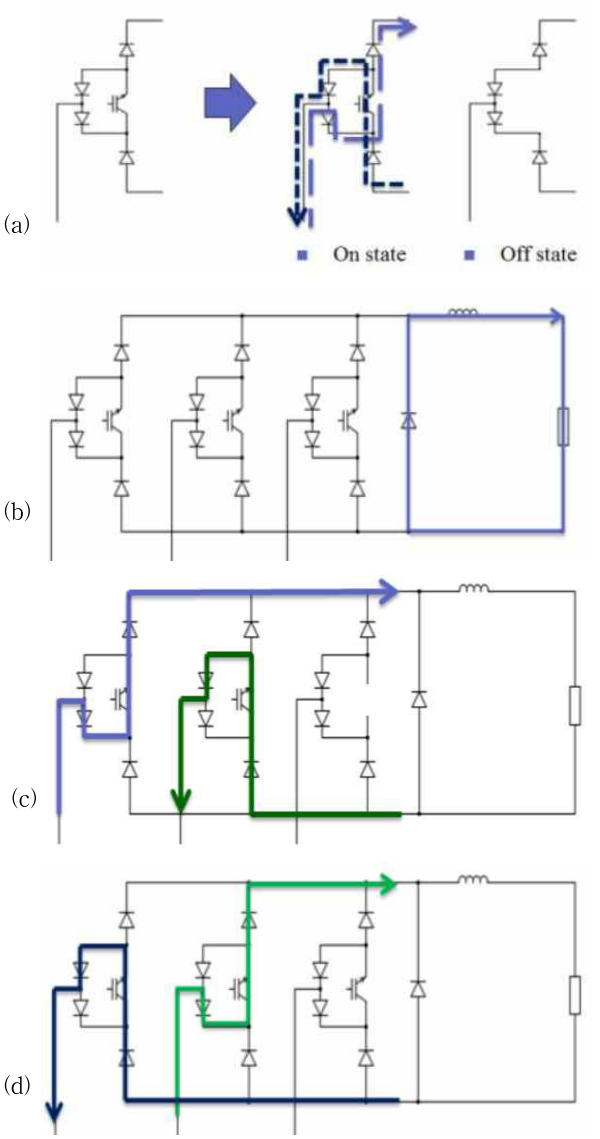

Fig. 2. Operation of three-phase three-switch buck-type rectifier (a) switch on-off operation of single leg, (b) free-wheeling mode, (c) active switching mode under $Va>Vb$, (110), (d) Diode rectifier mode under $Va<Vc<Vb$, (111).

Diode rectifier mode represents the case when all switches are turned on. The input phase of largest voltage amplitude is connected to the positive bar and the input phase of smallest voltage amplitude to the negative bar of the dc link. Converter input currents under each switching state are presented in Table I. When all IGBTs are conducting, i.e. Diode rectifier mode, the phase currents and switching states depend on the actual polarity of capacitor line voltages. In Table II, the period of a-phase current is divided into six intervals according to the relative magnitude of three-phase converter input currents, that is the fundamental components of converter input currents.

TABLE I
ACTIVE SWITCHING AND ZERO SWITCHING STATE

Switching State (SW_a, SW_b, SW_c)	I*a*	I*b*	I*c*	Zero/Active
(000)	0	0	0	Zero Switching
(100), (010), (001)	0	0	0	Zero Switching
(110)	±I*dc*	∓I*dc*	0	Active Switching
(011)	0	±I*dc*	∓I*dc*	Active Switching
(101)	±I*dc*	0	∓I*dc*	Active Switching
(111)	±I*dc*	±I*dc*	±I*dc*	Active Switching

TABLE II
SECTORS OF CONVERTER INPUT CURRENT

Sector	Converter input current	a-phase current angle(degree)
S1	I*a*>I*c*>I*b*	30~90
S2	I*a*>I*b*>I*c*	90~150
S3	I*b*>I*a*>I*c*	150~210
S4	I*b*>I*c*>I*a*	210~270
S5	I*c*>I*b*>I*a*	270~330
S6	I*c*>I*a*>I*b*	330~30

3. Conventional modulation strategy

Input currents are dependent on the relative amplitude of three phase capacitor voltages under the diode rectifier mode having the switching state of (111). The path of current flowing is changed when the polarity of input capacitor line voltage is changed. In Sector 1, a-phase current path is connected to the positive bar in dc-side, b-phase current path is connected to the negative bar in dc-side, and c-phase current becomes zero under in-phase condition. As the voltage condition is changed from in-phase to out-of-phase condition, that is, the angle of input current is not same as that of capacitor voltage, the positive and negative dc-link are connected to different ac phases as compared to in-phase condition. Therefore, the transition of voltage phase conditions may have a crucial impact on the path of current flowing. This leads to the distortion of converter input current when the converter input current and capacitor voltage have a phase angle difference.

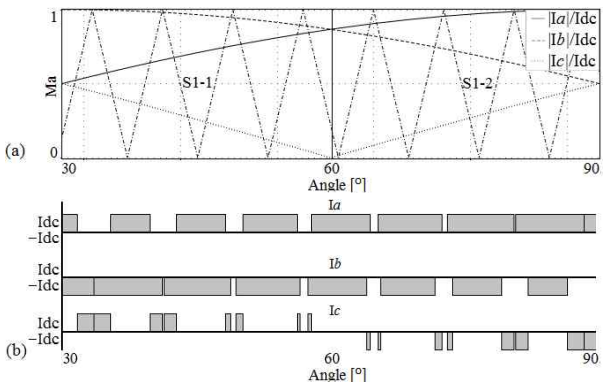

Fig. 3. Waveforms at sector S1 (I*a*>I*c*>I*b*) (a) absolute modulation signal of converter input currents and triangular carrier waveform, (b) converter input current of each phase under (V*a*>V*c*>V*b*).

TABLE Ⅲ
ACTIVE SWITCHING AND ZERO SWITCHING STATE AT SECTOR S1 (I*a*>I*c*>I*b*) UNDER (V*a*>V*c*>V*b*)

Sector S1-1 (30°~60°)				Sector S1-2 (60°~90°)			
Switching State	I*a*	I*b*	I*c*	Switching State	I*a*	I*b*	I*c*
(001)	0	0	0	(001)	0	0	0
(011)	0	-I*dc*	I*dc*	(101)	I*dc*	0	-I*dc*
(111)	I*dc*	-I*dc*	0	(111)	I*dc*	-I*dc*	0

One leg of three-phase three-switch buck-type rectifier is driven by only one switch unlike the popular 2-level voltage source converter. This switch drives both positive current and negative current at ac side. Owing to this fact, a rectified reference current of positive amplitude, instead of bipolar sinusoidal reference, is compared with a unipolar triangular carrier at switching frequency in pulse width modulator. This PWM action is explained in Fig. 3 for the particular case of Sector 1 (I*a*>I*c*>I*b*).In Fig. 3, for the sake of simplicity, the converter input currents are assumed to be in-phase with the corresponding filter capacitor voltages (V*a*>V*c*>V*b*) in Sector 1. In PWM action, the three modulating signals of I*a*/I*dc*, I*b*/I*dc*, and I*c*/I*dc* are compared with a unipolar triangular waveform. The particular phase current whose amplitude is either largest or smallest among three phase current values is put under PWM action. For example, in Sector 1, the phase-*a* current (I*a*) has the largest amplitude and the phase-*b* (I*b*) has the smallest amplitude, i.e. I*a*>I*c*>I*b*. Therefore, in Sector 1, both modulating signals of I*a*/I*dc* and I*b*/I*dc* are compared with a unipolar triangle carrier waveform to generate pulse width modulated waveforms of I*a* and I*b* as shown in Fig. 3. The polarity of modulated waveforms of I*a* and I*b* are determined by the relative magnitude of capacitor voltages of corresponding phases, i.e. V*a* and V*b*. For example, in Sector 1, the phase-*a* voltage (V*a*) has the larger amplitude than that of phase-*b* (V*b*). Therefore, the phase-*a* current (I*a*) has the positive amplitude while the phase-*b* current (I*b*) has the negative amplitude as illustrated in Fig. 3.

In general, the switch of the phase whose amplitude of current reference is at median among three phase currents is kept turned on during the complete interval of that particular sector irrespective of PWM action, e.g. SW_c in Sector 1. When all switches are turned on, i.e. *Diode rectifier mode*, the switch of median-phase does not carry the current since the current only flows through the switches of largest-phase and smallest-phase. On the other hand, when the switch of median-phase is turned on either with the switch of largest-phase or smallest-phase, the polarity of corresponding phase current is determined by the relative magnitude of capacitor voltages. For example, in Sector 1, when SW_b and SW_c are turned on, the phase-*c* current (I*c*) has the positive amplitude while the phase-*b* current (I*b*) has the negative amplitude as illustrated in Fig. 3. In the similar manner, when SW_a and SW_c are turned on, the phase-*a* current (I*a*) has the positive amplitude while the phase-*c* current (I*c*) has the negative amplitude. According to the PWM action as described in Fig. 3, a total of three possible switching states can be generated in each sector. These switching states and the polarity of corresponding phase currents are summarized in Table Ⅲ under the particular operating condition of Sector 1.

As described in Fig. 3, the switch of largest-phase and smallest-phase are controlled by PWM action while the switch of median-phase is kept turned on. This modulation technique can still generate three phase currents of sinusoidal waveform because, as long as two phase currents out of three phase currents are modulated to generate the sinusoidal waveform, the remaining phase current naturally follows the sinusoidal waveform, i.e. I*a*+I*b*+I*c*=0.

4. Proposed modulation strategy

State-of-the-art solutions of the carrier-based PWM

TABLE Ⅳ
PHASE CURRENT UNDER VARIOUS POWER FACTOR CONDITIONS IN SECTOR 1-1 AND SECTOR 1-2 WITH CONVENTIONAL METHOD

Sector S1-1 Ia>Ic>Ib(|Ib|>|Ia|>|Ic|)									
	Vc>Va>Vb 0°<leading angle<30°			Va>Vc>Vb In-phase			Va>Vc>Vb 0°<lagging angle<30°		
	Ia	Ib	Ic	Ia	Ib	Ic	Ia	Ib	Ic
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0
(011)	0	-Idc	Idc	0	-Idc	Idc	0	-Idc	Idc
(111)	0	-Idc	Idc	Idc	-Idc	0	Idc	-Idc	0
Sector S1-2 Ia>Ic>Ib(|Ia|>|Ib|>|Ic|)									
	Va>Vc>Vb 0°<leading angle<30°			Va>Vc>Vb In-phase			Va>Vb>Vc 0°<lagging angle<30°		
	Ia	Ib	Ic	Ia	Ib	Ic	Ia	Ib	Ic
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0
(101)	Idc	0	-Idc	Idc	0	-Idc	Idc	0	-Idc
(111)	Idc	-Idc	0	Idc	-Idc	0	Idc	0	-Idc

TABLE Ⅴ
PHASE CURRENT UNDER VARIOUS POWER FACTOR CONDITIONS IN SECTOR 1-1 AND SECTOR 1-2 WITH PROPOSED METHOD

Sector S1-1 Ia>Ic>Ib(|Ib|>|Ia|>|Ic|)									
	Vc>Va>Vb 0°<leading angle<30°			Va>Vc>Vb In-phase			Va>Vc>Vb 0°<lagging angle<30°		
	Ia	Ib	Ic	Ia	Ib	Ic	Ia	Ib	Ic
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0
(011)	0	-Idc	Idc	0	-Idc	Idc	0	-Idc	Idc
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0
Sector S1-2 Ia>Ic>Ib(|Ia|>|Ib|>|Ic|)									
	Va>Vc>Vb 0°<leading angle<30°			Va>Vc>Vb In-phase			Va>Vb>Vc 0°<lagging angle<30°		
	Ia	Ib	Ic	Ia	Ib	Ic	Ia	Ib	Ic
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0
(101)	Idc	0	-Idc	Idc	0	-Idc	Idc	0	-Idc
(110)	Idc	-Idc	0	Idc	-Idc	0	Idc	-Idc	0

for three-phase three-switch buck type rectifier usually maintain turn-on state for the switch of the phase whose current reference amplitude is at median among three phases as explained in Fig. 3. For example, In Sector 1, the switch of phase-*c*, SW_*c*, is kept turn-on as described in Table Ⅲ. This modulation scheme causes a trouble when the angle of converter current departs from that of filter capacitor phase voltage. This problem is described in Table Ⅳ. In general, the three-phase three-switch buck type rectifier operates as a current source type converter. Therefore, the switches are modulated to generate the reference current signals of sinusoidal waveform. In other words, the modulated current waveforms should be determined by the reference current signals independent of the relative magnitude of filter capacitor phase voltages. In Sector 1-1 under the in-phase condition, the three possible active switching states generate correct pattern of converter input current as same as those in Table Ⅲ. This pattern of converter input current is correctly maintained as long as the phase angle difference between the converter input current and filter capacitor voltage is less than 30 (lagging). However, as the phase angle difference departs from zero to leading side, the pattern of converter input current especially under the diode rectifier mode (111) is altered from that of in-phase condition as shown in Table Ⅳ. This incorrect pattern of modulated converter input current under the condition of leading angle would lead to the distortion of converter input current.

An advanced modulation scheme and its simple digital implementation method is proposed in order to prevent the converter input current distortion due to diode rectifier mode having the switching state of (111). This is made possible by replacing the switching state of (111) by its equivalent active switching state depending on the operating sector. For example, under the operation in Sector 1, instead of diode rectifier mode (111), the active switching state of (110) is selected. This active switching state (110) generates the effectively same path of current flowing thus resulting in the same modulated input current pattern as shown in Table Ⅴ. Table Ⅴ describes this replacement of diode rectifier mode by the corresponding active switching state in the case of Sector 1. This replacement of diode rectifier mode makes it possible that the current path is less affected by the transition of voltage phase conditions. The same criteria are applied at the other sectors.

In this paper, the advanced modulation scheme

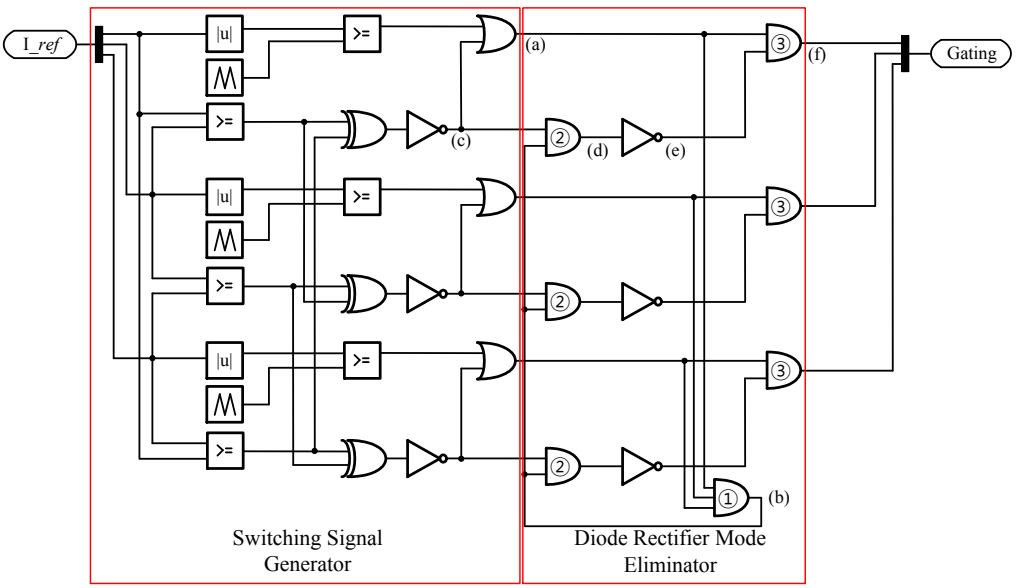

Fig. 4. Proposed modulation block.

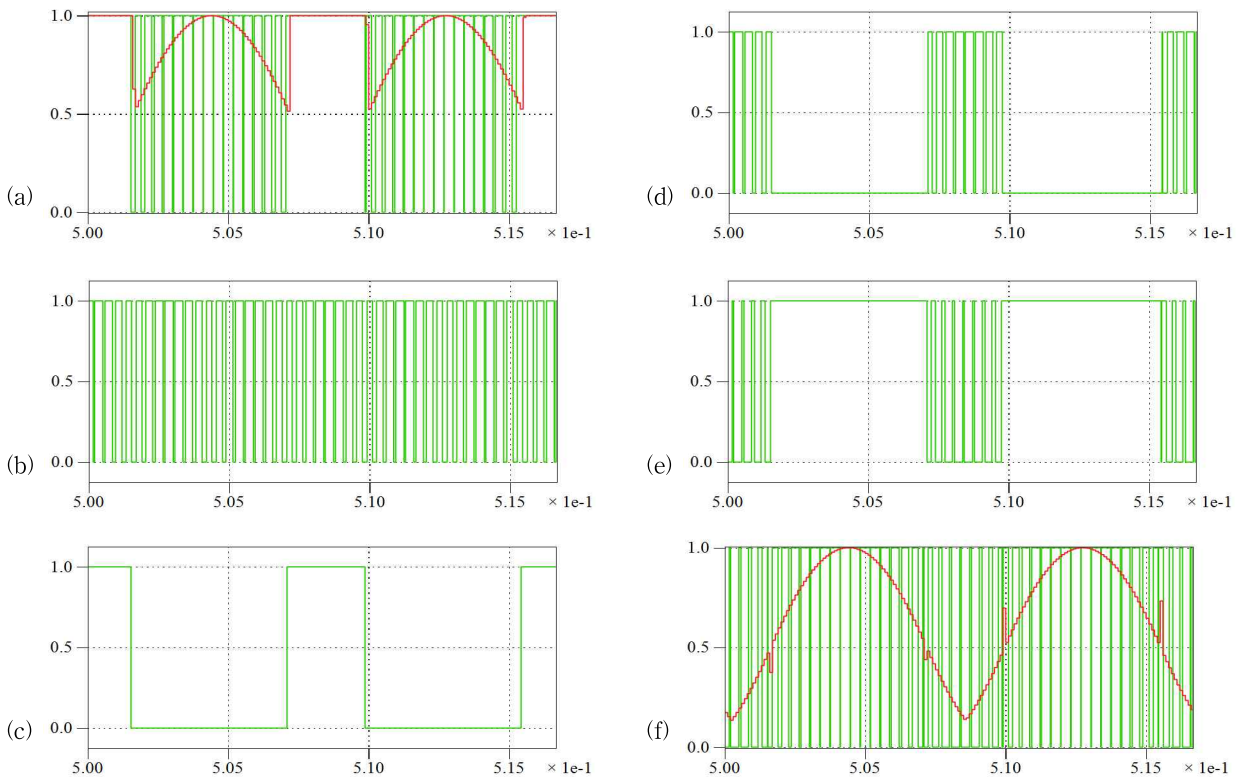

Fig. 5. Operating waveforms at the particular locations in the proposed modulator in Fig. 4 (a) gate output signal of phase-*a* and its local average waveform of conventional method, (b) output signal from diode rectifier mode eliminator, (c) logic signal of phase-*a* displaying the median-phase mode for phase-*a*, (d) output signal from diode rectifier mode eliminator sampled at the median-phase mode for phase-*a*, (e) inverse signal of (d), (f) final gate output signal of phase-*a* of proposed modulator and its local average waveform.

without diode rectifier mode is newly implemented in Carrier Based PWM. The practical implementation of this CBPWM scheme using digital logic gates is presented in Fig. 4. The key waveforms at the particular locations in the modulator gate block are illustrated in Fig. 5. In Fig. 4, *Switching Signal Generator* is the basic modulator function block in which a modulating rectified sine wave of current

reference is compared with a unipolar triangular carrier waveform. The output waveform of *Switching Signal Generator* function block for phase-a at the node of (a) in Fig. 4 is shown in Fig. 5-(a). This waveform corresponds to that of conventional modulation scheme using diode rectifier mode. As described in the previous sections, this gate signal has diode rectifier mode problem under out-of-phase condition. The function block of *Diode Rectifier Mode Eliminator* finds the switching state of (111) using the logic gate of AND ①. This AND ① is a logical product function of conventional gate signals. Therefore, the output of logic gate AND ① becomes high when the gate signals belong to the switching state of (111). The output signal from *Diode Rectifier Mode Eliminator* function block at the node of (b) in Fig. 4 is shown in Fig. 5-(b). The logic signal shown in Fig. 5-(c) represents the median-phase mode for phase-*a*, i.e. the output state becomes high when the amplitude of phase-*a* reference current (I*a*) is at median among three-phase reference currents (I*a*, I*b*, I*c*). The output of logic gate AND ② corresponds to the logical product of waveforms of Fig. 5-(b) and Fig. 5-(c). In other words, this signal represents the output of diode rectifier mode eliminator block sampled during the median-phase mode for phase-*a*. The waveform of logic gate AND ② output is displayed in Fig. 5-(d). The inverted logic signal of Fig. 5-(d) is shown in Fig. 5-(e). This waveform corresponds to the node of (e) in Fig. 4. Finally, the waveforms of Fig. 5-(a) and Fig. 5-(e) are logically multiplied to each other and the result is illustrated in Fig. 5-(f). This final waveform corresponds to the gate output signal of phase-*a* at the node of (f) in Fig. 4, i.e. the output of AND ③. It is noted that this final gate output signal is different from that of gate output signal from the conventional modulation scheme, i.e. Fig. 5-(a), only during median-phase mode. During median-phase mode, instead of turning on the switch of the corresponding phase as done in the conventional modulation, the switch is turned off under the switching state (111) of diode rectifier mode. The local average waveform of the final gate output signal is also given along with its gate output signal in Fig. 5-(f). This local average waveform confirms the fact that during median-phase mode the gate output signal is sinusoidally modulated instead of being put on-state.

TABLE VI
SPECIFICATIONS OF CHARGING SYSTEM

Parameters	Value
Rated power(P_{rated})	60kW
Rated line voltage($V_{llrated}$)	380V
Rated ac input current (I_{rated})	117A
Frequency(f_{in})	60Hz
Converter switching frequency(f_{sw})	10kHz
Transformer leakage inductance(L_{trans})	73.69uH (0.067 pu)
Filter inductance(L_{filter})	449uH (0.4 pu)
Filter capacitance(C_{filter})	63.48uF (0.1 pu)
Filter resistance(R_{damp})	24.05Ω (5.74 pu)

5. Simulation Results

The proposed modulation block has been simulated using Matlab Simulink and PLECS. The simulation conditions are summarized in TABLE VI. Diode Rectifier Mode Eliminator is also modeled by PLECS.

Figure 6 and 7 describe waveforms of conventional modulation method. In Fig. 6-(a), it shows the gate signal of active switch (SW_a) in phase-*a* leg. It clearly indicates the region of Ma being equal to 1.0. This region corresponds to the mode during which the amplitude of phase-a reference current becomes the median value among references of three-phase currents (I*a*, I*b*, I*c*). Figure 6-(b), (c) and (d) are converter input current waveforms under the different phase angle conditions, i.e. in-phase, 30 degree leading, 30 degree lagging. For the convenience of reading the fundamental component of chopped converter input current, its local average waveform is presented in Fig. 7 along with the actual waveform of filter capacitor voltage. The three different phase angle conditions are clearly visible in Fig. 7. The conventional modulation method exhibits a sinusoidal waveform when the converter input current is in-phase with the capacitor voltage. But when the converter input current operates under out-of-phase condition, current distortion occurs at the boundary of voltage sectors. This current distortion is noted in Fig. 7-(c) and (d).

Figure 8 and 9 illustrate the waveforms generated by the proposed modulation scheme. The waveform of phase-a gate signal shown in Fig. 8-(a) demonstrates

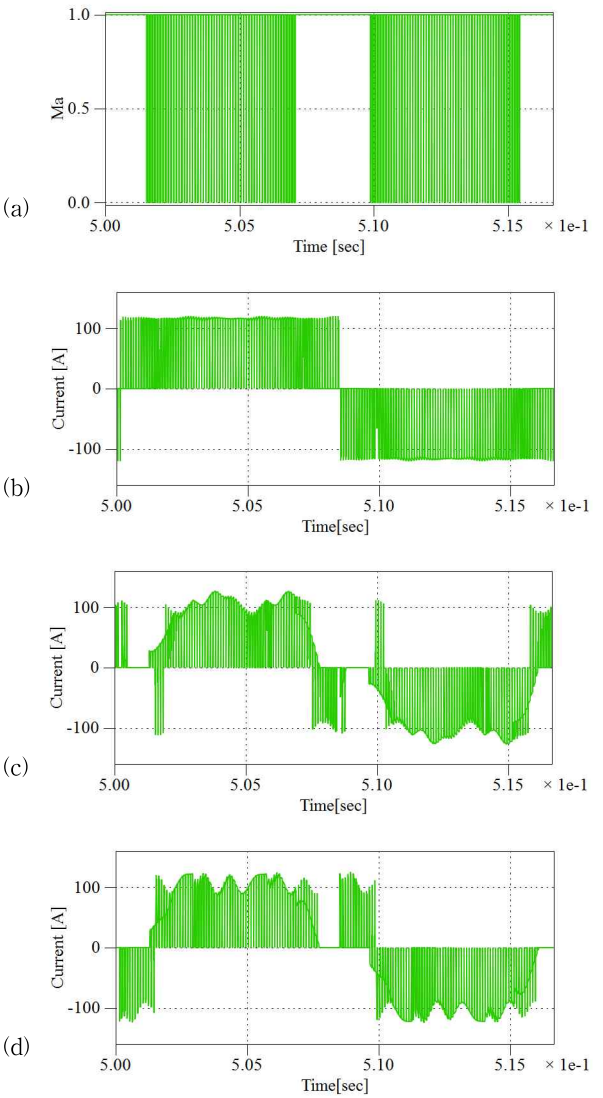

Fig. 6. Gate signal and converter input current (I*a*) waveforms of phase-*a* using conventional modulation (a) gate signal, (b) converter input current (I*a*) under in-phase condition, (c) converter input current (I*a*) under 30 degree leading angle, (d) converter input current (I*a*) under 30 degree lagging angle.

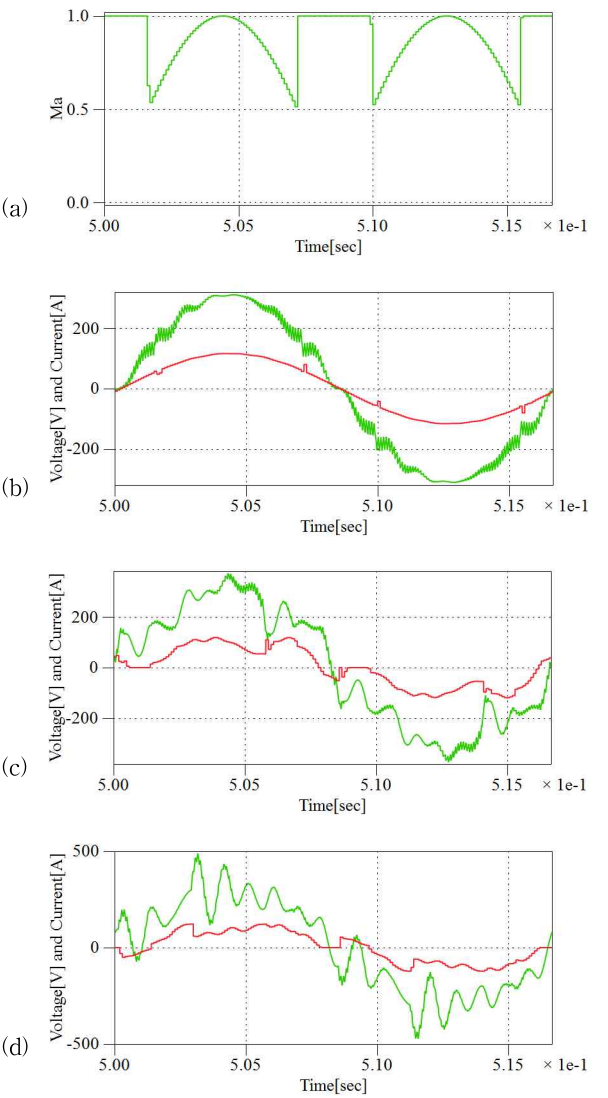

Fig. 7. Local average waveforms of phase-*a* converter input current (I*a*) and exact waveforms of filter capacitor voltage (V*a*) using conventional modulation (a) gate signal, (b) under in-phase condition, (c) under 30 degree leading angle, (d) under 30 degree lagging angle.

the fact that the diode rectifier mode with the switching state of (111) is fully eliminated as compared to the conventional method. The waveform of converter input current is similar to that of conventional method when the current is in-phase with the capacitor voltage as shown in Fig. 8-(b). Under the condition of phase angle difference between the converter input current and capacitor voltage, the distortion of converter input current due to the anomaly of conventional modulation method in diode rectifier mode is mitigated in the proposed modulation scheme. This improved performance of proposed method is clearly visible in Fig. 9-(c) and (d) as compared to those of Fig. 7-(c) and (d).

Figure 10 presents the waveforms of capacitor ripple current (I*cf_abc*) under three different phase angle conditions; in-phase, 30 degree leading, and 30 degree lagging in case of the conventional modulation scheme. In the similar manner, the waveforms of capacitor ripple current for the case of proposed modulation scheme are given in Fig. 11. As noted in the waveforms of converter input current, the capacitor ripple currents also exhibit the fact that the proposed modulation scheme successfully mitigates the

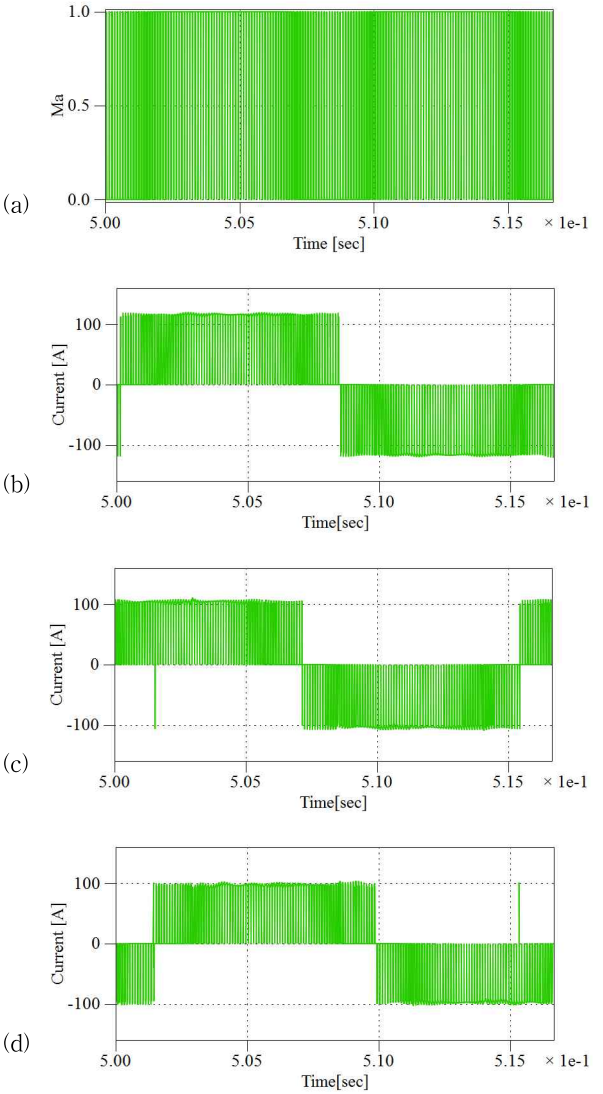

Fig. 8. Gate signal and converter input current (I*a*) waveforms of phase-*a* using proposed modulation (a) gate signal, (b) converter input current (I*a*) under in-phase condition, (c) converter input current (I*a*) under 30 degree leading angle, (d) converter input current (I*a*) under 30 degree lagging angle.

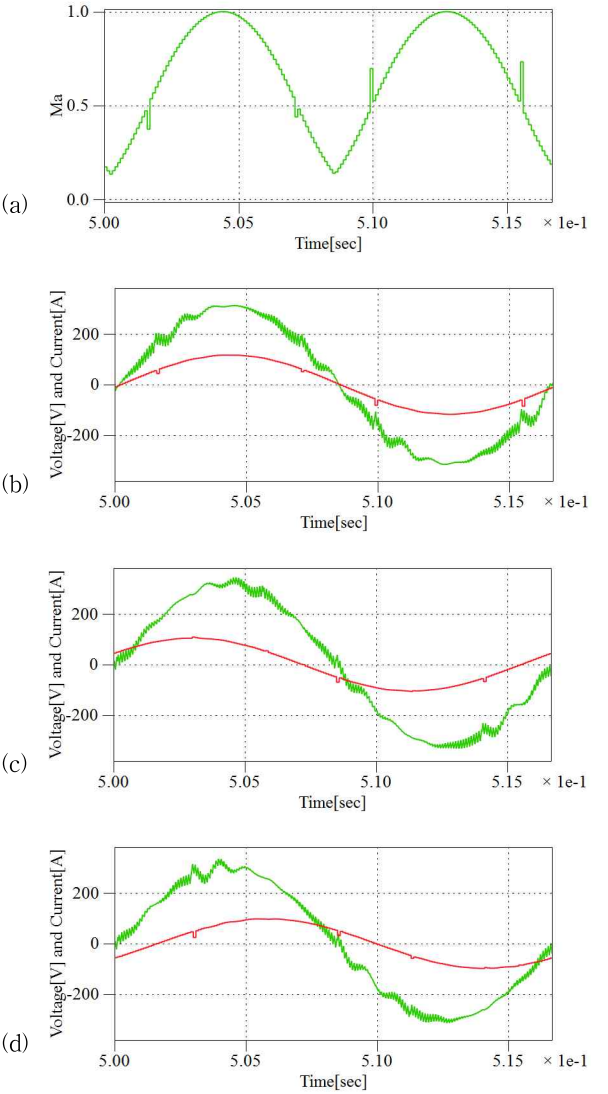

Fig. 9. Local average waveforms of phase-*a* converter input current (I*a*) and exact waveforms of filter capacitor voltage (V*a*) using proposed modulation (a) gate signal, (b) under in-phase condition, (c) under 30 degree leading angle, (d) under 30 degree lagging angle.

current distortion under the out-of-phase conditions. This reduction of harmonic distortion in capacitor ripple current has a positive influence on the life cycle of filter capacitor which is one of critical components in current source converters.

The waveforms of grid input currents (I*g_abc*) are described in Fig. 12 and 13 for the cases of conventional modulation and proposed modulation scheme, respectively. Under the phase angle difference of 30 degree leading, the grid input currents become quite distorted with THD of 47.5%. Also, under the phase angle difference of 30 degree lagging, the THD of grid input currents is deteriorated to 50.1%. The proposed modulation scheme mitigates this current distortion problem leading to better THD. By employing the proposed modulation scheme, THD of grid input current is improved to reach the level of 4.9% and 4.8% under the phase angle difference of 30 degree leading and 30 degree lagging, respectively. That is shown in Table VII.

Figure 14 and 15 show the Fourier spectrum of grid input current. In Fig. 14, the conventional modulation method contains 5th, 7th, 11th, 13th, and higher odd-order harmonics under out-of-phase

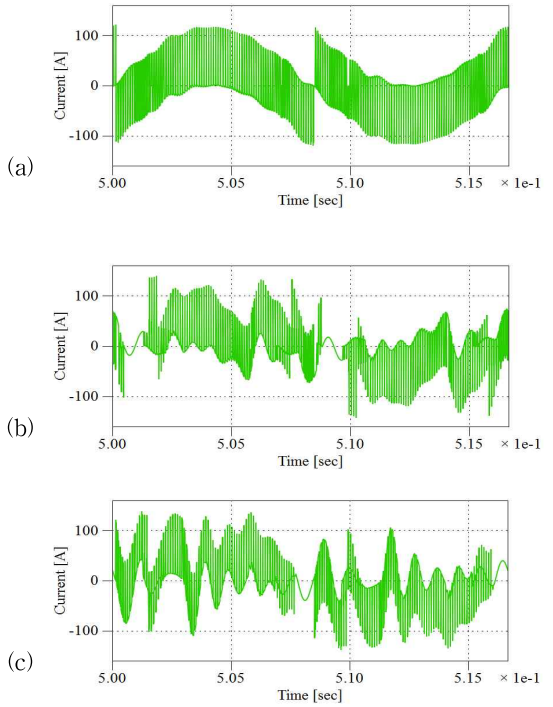

Fig. 10. Waveforms of capacitor ripple current of phase-*a* (I*cf_a*) using conventional modulation (a) under in-phase condition, (b) under 30 degree leading condition, (c) under 30 degree lagging condition.

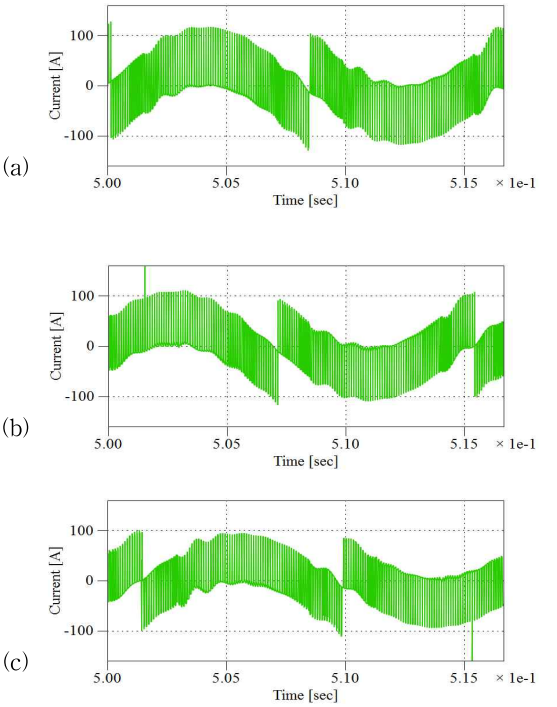

Fig. 11. Waveforms of capacitor ripple current of phase-*a* (*Icf_a*) using proposed modulation (a) under in-phase condition, (b) under 30 degree leading condition, (c) under 30 degree lagging condition.

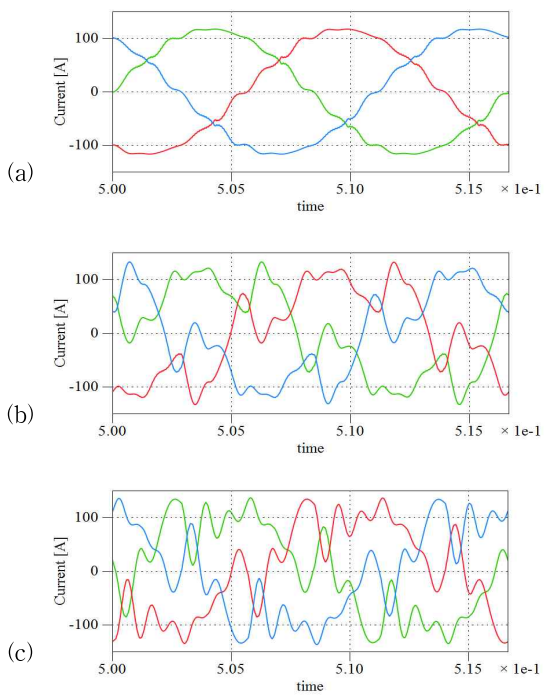

Fig. 12. Waveforms of three-phase grid input current (I*g_abc*) using conventional modulation (a) under in-phase condition, THD=4.3%, (b) under 30 degree leading condition, THD=47.5%, (c) under 30 degree lagging condition, THD=50.1%.

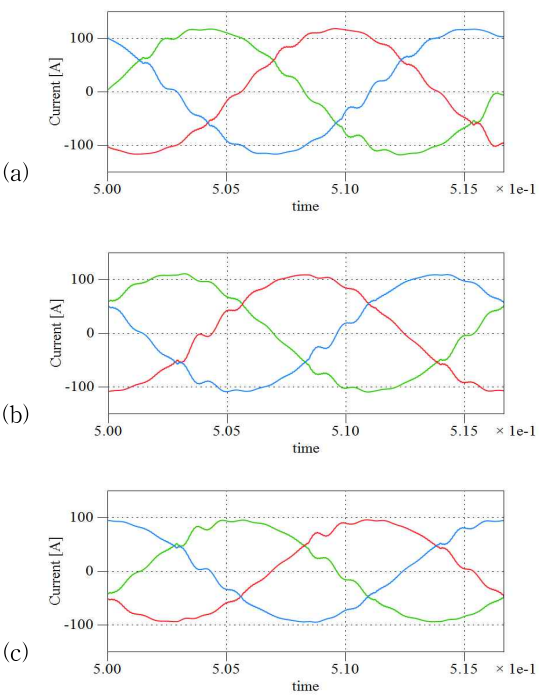

Fig. 13. Waveforms of three-phase grid input current (I*g_abc*) using proposed modulation (a) under in-phase condition, THD=4.8%, (b) under 30 degree leading condition, THD=4.9%, (c) under 30 degree lagging condition, THD=4.8%.

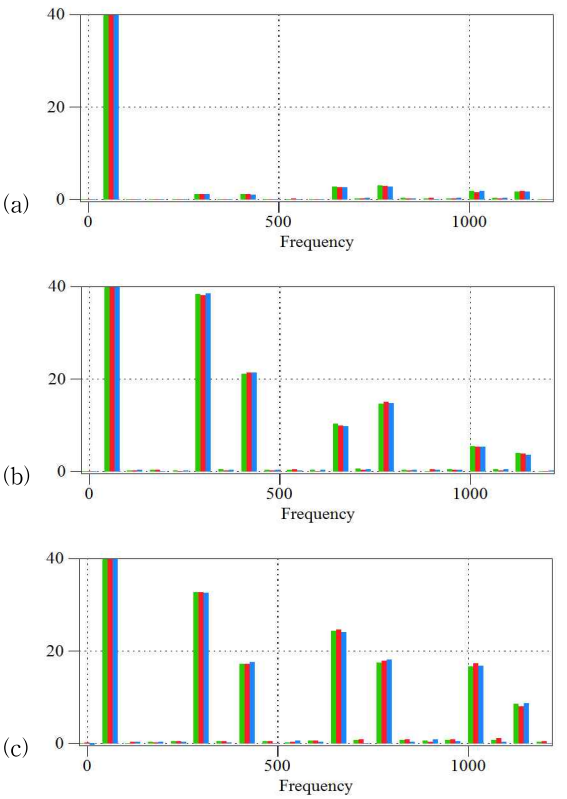

Fig. 14. Fourier spectrum of grid input current (I*g_abc*) using conventional modulation (a) under in-phase condition, (b) under 30 degree leading condition, (c) under 30 degree lagging condition.

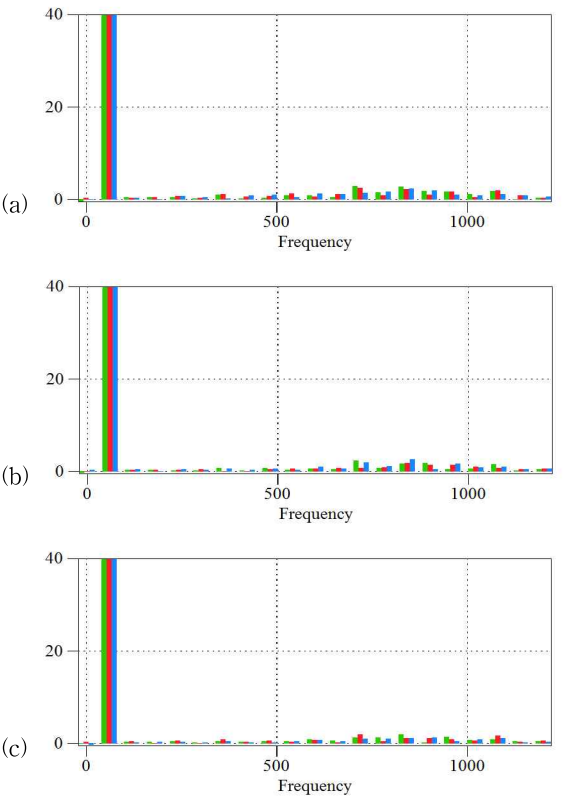

Fig. 15. Fourier spectrum of grid input current (I*g_abc*) using proposed modulation (a) under in-phase condition, (b) under 30 degree leading condition, (c) under 30 degree lagging condition.

TABLE Ⅶ
SPECIFICATIONS OF CHARGING SYSTEM

	Grid current THD - Conventional modulation	Grid current THD - Proposed modulation
In-phase condition	4.3%	4.8%
30 degree leading condition	47.5%	4.9%
30 degree lagging condition	50.1%	4.8%

conditions. But proposed modulation method has smaller harmonics resulting in ac grid currents of better quality than conventional modulation method even under the condition of out-of-phase angle.

As a result, the proposed modulation scheme along with the digital logic circuit implementation eliminating diode rectifier mode from the conventional modulation scheme is successfully verified through these simulation results. Experimental verification is under progress and the result will be reported in future publications.

6. Conclusion

The three-phase three-switch buck-type rectifier has become one of many feasible converter topologies suitable for EV charging systems due to its low cost and simple structure in addition to the generic feature of voltage step-down. The major challenge of this topology lies in the fact that, due to the current source structure, the modulation is not straightforward as in most of voltage source type converters. Conventional modulation schemes suffer from the fact, in the existence of phase angle difference between the converter input current and capacitor voltage, the switching states experience anomaly due to uncontrolled diode rectifier mode. The proposed modulation scheme solves this disadvantage of conventional modulation scheme during the transition

of voltage sector by eliminating diode rectifier mode and replace with equivalent active switching vector depending on the voltage phase conditions under transition. The proposed modulation scheme is implemented as carrier based PWM using simple logic gates. The proposed method is confirmed through simulation verification. The distortion of input current observed in the case of conventional modulation schemes is successfully mitigated in the proposed scheme. As a result, the proposed modulation technique and its implementation scheme can expand the operation range of the three-phase three-switch buck-type rectifier having ac input and capacitor ripple current of high quality.

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