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# Design and Research on High-Reliability HPEBB Used in Cascaded DSTATCOM

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## Abstract

The H-bridge inverter is the fundamental power cell of the cascaded distribution static synchronous compensator (DSTATCOM). Thus, cell reliability is important to the compensation performance and stability of the overall system. The concept of the power electronics building block (PEBB) is an ideal solution for the power cell design. In this paper, an H-bridge inverter-based "plug and play" HPEBB is introduced into the main circuit and the controller to improve the compensation performance and reliability of the device. The section that discusses the main circuit primarily emphasizes the design of electrical parameters, physical structure, and thermal dissipation. The section that presents the controller part focuses on the principle of complex programmable logic device -based universal controller This section also analyzes typical reliability and anti-interference issues. The function and reliability of HPEBB are verified by experiments that are conducted on an HPEBB test-bed and on a 10 kV/± 10 Mvar DSTATCOM industrial prototype.

**Key words:** Anti-interference, Cascaded multilevel, CPLD, DSTATCOM, H-bridge inverter, HPEBB, Module, Reliability

## I. INTRODUCTION

With the progress of science and technology and social development, distribution network encounter serious problems with power quality. This issues are attributed to the many applications of large-capacity and impact reactive loads such as arc furnaces, welding machines, and rolling mills, and non-linear loads such as power electronic devices [1]-[4]. Distribution static synchronous compensator (DSTATCOM) can effectively address the power problems caused by reactive power and harmonics, such as point of common coupling voltage fluctuation and flicker, three-phase imbalance, electromagnetic interference, transmission loss, and noise. DSTATCOM has good application prospects and high research value given its excellent operation performance, including highly accurate static compensation, fast dynamic response, wide operating range, and low output harmonic. Moreover, this compensator has received extensive attention from scholars worldwide [5]-[8].

Fig. 1 shows the schematic of the H-bridge inverter-based cascaded multilevel DSTATCOM. This compensator is simple in structure and facilitates the modular design of the basic H-bridge power cell with convenience. The power cells are connected in series to improve AC output voltage and are controlled by multi-level modulation to increase equivalent switching frequency. The higher equivalent frequency assists in reducing the volume and capacity of the output filter. The modulation method has been widely used in many industrial processes, especially in medium-voltage distribution network where compensation requirements are high. Equipment based on this topology has been investigated in-depth, and achievements have been reported with regard to modeling, the control strategy on the AC and DC sides, operation performance, modulation methods, and the application field [9]-[14].

The reliability, controllability, and scalability of the many power cells for DSTATCOM application are directly related to the overall system in terms of compensation performance and stability. Cell design can be optimized rationally to improve system power density effectively and meet the different voltage and capacity requirements. In the process, the compensation performance and flexibility of devices are enhanced.

The concept of power electronics building block (PEBB) is an ideal solution for the basic DSTATCOM power cell. PEBB is a platform-based approach where basic building blocks are consistent with one another. This approach has a defined

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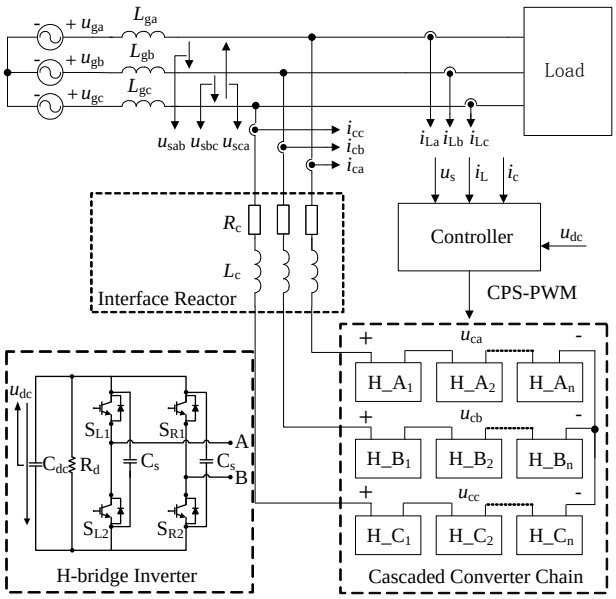



Fig. 1. System configuration of the cascaded DSTATCOM.

functionality, as well as standardized hardware and control interfaces. PEBB technology regards a "plug and play" module as a common standard converter device. The module integrates power electronic devices, systems, and optimization topologies, including power switches, sensors, drive and protection circuits, and controllers. The adoption of building block(s) increases volume production and reduces engineering effort, design testing, onsite installation, and maintenance work. The philosophy of PEBB standardization is outlined in many studies [15]-[17]. In addition, PEBB has often been investigated and applied in the fields of renewable energy, efficiency improvement, electric energy storage, and energy independence through wind, solar, and electric vehicles [18]-[20].

The current paper introduces an H-bridge-based "plug and play" HPEBB integrated with functions such as power conversion, drive, control, detection, and protection. This HPEBB achieves high voltage and large capacity in the main circuit and the controller, as well as high modularization, controllability, scalability, and reliability. The section that introduces the main circuit focuses on the electrical, structural, and thermal dissipation designs. The section that discusses the controller emphasizes the principle of the complex programmable logic device (CPLD) based universal HPEBB controller. This section also analyzes typical reliability and anti-interference issues. Finally, an HPEBB test-bed and a 10 kV/±10 Mvar industrial prototype are established to verify the reliability and availability of the designed HPEBB.

## II. Main Circuit Design

### A. Electrical Parameters

The circuit diagram of the HPEBB is shown in Fig. 1. Each module is composed of the insulated-gate bipolar transistor (IGBT) based H-bridge inverter, the DC link capacitor $C_{dc}$, the discharge resistor $R_d$, and the peak absorption capacitor-based snubber $C_s$. DC voltage is stabilized in operation at a given value $u_{dc}$. Furthermore, the bridge arms switch according to the pulses generated by pulse-width modulation (PWM) technology to obtain the desired fundamental AC output voltage $u_{AB}$.

In IGBT selection, the main considerations are the operating limit of the voltage/current in HPEBB, switching frequency, package, and thermal dissipation. Extreme conditions can be simulated by software. A certain margin can then be derived based on the simulation results. Each bridge arm may be composed of several IGBTs in parallel to meet current and dissipation requirements. An IGBT with a flat bolt structure, such as the Infineon Econodual series, can effectively limit module parasitism through convenient DC bus design [21]. This IGBT is not only suitable for HPEBB modularization, but it also facilitates the transient performance of HPEBB.

DC capacitor is used to support voltage and to filter out DC-side ripples during the HPEBB operation. The design principles of the capacitor is as follows: the DC voltage and the current of capacitors are limited to a safe range in both steady and dynamic states. Withstanding voltage and the capability for ripple current absorption meet the operation requirements. Finally, power loss is low, and the package is fit for modular design. When DSTATCOM is compensating for reactive power, DC voltage fluctuation in the HPEBB during a fundamental cycle can be calculated using Eq. (1), where $\Delta U_{dc}$ is the voltage fluctuation in a fundamental cycle, $\omega$ is the angular frequency, $M$ is the modulation ratio, and $I$ is the peak output current [22]. Then, total capacitance $C_{dc}$ can be determined on the basis of the specified value of DC voltage ripple. Several metalized film capacitors should be presented in parallel to enhance withstanding voltage and the capability for ripple current absorption. The energy stored in the capacitors is released by the discharge resistor $R_d$ when HPEBB stops for operator safety.

$$\Delta U_{dc} = \frac{2MI}{4\omega C_{dc}}. \tag{1}$$

When HPEBB stops running, the energy stored in the DC capacitor should be discharged by the discharge resistor within a specified time according to either the national standard or the standard of the International Electrotechnical Commission (IEC). The discharging time determined using Eq. (2) is mainly considered in resistor selection. The resistance power should be greater than the steady-state loss obtained with Eq. (3) for reliable long-term operation. In addition, resistance precision should be as high as possible because the voltages among different HPEBBs are mainly balanced by the discharge resistor before applying the voltage balancing algorithm during DSTATCOM start-up.

$$\tau = (3 \sim 5) \cdot R_d C_{dc} . \quad (2)$$

$$W_{loss} = U_{dc}^2 / R_d . \quad (3)$$

Absorption capacitors are primarily used to suppress the turn-off voltage spikes in the IGBT to prevent the device from incurring overvoltage damage. The capacitance can be calculated with Eq. (4). The formula indicates the energy conservation between the loop parasitic inductor and the capacitor, where $L$ is the parasitic inductance of the DC bus and IGBT internal leads. The parasitic inductance can be controlled to less than 50 nH by applying plane laminated bus technology. This technology significantly improves the dynamic performance of the device. $U_{max}$ is the maximum allowable voltage overshoot in IGBT.

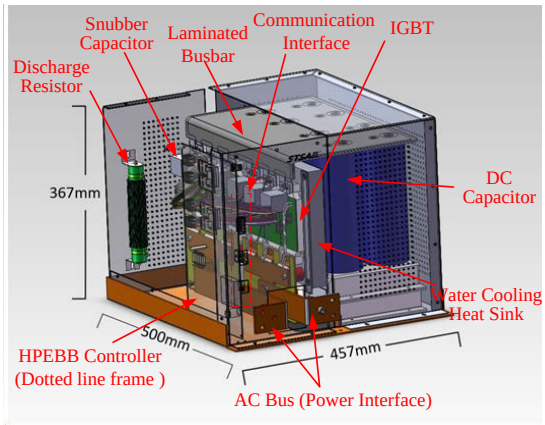
$$\frac{1}{2} L I^2 = \frac{1}{2} C_s U_{max}^2 . \quad (4)$$

### *B. HPEBB Structure Design*

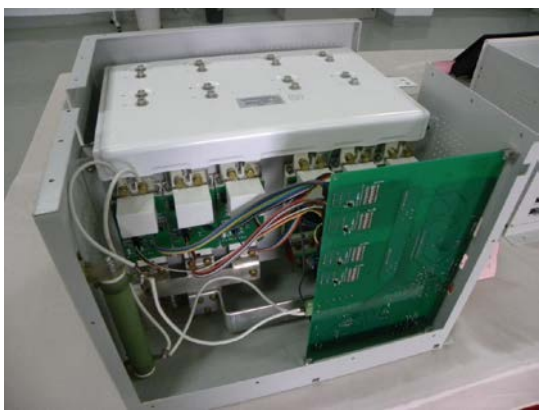
The physical structure is designed by the mechanical drawing software Solid Works. Fig. 2 depicts a sample HPEBB in 3D and presents an image of an actual designed HPEBB. The actual HPEBB has a nominal capacity of 300 kW and a rated output current of 600 A. Each bridge arm is composed of three IGBTs in parallel. The DC side consists of eight metalized film capacitors in parallel. A plane laminated bus-bar is applied to reduce the effect of parasitic parameters. All electrical clearances, creeping distances, and current densities meet the requirements of the IEC standard. Moreover, the electrical margin should be sufficient in case of fault conditions. Structural reliability and installation flexibility are also considered. Given the concept of the PEBB standard and the "plug and play" features, the internal module integrates the control, drive, sensor, and protection functions. The external module reserves only the communication interface for communication with the upper system controller, as well as the AC power interface for linkage with other HPEBBs.

### *C. Thermal Dissipation Design*

The heat loss in each IGBT is the basis for thermal dissipation design. Apart from using the traditional calculation method, heat simulation software such as IPOSIM can be applied to obtain accurate results for detailed parameter settings, targeted circuit topology, and the modulation method. Fig. 3 shows the results for each IGBT as calculated according to the operation conditions of the HPEBB design presented in the previous chapter. The total dissipation of all of the switches can be computed as 2 kW for each HPEBB by adopting a certain margin. A water-cooled heat sink is utilized to dissipate heat. The set rate of water flow should ensure that the maximum temperature of the chip junction of IGBT remains within a safe operation range. In addition, the cooling water must have a resistivity of more than 5MΩ/cm to meet insulation requirements. Fig. 4 depicts the thermal simulation result of the heat sink at 45 °C, as well as the actual




(a)



(b)

Fig. 2. 3D impression and image of the designed HPEBB. (a) 3D impression. (b) Image of the designed HPEBB.

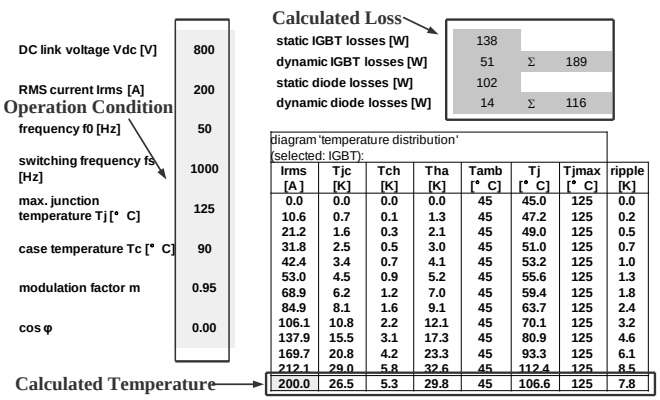



Fig. 3. Results of the thermal simulation and experiment.

temperature rise curve measured for the highest heat point of a real HPEBB. This curve plots the point of temperature rise to the point of balance. According to the device datasheet, the difference in the steady-state temperature of an IGBT junction and the surface of the heat sink is calculated to be 25 °C when operating at nominal condition. The simulation and experimental results both show that the maximum junction temperature is less than 85 °C. Thus, this scenario meets the thermal dissipation requirement.

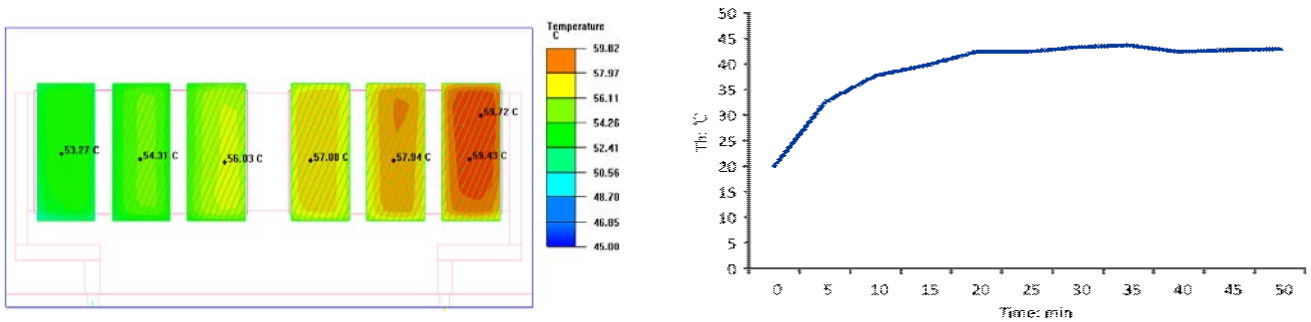



Fig. 4. Results of the thermal simulation and experiment. (a) Thermal simulation results for the heat sink. (b) Measured curve of temperature rise.

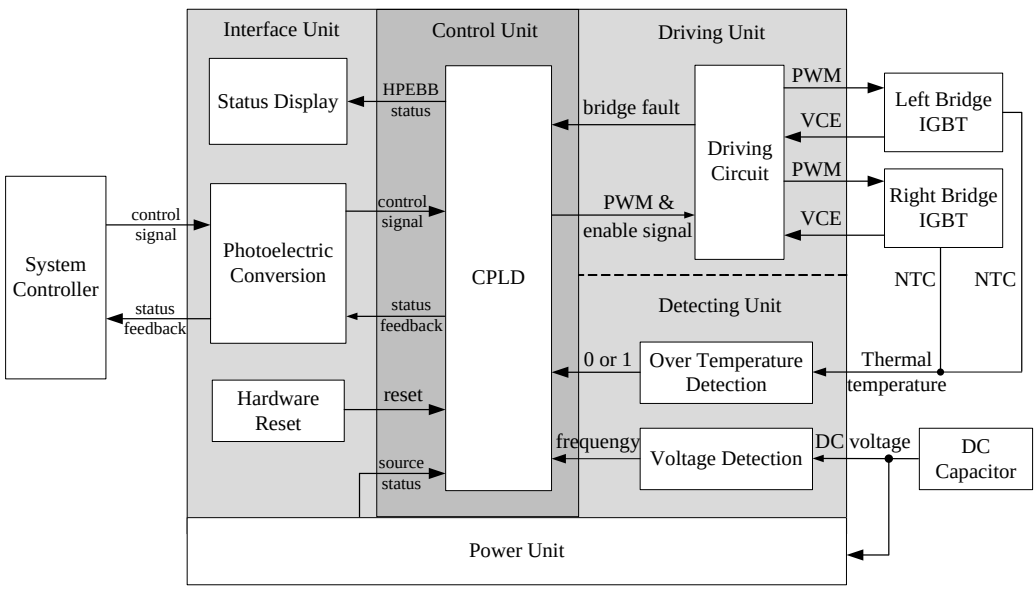



Fig. 5. Block diagram of the module controller.

## III. Controller Design

### *A. Principle of the Universal HPEBB Controller*

The block diagram of the CPLD-based universal HPEBB controller is displayed in Fig. 5. The controller consists of the following five units: interface, power supply, driving, detecting, and control. The controller receives control signals from the upper system controller of DSTATCOM and feeds back the HPEBB status simultaneously. An optical fiber is applied to transfer communication data reliably and accurately. Signals are photoelectrically converted by the interface unit. In addition, the status fed back from the control unit is reported using light-emitting diodes (LEDs). These signals can be eliminated by the reset circuit.

The driving unit is directly connected to the main circuit. The electromagnetic environment of the HPEBB in switching condition is harsh; thus, the SCALE-2 series-dedicated driver core of CONCEPT is adopted in the design of the driving unit to ensure the integrity and reliability of the driving signal. The driver core also generates the dead-time in the upper/lower legs, protects the IGBT from short circuit and over voltage by detecting the collector-emitter voltage (VCE) of the IGBTs, and monitors power failures. All driver-core operation statuses are transmitted to the control unit.

The detecting unit detects DC voltage and IGBT over-temperature. The detection principles are presented in Fig. 6. Specifically, the analog DC voltage $U_{dc}$ is digitized to a pulse signal given frequency information derived from the voltage-to-frequency converter circuit, as depicted in Fig. 6(a). Following electrical isolation, the signal is sent to the control unit. The inner negative temperature coefficient (NTC) of the IGBT thermal resistor is applied to judge the case temperature, as indicated in Fig. 6(b). NTC resistance decreases with the increase in module temperature, and sampling voltage $U_s$ rises as well. The comparator threshold $U_{ref}$ is set according to the maximum permitted operating temperature of the IGBT junction. Then, the over-temperature status can be assessed by comparator output. The output signal should be isolated as well.

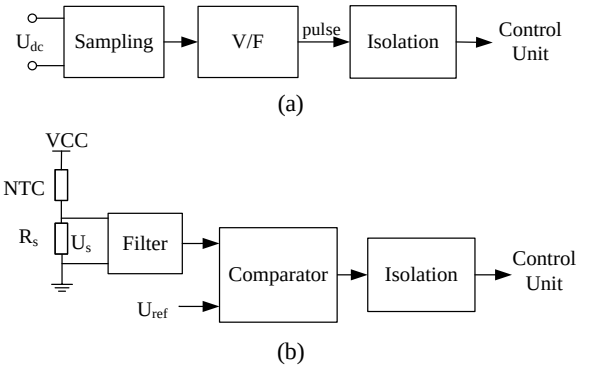



Fig. 6. Block diagram of the detecting unit. (a) DC voltage detector. (b) Over-temperature detection.

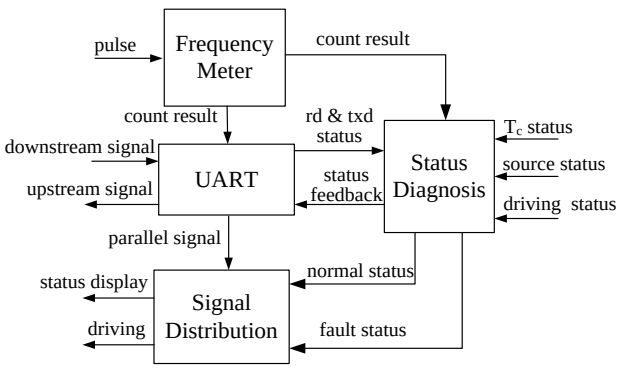



Fig. 7. Block diagram of control unit.

### *B. Development of CPLD Based Control Unit*

The control unit is the core of the HPEBB. Module flexibility, compatibility, anti-interference capability, and "plug and play" features are effectively improved by the corresponding design programs. These programs meet different application requirements. The block diagram of the control unit is exhibited in Fig. 7. The control unit includes four sub-modules: frequency meter, universal asynchronous receiver transmitter (UART), status diagnosis, and signal distribution.

Fig. 8 shows the principle of the frequency meter, which is used to measure the frequency of the input pulse signal acquired by the detection unit. The period of input signal is counted by standard clock pulses. Upon shaping and frequency dividing, the input signal is converted into a square waveform that is twice that of the original period. Two high/low-level counting and low/high-level clearing counters are adopted for counting in the half-period of the square waveform signal. The count results are stored in corresponding positive and negative edge triggered latches. Then, the latch output indicates the period of the input signal. A router is used to output the most recent updated data. Thus, accuracy of frequency measurement can be ensured in real-time. The count value is uploaded to the system controller. The period of input signals can be calculated using $f_{dc} = f_s/n$, where $f_{dc}$ is the frequency of the input signal, $f_s$ is the frequency of the standard clock, and $n$ is the count value.

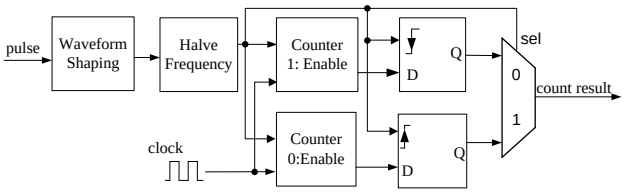



Fig. 8. Principle of the frequency meter.

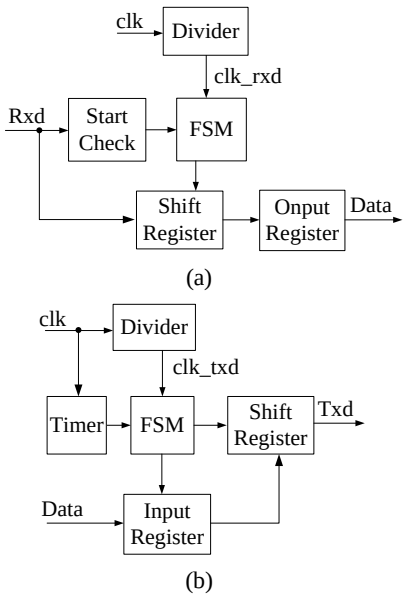



Fig. 9. Principle of UART. (a) Receiver. (b) Transmitter.

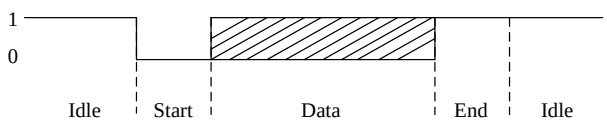



Fig. 10. Data format of UART.

UART is used in the communication between the system and the module controller. The principle of the module, which contains a receiver and a transmitter, is illustrated in Fig. 9. The working sequence is controlled by the finite state machine (FSM). Fig. 10 presents the data format of UART. Each data frame includes one low-level start bit, one high-level end bit, and several data bits. During idle time, the bus level is set to high. Fig. 11 displays the experimental results for the communication data. The top waveform of the figure denotes the overall process of communication. The bottom waveform represents the details of frame data. Five bits are generated for each frame of downstream data, whereas 18 bits are produced for each frame of upstream data. Each bit lasts for 400 ns. Then, a minimum of 2 μs is required for downstream data communication, whereas at least 7.2 μs is needed for upstream data communication. The communication frame rates are set to 4 and 20 μs per frame for downstream and upstream data, respectively, to facilitate reliable communication and extension in future updates. These rates are high enough to control and protect the HPEBB. The transmission rates of upstream and

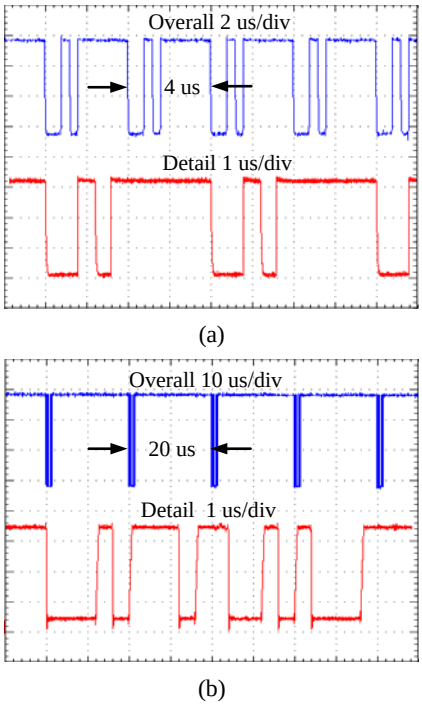



Fig. 11. Waveforms of data sending and receiving. (a) Downstream data. (b) Upstream data.

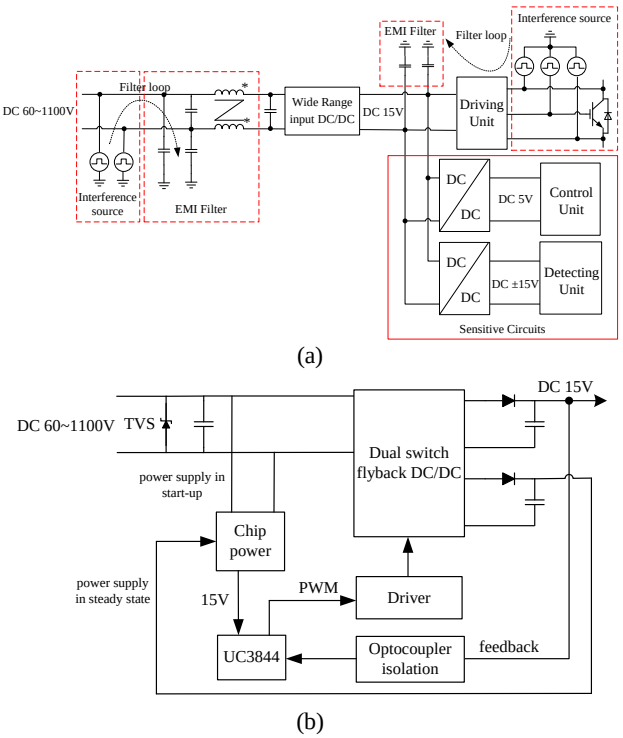



Fig. 12. Schematic of the power unit. (a) Block diagram of power supply. (b) Block diagram of the wide-range input DC/DC power module.

downstream data may differ due to use of two independent optical fiber for full duplex communication. Downstream data represent the control instruction, including two bits for PWM enable, two bits of PWM for each arm, and one bit for software reset. Meanwhile, the upstream data include 13 bits for count value and 5 bits for the HPEBB status flags. These bits are distinguished by the status diagnosis module. The statuses include over-temperature, IGBT right/left-arm-fault, and DC-side under/over-voltage. First, these signals are decoded by UART. Then, they are distributed by the signal distribution module.

### *C. Reliability and Anti-Interference Design*

*1) Electromagnetic Interference (EMI)-Caused Disturbance and Solution:* The power unit is a source of power for other units. Fig. 12 shows the block diagram of this unit. The input of the power unit is derived from the DC capacitor. The dual-switch, flyback-based wide range DC/DC power module depicted in Fig. 12(b) is developed to fit operations when DC voltage varies from 60 V to 1100 V. The quality of the power supply directly affects the stability and performance of the module controller. Thus, two additional power management chips with high reliability and regulated output are used to supply power to the control and detecting units. The design of the unit should fully consider power capacity, load effect, isolation, and EMI The interference source and sensitive circuits are highlighted in the box composed of dashed lines. External power and IGBT switching may induce severe interference that affects the normal operations of the control and detecting units. The EMI filter can reduce the interference to sensitive circuits by generating a low impendence path to the noise signal. Fig. 13 depicts a sample typical filter effect. Disturbance is caused by the surge current when the AC load of the HPEBB changes. The disturbance is coupled with the low-voltage side through the leakage inductance of the isolation transformer of the driver, thereby affecting the fault feedback signal of the IGBT. The generated waveforms suggest that the signal contains many high-frequency components in the absence of an EMI filter. This scenario may result in erroneous judgments regarding HPEBB status. These high-frequency components are eliminated by EMI filters. This removal assists in improving the anti-interference capability of HPEBB. The error in HPEBB judgment is thus eliminated in the actual experimental test.

*2) Transient Process-Caused Interference and Solution:* The control and feedback signals of HPEBB may be subject to interference due to the nonlinearity of semiconductor devices, transmission delay, and the matching of timing in transient processes, such as power up/off, power supply interruption, and other fault conditions. This interference may induce module failure and error protection. Given the flexibility of CPLD, the reliability and anti-interference capability of HPEBB can be improved significantly by developing corresponding digital filters on CPLD to address control and feedback signals on the basis of different interference characteristics. This process effectively cancels out noise signals without changing the hardware circuit.

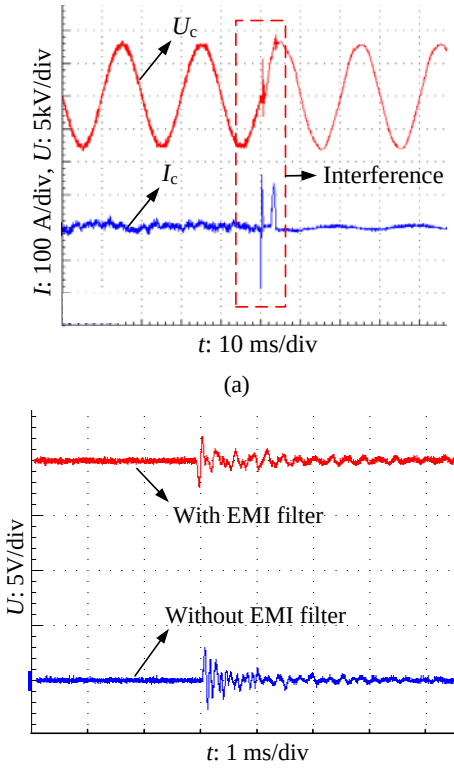



Fig. 13. Effect of the filter on the interference caused by surge currents. (a) Interference caused by surge currents. (b) IGBT fault feedback.

Fig. 14 presents the principle and filter effect when the digital filter eliminates the interference caused by the nonlinearity of optical components. If the power supply of the system controller is interrupted, then the output of driver IC (DS75451) is open circuit. The voltage of the fiber-optic transmitter $U_D$ first rises increases to its conduction voltage; then, $U_D$ decreases with $VCC_1$. When $U_D$ drops to the nonlinearity conduction boundary of internal LED, the diode flashes and initiates oscillation in the downstream communication signals of HPEBB. The oscillation is decoded by UART to high-frequency PWM and PWM-enable (PWMen) pulses. The pulses may induce the false action of IGBTs. When the frequency exceeds the allowable level, the controller is subject to overload protection. What's more, the drivers and IGBTs may even be damaged as well. A low frequency D-trigger-based delay comparison filter is applied to the PWMen signal. The clock frequency and delay time of the filter are determined according to the duration of the transient process to ensure that the PWMen signal remains within the inactive voltage level and that the PWM signal is blocked during oscillation. The generated waveforms indicate that the false PWMen pulses are cancelled out by the designed digital filter.

Similarly, Fig. 15 depicts the principle and filter effect of the interference caused at start-up transition. An RC hardware power-on reset circuit is employed to initialize the status of

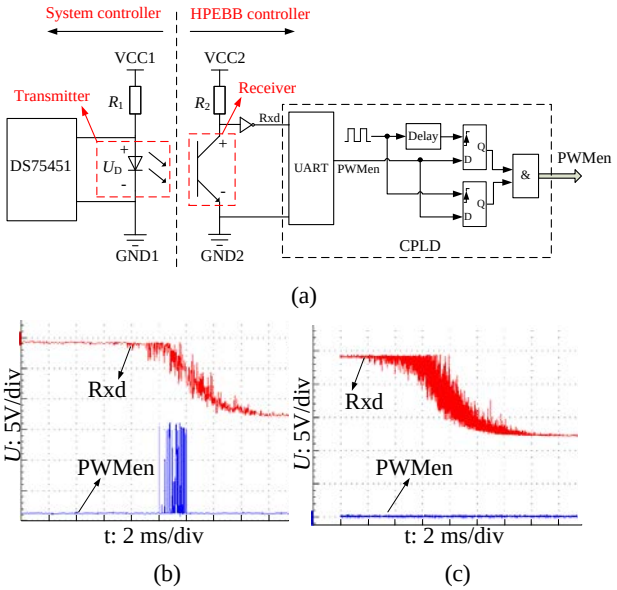



Fig. 14. Principle and solution for the interference caused by power supply interruptions. (a) Principle and solution for the interference. (b) Waveforms without digital filter. (c) Waveforms with digital filter.

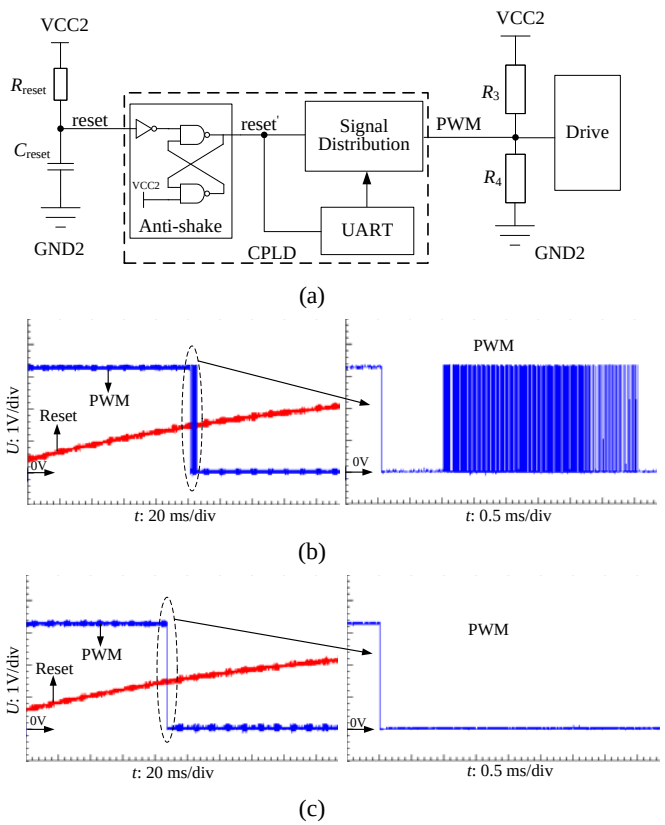
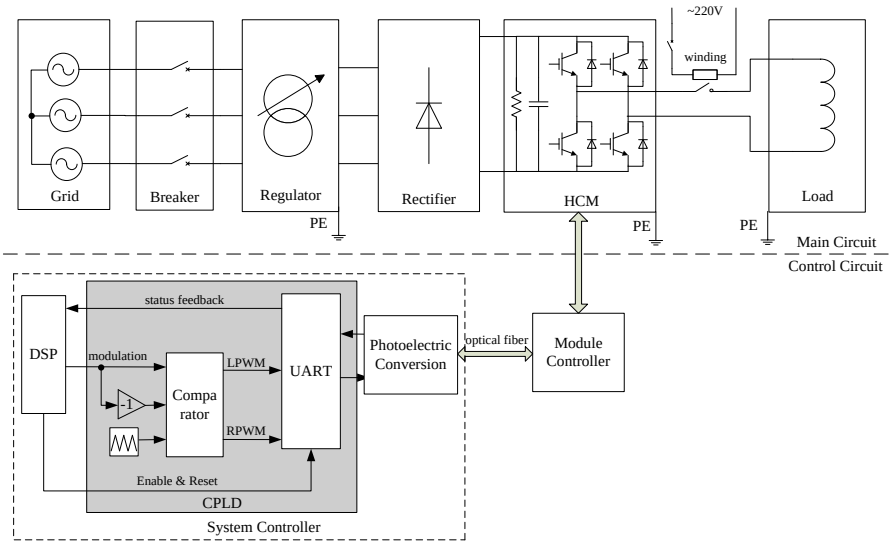
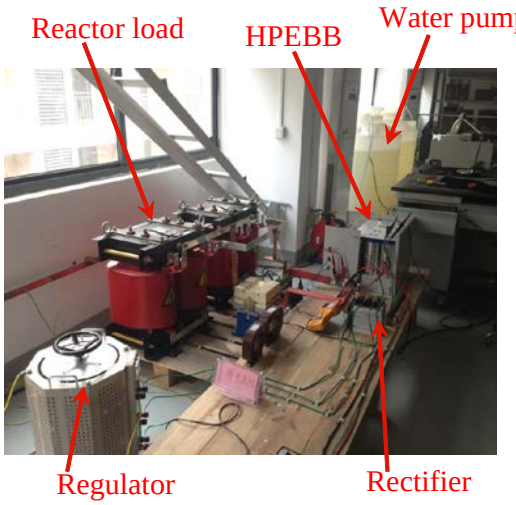



Fig. 15. Principle and solution for the interference caused during start-up. (a) Principle and solution for the interference. (b) Waveforms without digital filter. (c) Waveforms with digital filter.

each sub-module. The voltage level of the reset pin (reset) rises according to the time constant determined by $R_{reset}$ and $C_{reset}$. The internal reset signal (reset') is low when the pin voltage is lower than the input low voltage (VIL) of CPLD. Then, all




(a)




(b)

Fig. 16. HPEBB test bed. (a) Schematic. (b) Image of the test bed.

sub-modules are reset. The internal reset signal is high when the pin voltage rises above the input high voltage (VIH) of CPLD. Then, module controller operation is initiated. However, the internal reset signal is uncertain and oscillates if the pin voltage is between VIL and VIH. In this case, the UART and the signal distribution sub-modules may generate high-frequency false PWM pulses, as shown in Fig. 15(b). These pulses induce overload protection in the controller and even damage the drivers and IGBTs, as in the previous analysis. Thus, a bistable anti-shake circuit is developed on CPLD to prevent the oscillation of reset', which is illustrated in Fig. 15(a). The experimental waveforms in Fig. 15(c) indicate that the error pulses are completely eliminated at start-up transition.

## IV. HPEBB Test and Application

### *A. HPEBB Test Bed and Experimental Test*

An experimental test bed is established to verify HPEBB functionality and performance. Experiments are conducted to test the key control signals and operation performance. The schematic of the experimental platform is displayed in Fig. 16. This platform includes the main and control circuits. The electrical parameters of HPEBB are similar to those of the module design presented in part II. HPEBB operates in the passive inverter state with respect to the inductive load. DC voltage is generated and controlled by the regulator circuit. As reactive power is exchanged between the load and HPEBB, a small amount of energy must be supplied by the grid to compensate for the loss of HPEBB and line.

The controller circuit includes the system and HPEBB controllers designed in this study. The system controller mainly consists of a digital signal processor (DSP), CPLD, and photoelectric conversion circuit. Unipolar double frequency sinusoidal PWM is applied to improve the equivalent switching frequency of HPEBB. Modulation signals are provided by the DSP with a given modulation index. The PWM signals of the

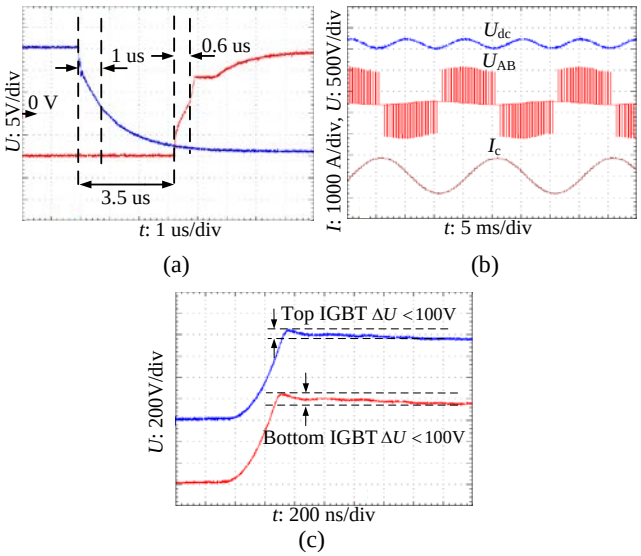



Fig. 17. Waveforms obtained during the HPEBB test. (a) IGBT gate signals. (b) Test main circuit waveforms under rated condition. (c) Voltage overshoot of $V_{ce}$ under rated condition.

two arms are produced by comparing the modulation signals with a pair of inverted triangular carriers. The fundamental frequency and the root mean square of the module output are determined by the frequency and the modulation index of the modulation signals. When the fault status of HPEBB is detected, the DSP immediately sets the enable signal to invalid level to protect the module.

A pair of gate signals related to an arm is displayed in Fig. 17(a). The switching frequency of IGBT is 1 kHz. The turn-on delay is 0.6 μs, whereas the turn-off delay is 1 μs. The effective dead-time is 3.5 μs. To reduce the influence of high-frequency noise and to ensure reliable shutdown, the gate voltage is restricted to -10 V when the IGBT is turned off. Stabilize the DC voltage at rated 800 V by regulator and control the index of modulation signal to make the HPEBB output rated current of 600 A with a fundamental frequency of 50 Hz. Fig. 17(b) depicts the experimental waveforms under full load operation. DC voltage exhibits a ±100 V and 100 Hz ripple when HPEBB operates at full load. Fluctuations are reflected on the AC side. IGBT voltage should be controlled strictly within the limits provided in the datasheet; therefore, the voltage overshoot of $V_{ce}$ when the device is turned off [Fig. 17(c)] should be controlled within these limits as well. Voltage overshoot is suppressed to within 100 V when the laminated bus-bar and snubber capacitor are applied. Furthermore, maximum IGBT voltage is less than 1000 V; this value meets the security requirements.

### *B. HPEBB Application in an Industrial Prototype*

The designed HPEBB is applied to a three-phase industrial prototype of DSTATCOM to verify its adaptability and universality further. The rated voltage and capacity of the prototype is 10 kV/10 Mvar. Twelve HPEBBs are connected in series for each phase. Fig. 18 presents the experimental schematic of the prototype. The 10 kV feeder is produced by a regular transformer. Given the limitation on feeder capacity, capacitive load is used to support the bus. The experiment on maximum dynamic cannot exceed the bus capacity for safety. First, the prototype operates at current tracking mode. Figs. 19(a) and 19(b) indicate the results for static and dynamic reactive power compensation, respectively. Fig. 19(c) shows the harmonic compensation results, and the generated waveforms include the load and grid currents. Then, the prototype operates at voltage stabilizing mode. Fig. 19(d) depicts the dynamic waveforms when the feeder voltage of 10

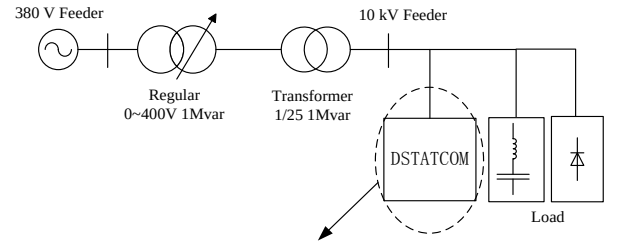



Fig. 18. Experimental schematic of the prototype.

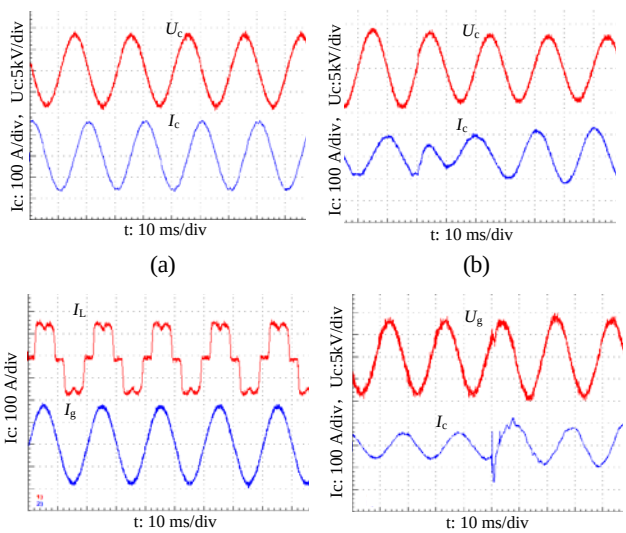



Fig. 19. Experimental results for the prototype. (a) 2-Mvar capacitive compensation. (b) 1.5-Mvar capacitive-to-inductive compensation. (c) Harmonics compensation. (d) Feeder voltage stabilization.

kV is fluctuation. All of the experimental results suggest that the performance and reliability of the designed HPEBB are satisfactory.

## V. CONCLUSION

This study designed a main circuit and controller for an H-bridge-based, "plug and play" type HPEBB. This HPEBB is applied to the cascaded DSTATCOM by integrating power conversion, driving, control, sampling, and protection, among others. Electrical parameter structure and thermal dissipation design are discussed in detail in the section that focuses on the main circuit. The section that emphasizes the controller introduces the design of the CPLD based universal module controller. With respect to the reliability and anti-interference capability of HPEBB, traditional EMI issues and interference caused by the transient module controller process are analyzed as per the corresponding proposed solutions. All module design aspects are verified by test experiments conducted on an HPEBB test bed. HPEBB is applied to a 10 kV/10 Mvar DSTATCOM industrial prototype for reactive power compensation, voltage support, and harmonic compensation experiments. The experimental results prove the reliability and adaptability of the designed module.

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