JPE 15-3-19

http://dx.doi.org/10.6113/JPE.2015.15.3.763
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Analysis and Design of DC-link Voltage Controller in Shunt Active Power Filter

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Abstract

This study investigates the inherent influence of a DC-link voltage controller on both DC-link voltage control and the compensation performance of a three-phase, four-wire shunt active power filter (APF). A nonlinear variable-parameter DC-link voltage controller is proposed to satisfy both the dynamic characteristic of DC-link voltage control and steady-state compensation performance. Unlike in the conventional fixed-parameter controller, the parameters in the proposed controller vary according to the difference between the actual and the reference DC-link voltages. The design procedures for the nonlinear voltage controller with variable parameters are determined and analyzed so that the proposed voltage controller can be designed accordingly. Representative simulation and experimental results for the three-phase, four-wire, center-spilt shunt APF verify the analysis findings, as well as the feasibility and effectiveness of the proposed DC-link voltage controller.

Key words: Active power filter, Compensation performance, Dynamic characteristic, Nonlinear variable-parameter controller

I. INTRODUCTION

Power electronic devices have been widely utilized with the rapid development of power electronics technology. Therefore, much harmonic current is injected into grids, thus deteriorating power quality and severely damaging the power system further [1]. As a result, harmonic control is a hot issue and has been studied extensively [2]. Active power filters (APFs) can detect and compensate system harmonics and reactive power in real time, thereby reducing the harmonic effect on the grid and ensuring operations [3]. APF exhibits a dynamic response, real-time characteristic, and controllability that are superior to those of the passive filter. Thus, APF is an ideal device with which to compensate harmonics and improve power quality [4].

DC-link voltage must be sufficiently constant in value so that APF can function properly. This process ensures that the compensating current produced by APF strictly follows the control requirement and generates the desired compensation effect [5]. Therefore, the design of DC-link voltage controllers is important; it requires detailed quantitative analysis and specification. Studies have been conducted on the APF control algorithm and on DC-link voltage control strategy [6]-[11]. Nonetheless, few studies investigate APF DC-link voltage control specifically. Existing literature mainly focuses on DC-link capacitor minimization [12], [13], DC-link voltage control strategy [14], [15], minimum DC-link voltage design [16]-[18], and adaptive strategies for DC-link voltage reference value [19]-[22]. Such studies seldom emphasize the inherent relationship between DC-link voltage controllers and the steady-state compensation performance of APF. Furthermore, the design procedures for the DC-link voltage controller are not considered and analyzed, including dynamic and steady-state performance. Given the limitations in literature, the current study investigates the inherent influence of the DC-link voltage controller not only on DC-link voltage control but also on the steady-state compensation performance of APF. The design procedures for the DC-link voltage controller are discussed as well.

A nonlinear, proportional—integral (PI) DC-link voltage controller with variable parameters is proposed to overcome the shortcoming of the conventional fixed-parameter PI DC-link voltage controller. The proposed controller satisfies both the dynamic characteristic of DC-link voltage control and the steady-state compensation performance of APF. DC-link voltage is determined by the P/PI voltage controller in the majority of previous studies. The PI controller is generally

Manuscript received Nov. 12, 2014; accepted Feb. 24, 2015
Recommended for publication by Associate Editor Jun-Keun Ji.
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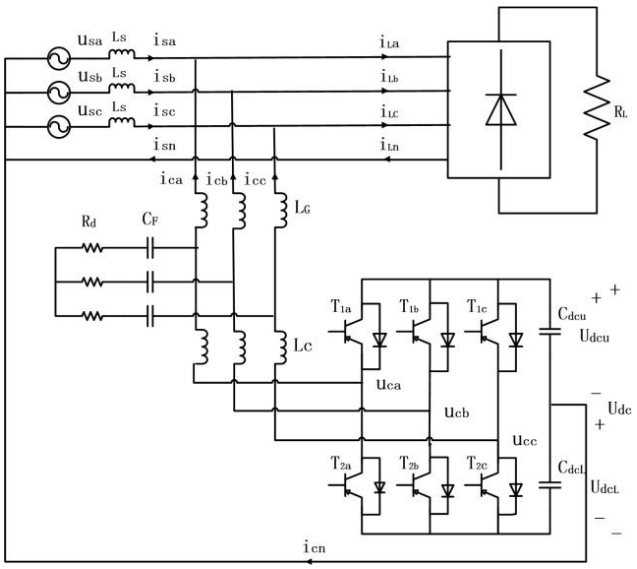


Fig. 1. Circuit of the three-phase, four-wire, center-split shunt APF.

applied [6]-[17], and the controller parameters are fixed. P/PI DC-link voltage control is thus improved. A fast-acting DC-link voltage controller that is based on the energy of the DC-link capacitor was proposed in [23]. Overshoot and settling time are reduced for DC-link voltage when the load changes suddenly. A new strategy was presented in [24] to control the square of the DC-link voltage, rather than the DC-link voltage itself. DC-link voltage command was fast-tracked with zero steady-state error. Appropriate parameters were determined through mathematical derivation and design experience for the proposed controllers that can reduce settling time and can avoid overshoot and saturation in line currents. The precision and reliability of the controller parameters were uncertain due to modeling error and to the uncertain and varied system parameters. Moreover, the proposed controllers were still fixed-parameter PI controllers; thus, their values could not be adjusted adaptively according to varying system parameters and control requirements in different control stages.

In the current study, a nonlinear PI controller is proposed and applied to the APF DC-link voltage controller to overcome the shortcoming of conventional fixed-parameter DC-link voltage control. The parameters of the PI controller vary according to the difference between the actual and the reference DC-link voltages. Unlike in the conventional fixed-parameter PI controller, the parameters in the proposed controller are adjusted adaptively on the basis of the difference between the actual and the reference DC-link voltages. The control requirements in different control stages are adopted to satisfy both the dynamic characteristic of DC-link voltage control and the steady-state compensation performance of APF. These requirements include start-up, load fluctuation, and APF steady-state operation period.

The rest of the paper is organized as follows: a three-phase, four-wire, center-split shunt APF is illustrated in Section II. The influence of the DC-link voltage controller on DC-link voltage control and APF compensation performance is analyzed in Section III through control strategy analysis and mathematical deduction. The design procedures for the DC-link voltage controller are considered and analyzed as well in this section. A nonlinear DC-link voltage controller with variable parameters is described in Section IV to overcome the shortcoming of the conventional fixed-parameter DC-link voltage controller and to satisfy the dynamic characteristic of DC-link voltage control and steady-state compensation performance. The simulation and experimental verifications of the analysis of DC-link voltage control, as well as of the proposed voltage controller, are presented in Sections V and VI, respectively. Finally, the conclusions are provided in Section VII.

II. Three-Phase Four-Wire Center-Split Shunt APF

The circuit of the three-phase, four-wire, center-split shunt APF is shown in Fig. 1. U_{sx} is the grid voltage, and U_{cx} is the inverter voltage. i_{sx}, i_{lx}, and i_{cx} are the grid, load, and compensating currents for each phase, respectively. Subscript x denotes phases a, b, c, and n. C_{dc} and U_{dc} denote the DC-link capacitor and the DC-link voltages, respectively. The upper and lower DC-link capacitor voltages are $U_{dcU} = U_{dcL} = 0.5 U_{dc}$. L_s is the grid inductor and is normally neglected due to its low value. The nonlinear load is composed of a three-phase, full-bridge rectifier and a resistance R_L that acts as a harmonic-producing load. The LCL filter that consists of L_C, L_G, and C_F is used to filter out the harmonics at switching frequencies. R_d is used to suppress the resonance peak of this filter at resonance frequency and to maintain system stability. Given that the LCL filter behaves as an inductor at the frequency range below 2.5 kHz and that the common requirement of the APF output current involves the 50th harmonic, only the frequency range below 2.5 kHz should be considered in control system design. As a result, the LCL filter can be reasonably simplified as an inductor in a low-frequency range. The inductance value of this inductor is determined by $L = L_C + L_G$. R is the equivalent resistance of the inductor [25].

III. Analysis of DC-link Voltage Control

With the aid of the harmonic detection algorithm based on instantaneous reactive power theory, DC-link voltage can be effectively controlled by feedback from the DC-link-voltage-regulated signal as a positive, fundamental, active current component of this algorithm. The difference between the reference and the actual DC-link voltages is regulated by the voltage controller, and the post-regulation signal is added to the aforementioned current component.

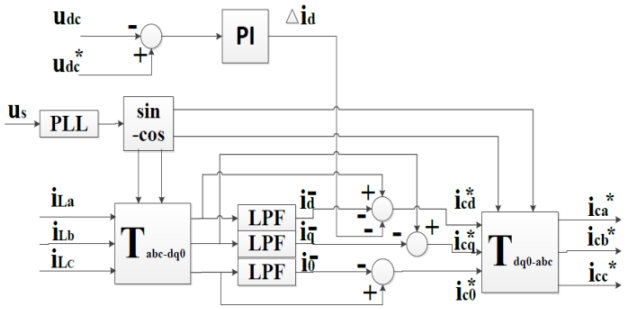


Fig. 2. Harmonic detection module with DC-link voltage control.

Therefore, the reference currents contain the fundamental, active current component that ensures energy exchange between the DC and AC links of APF and maintains DC-link voltage at a reference level. The id–iq harmonic detection method based on instantaneous reactive power theory is typically applied to detect load harmonics accurately. The harmonic detection module with DC-link voltage control is presented in Fig. 2, where $T_{abc\text{-}dq0}$ is the transformation matrix from the abc coordinate to the dq0 coordinate; $T_{dq0\text{-}abc}$ is the transformation matrix from the dq0 coordinate to the abc coordinate; U_{dc} is the actual DC-link voltage; U_{dc}* is the reference DC-link voltage; and ΔI_d is the signal regulated by DC-link voltage. i_{La}, i_{Lb}, and i_{Lc} are load currents. i_{ca}*, i_{cb}*, i_{cc}* and i_{cd}*, i_{cq}*, i_{c0}* are reference compensation currents in the abc and dq0 coordinates, respectively.

A. Influence of DC-link Voltage Controllers on DC-Link Voltage Control

In the majority of existing studies, DC-link voltage is effectively controlled by the P/PI voltage controller. The PI controller is generally used [6]-[17] to feed back the controlled signal as an active current component or a reactive current component, thus maintaining DC-link voltage at a sufficient reference level.

The influence of the DC-link controller on DC-link voltage control is determined in conditions wherein the PI controller is applied. When K_i is fixed at K_i = 50, the effect of different K_p values on step response is shown in Fig. 3. When K_i is fixed, a large K_p value results in short rise and settling times, as well as a small overshoot. When K_p is fixed at K_p = 5, the effect of different K_i values on step response is depicted in Fig. 4. When K_p is fixed, a large K_i value yields a short rise time, but a large overshoot and a long settling time for DC-link voltage.

The effect of K_p on step response when the P controller is employed is displayed in Fig. 5. When K_p value varies from 5 to 25, a large K_p yields a short rise time for DC-link voltage. Overshoot does not occur when the P controller is used. However, this controller generates more steady-state errors than the PI controller does.

If the steady-state error in DC-link voltage is considered, then the PI controller is preferred. However, overshoot occurs when this controller is used. Moreover, the PI controller may

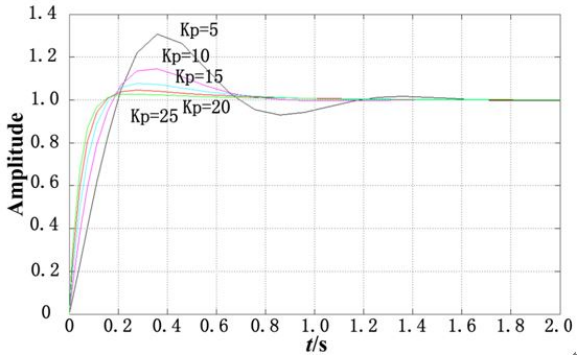


Fig. 3. Step response simulation for the PI controller when K_i = 50 and when K_p varies from 5 to 25.

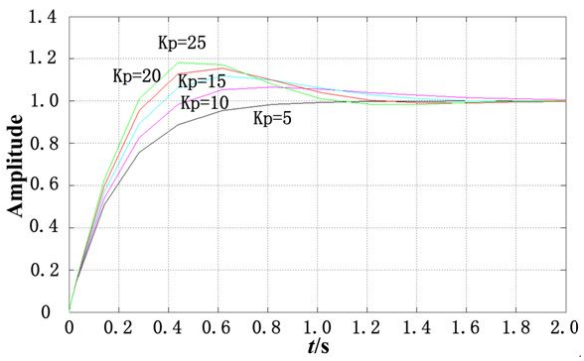


Fig. 4. Step response simulation for the PI controller when K_p = 5 and when K_i varies from 5 to 25.

protect APF from over-voltage and over-current situations. This process poses risks to devices such as insulated-gate bipolar transistors. Although overshoot can be suppressed by increasing K_p, this adjustment may enhance steady-state error. As a result, the voltage control loop exceeds the stability range. A large K_i value also yields a short rise time but a large overshoot for DC-link voltage. Furthermore, K_i appears to be a contradictory parameter for measuring performance. The analysis and design processes for control systems are more complex for the PI controller than for the P controller. The overshoot problem can also be solved by considering the critical damping of DC-link voltage control. When this critical damping is applied, the phase margin of the DC-link voltage control system is small and system stability worsens. Moreover, system parameters vary during operation. Thus, the critical damping of the DC-link voltage control cannot be set accurately. This scenario poses a risk to DC-link voltage control. Therefore, the P controller is preferable for the DC-link voltage controller in APF even though the P controller generates steady-state error. The P controller is advantageous because it does not induce overshoot in the process of increasing DC-link voltage. In the process, the system is protected. Moreover, this controller is simple and saves memory resources in the digital signal processor.

B. Influence of DC-Link Voltage Controllers on APF Steady-State Compensation Performance

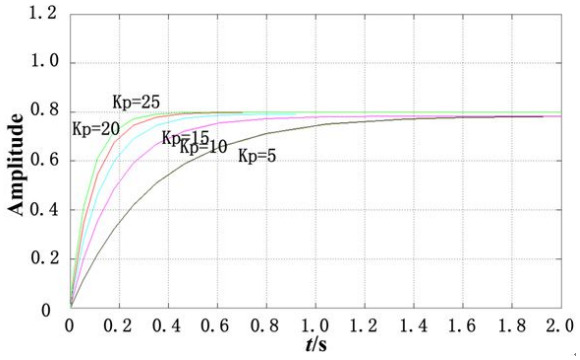


Fig. 5. Step response simulation for the P controller when K_p varies from 5 to 25.

APF can produce the compensation currents to adhere strictly to the reference currents that are equal to the load harmonic component. The harmonic component is compensated to avoid harmonic pollution in the power grid. APF compensation performance is mainly determined by two factors: whether or not the reference currents are equal to the load harmonic currents and whether or not the compensation currents track the reference currents effectively. Numerous studies verify that the harmonic detection module determines the accuracy of reference currents with respect to the load harmonic component. Furthermore, the performance of the compensation current controller determines the capability of compensation currents to follow the reference currents. The influence of DC-link voltage controllers on APF compensation performance is analyzed on this basis.

As per the harmonic detection algorithm for DC-link voltage control (presented in Fig. 2), the final reference currents i_{cd}*, i_{cq}*, and i_{c0}* in the dq0 coordinate are composed of two parts: the original reference current i_c* that is equal to the load harmonic component and the DC-link voltage control signal ΔI_d that is incorporated into the active current component of the reference current. Therefore, these final reference currents can be written as follows:

$$i^*_{c-final} = i^*_c + \Delta i_d$$

$$\begin{bmatrix} i^*_{cd} \\ i^*_{cq} \\ i^*_{c0} \end{bmatrix} = \begin{bmatrix} \sum_{n=0}^{\infty} I_{cdn}\cos n\omega t \\ \sum_{n=0}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=0}^{\infty} I_{c0n}\cos n\omega t \end{bmatrix} + \begin{bmatrix} -\sum_{n=0}^{\infty} \Delta I_d \cos n\omega t \\ 0 \\ 0 \end{bmatrix}. \quad (1)$$

$$= \begin{bmatrix} \sum_{n=0}^{\infty} [I_{cdn} - \Delta I_d]\cos n\omega t \\ \sum_{n=0}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=0}^{\infty} I_{c0n}\cos n\omega t \end{bmatrix}$$

According to Eq. (1), the final reference currents i_{ca}*, i_{cb}*, and i_{cc}* in the abc coordinate can be obtained as follows:

$$\begin{bmatrix} i^*_{fa} \\ i^*_{fb} \\ i^*_{fc} \end{bmatrix} = T_{dq0-abc} \begin{bmatrix} i^*_{fd} \\ i^*_{fq} \\ i^*_{f0} \end{bmatrix}, \quad (2)$$

where $T_{dq0\text{-}abc}$ is the matrix of transformation from the dq0 coordinate to the abc coordinate:

$$T_{dq0-abc} = \begin{bmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix}. \quad (3)$$

By integrating Eq. (1) into Eq. (2), the final reference currents in the abc coordinate can be written as follows:

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = T_{dq0-abc} \begin{bmatrix} \sum_{n=0}^{\infty} I_{cdn}\cos n\omega t \\ \sum_{n=0}^{\infty} I_{cqn}\cos n\omega t \\ \sum_{n=0}^{\infty} I_{c0n}\cos n\omega t \end{bmatrix} + T_{dq0-abc} \begin{bmatrix} -\sum_{n=0}^{\infty} \Delta I_d \cos n\omega t \\ 0 \\ 0 \end{bmatrix}. \quad (4)$$

As per Eqs. (1) and (4), the final reference currents in both the abc and dq0 coordinates are divided into two parts: the detected harmonic currents and the DC-link voltage control signal. Assuming that the harmonic detection module constructed with the id–iq method can detect the harmonic currents accurately, the first part of the final reference currents represents the specific harmonic currents that must be compensated. However, the other part of the final reference currents, that is, DC-link voltage control, may influence the accuracy of the final reference currents. Consequently, APF compensation performance is affected as well.

The DC-link voltage control signal in Eq. (4) can be expressed as follows:

$$\begin{bmatrix} \Delta i_{da} \\ \Delta i_{db} \\ \Delta i_{dc} \end{bmatrix} = T_{dq0-abc} \begin{bmatrix} -\sum_{n=0}^{\infty} \Delta I_d \cos n\omega t \\ 0 \\ 0 \end{bmatrix}$$

$$= \begin{bmatrix} \cos\omega t & -\sin\omega t & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & -\sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} -\sum_{n=0}^{\infty} \Delta I_d \cos n\omega t \\ 0 \\ 0 \end{bmatrix}. \quad (5)$$

$$= \begin{bmatrix} -\sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n-1) + \sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n+1) \\ -\sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n-1-\frac{2\pi}{3}) + \sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n+1-\frac{2\pi}{3}) \\ -\sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n-1+\frac{2\pi}{3}) + \sum_{n=0}^{\infty} \frac{\Delta I_d}{2}\cos(n+1+\frac{2\pi}{3}) \end{bmatrix}$$

According to Eq. (5), the n^{th} ($n > 0$, $n = 1,2,3,\ldots$) component of the DC-link voltage control signal ΔI_d in the dq0 coordinate reduces the $(n\text{-}1)^{th}$ component and increases the value of the $(n+1)^{th}$ component in the abc coordinate. This scenario is observed in all abc phases. As per Eqs. (1) and (5), the feedback DC-link control signal changes the values of the final reference currents and limits their accuracy in both the abc and dq0 coordinates.

Given that the P controller is preferred and is selected for DC-link voltage control in line with the previously described analysis results, the value of DC-link voltage control signal ΔI_d can be obtained as follows:

$$\Delta I_d = K_P \Delta U_{dc} = K_P (U_{dc}^* - U_{dc}) . \quad (6)$$

Given Eq. (6), ΔI_d increases as controller parameter K_p increases under a constant voltage difference ΔU_{dc} and vice versa. APF output compensation currents are controlled and adhere strictly to the final reference currents. A large K_p enhances the deviation of the value of the final reference currents from that of actual harmonic currents. Thus, the APF output compensation currents that follow the final reference currents deviate further from the actual harmonic currents and should be compensated. In this case, the steady-state compensation performance of APF deteriorates further.

IV. Proposed Nonlinear DC-Link Voltage Controller with Variable Parameters

A. Proposed Nonlinear PI Voltage Controller

According to the analysis results described above, the dynamic performance of DC-link voltage control is improved with the increase in the values of voltage controller parameters. However, this increase also deteriorates APF steady-state compensation performance and vice versa. Therefore, a nonlinear DC-link voltage controller is proposed to satisfy both the dynamic characteristic of DC-link voltage control and steady-state compensation performance. The parameter in the proposed controller is first set to a small fixed value (i.e., less than 0.1). Then, this parameter is multiplied by the absolute value of the voltage difference, which represents the real-time value of the controller parameter. The proposed law of nonlinear DC-link voltage control can be expressed as follows:

$$u(t) = K_P \mid \Delta U_{dc}(t) \mid \Delta U_{dc}(t) + K_I \mid \Delta U_{dc}(t) \mid \int_0^t \Delta U_{dc}(t) dt . \quad (7)$$

Thus, controller parameter values vary according to the difference between the actual and the reference DC-link voltages in real time. Specifically, the parameter values in the proposed controller increase when the actual and the reference DC-link voltages differ significantly, such as in the start-up stage and in the load fluctuation period. This scenario ensures the satisfaction of the dynamic characteristic in DC-link voltage control. By contrast, the parameter values in the proposed controller decrease when the difference between the actual and the reference DC-link voltage is slight, such as in the APF steady operation period. This occurrence prevents the voltage control signal from affecting the accuracy of harmonic detection and steady-state compensation performance.

The P controller is preferred and is selected for DC-link voltage control on the basis of the discussion in Section III regarding the characteristics of PI and P controllers in this voltage control. The law of nonlinear DC-link voltage control proposed in this paper is rewritten as follows:

$$u(t) = (K_P \mid \Delta U_{dc}(t) \mid) \bullet \Delta U_{dc}(t) . \quad (8)$$

B. Limitation of the Proposed Controller Parameter Value

The stability of the DC-link voltage control loop should be maintained to avoid the overflow problem. Thus, a limiter is applied to the controller parameter. According to the instantaneous energy balance principle highlighted in Fig. 1, the instantaneous power in the DC-link is equal to that in the AC-link. If the ripple effect is ignored, then the following instantaneous power balance equation can be obtained:

$$U_{dc}(t) I_{dc}(t) = u_{sa}(t) i_{ca}(t) + u_{sb}(t) i_{cb}(t) + u_{sc}(t) i_{cc}(t) - R[i_{ca}^2(t) + i_{cb}^2(t) + i_{cc}^2(t)] - \frac{L}{2} \frac{d}{dt} [i_{ca}^2(t) + i_{cb}^2(t) + i_{cc}^2(t)] , \quad (9)$$

where U_{dc}(t) is the instantaneous DC-link voltage; I_{dc}(t) is the instantaneous DC-link current; and i_{cx} is the compensation current. L is the inductance value of the simplified LCL filter in low-frequency range, and R is the equivalent resistance of the inductor, as discussed in Section II. The grid inductor L_s is normally neglected; hence, U_{sx} represents the voltage at the point where APF accesses the entire system. This voltage is equal to the grid voltage.

The influence of grid voltage fluctuation on DC-link voltage can be eliminated by applying the feed-forward control strategy proposed in [26]. Thus, the following derivations based on the balanced, three-phase grid voltage system simplify calculation and deduction to establish the DC-link voltage control loop. The equations below can be established according to instantaneous power theory [26]:

$$3U_S I_P(t) = u_{sa}(t) i_{ca}(t) + u_{sb}(t) i_{cb}(t) + u_{sc}(t) i_{cc}(t) , \quad (10)$$

$$I_{dc}(t) = C \frac{dU_{dc}(t)}{dt} , \quad (11)$$

where U_S is the effective value of the grid voltage; I_P(t) is the instantaneous value of the active compensation current; I_{dc}(t) is the instantaneous value of the DC-link current; and C is the capacitance value in the DC-link.

The compensation current i_c(t) is composed of fundamental current i_p(t) and harmonic compensate current i_h(t). i_p(t) maintains the DC-link voltage and i_h(t) compensates the load harmonics.

$$i_c(t) = i_p(t) + i_h(t) . \quad (12)$$

Then, the three-phase instantaneous power consumed by inductance and its equivalent resistance can be expressed as

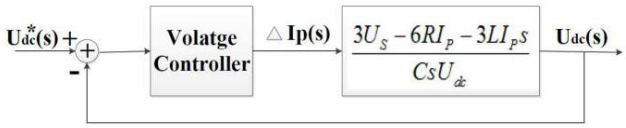


Fig. 6. Closed-loop block diagram for DC-link voltage control.

follows:

$$R[i_a^2(t)+i_b^2(t)+i_c^2(t)]=3R[I_p^2(t)+I_h^2(t)]\,. \quad (13)$$

$$\frac{L}{2}\frac{d}{dt}[i_a^2(t)+i_b^2(t)+i_c^2(t)]=\frac{3L}{2}\frac{d}{dt}[I_p^2(t)+I_h^2(t)]\,. \quad (14)$$

By integrating Eqs. (10), (11), (13), and (14) into Eq. (9), the following equations can be obtained:

$$3U_S I_P(t)=$$
$$3R[I_p^2(t)+I_h^2(t)]+\frac{3L}{2}\frac{d}{dt}[I_p^2(t)+I_h^2(t)]+CU_{dc}(t)\frac{dU_{dc}(t)}{dt}\,. \quad (15)$$

Changes in the fundamental current can cause fluctuations in DC-link voltage. Therefore, a transformation is initiated with a slight disturbance at the equilibrium point. Given a slight disturbance, the following can be obtained:

$$\begin{cases} U_{dc}(t)=U_{dc}^*+\Delta U_{dc} \\ I_P(t)=I_P+\Delta I_P \\ I_f(t)=I_f+\Delta I_f \end{cases}, \quad (16)$$

where U_{dc} is the reference value for DC-link voltage.

By integrating Eq. (16) into Eq. (15), the quadratic term is ignored and linearization is performed near the equilibrium point. The following equations can then be derived:

$$3U_S\Delta I_P(t)-6RI_P\Delta I_P(t)-3LI_P\frac{d\Delta I_P(t)}{dt}=CU_{dc}\frac{d\Delta U_{dc}(t)}{dt}\,. \quad (17)$$

$$\frac{d\Delta U_{dc}(t)}{dt}=\frac{d[U_{dc}(t)-U_{dc}^*]}{dt}=\frac{dU_{dc}(t)}{dt}\,. \quad (18)$$

When Eq. (18) is integrated into Eq. (17), the latter is transformed as follows:

$$3U_S\Delta I_P(t)-6RI_P\Delta I_P(t)-3LI_P\frac{d\Delta I_P(t)}{dt}=CU_{dc}\frac{dU_{dc}(t)}{dt}\,. \quad (19)$$

When Laplace transform is applied to Eq. (19), the transfer function of the DC-link voltage control loop can be derived:

$$G_{\mathrm{APF}}(s)=\frac{U_{dc}(s)}{\Delta I_P(s)}=\frac{3U_S-6RI_P-3LI_P s}{CsU_{dc}}\,. \quad (20)$$

Then, the control block diagram for DC-link voltage can be constructed as shown in Fig. 6. The closed-loop transfer function of DC-link voltage control can be obtained as follows by integrating the transfer function of the voltage controller into the loop:

$$G(s)==\frac{3K_PU_S-6K_PRI_P-3K_PLI_Ps}{(CU_{dc}^*-3K_PLI_P)s+(3K_PU_S-6K_PRI_P)}\,. \quad (21)$$

Given the closed-loop transfer function, the controller parameter value can be limited by applying the Routh criterion as follows:

TABLE I
SYSTEM PARAMETERS

Grid Voltage	U_{sn}	220 V
Grid Frequency	f	50 Hz
Switching Frequency	f_S	9.6 kHz
Inductor Filter	L	0.45 mH
Equivalent Resistance	R	0.2 ohm
DC-link Capacitance	C_{dcu} C_{dcL}	10000 uF
DC-link Voltage	U_{dc}^*	720 V

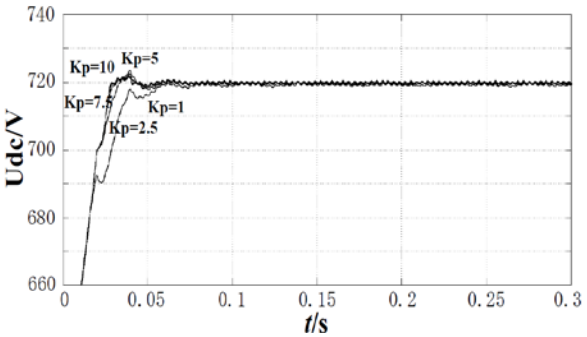
$$0<K_P<\frac{CU_{dc}^*}{3LI_P}\,. \quad (22)$$

V. SIMULATION AND EXPERIMENTAL VERIFICATION OF VOLTAGE CONTROLLER INFLUENCE

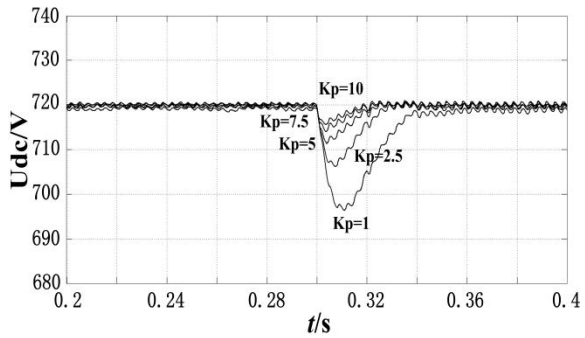
Simulations and experiments on the three-phase, four-wire shunt APF are conducted to verify the deduction and the proposed controller. The simulations are performed in MATLAB. To validate the simulation results, a prototype of this APF is also generated in laboratory. The parameters of the simulated and the experimental systems are listed in Table I. In addition, the P controller is used in DC-link voltage control, and the PI-repetitive compound control algorithm is utilized in compensation current control [27]. The influence of the DC-link voltage controller on DC-link voltage control and APF steady-state compensation performance is verified in this section.

Fig. 7 shows the simulation results in the start-up stage and during load change when voltage controller K_p varies from 1 to 2.5, 5, 7.5, and 10. The rise and resume times of DC-link voltage shorten with the increase in K_p. Similar results are also obtained in the experiments. The rise time for DC-link voltage in the start-up stage and the resume time in the load change period are shorter when K_p = 10 than when K_p = 1. The experiment results in the start-up stage and in load change are displayed in Figs. 8 and 9, respectively. A large K_p improves the dynamic characteristic in DC-link voltage control.

The influence of the DC-link voltage controller on steady-state compensation performance is determined. Without APF, the load currents contain numerous harmonics. The total harmonic distortion (THD) values of the simulated and the experimental load currents are 23.78% and 25.13%, respectively. Therefore, the currents are severely distorted. The value of each harmonic order current is listed in Table II. In general, even-ordered harmonics are largely offset in the three-phase system. Thus, these harmonics can be ignored in the calculation process. Given that the load harmonic currents beyond the 30th order are small, only the harmonic orders within the 30th are considered in this study for simplicity.

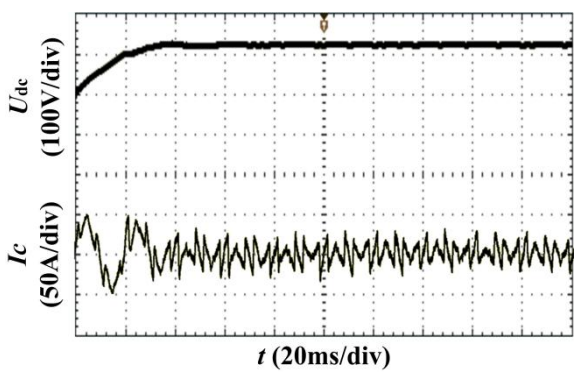


(a)



(b)

Fig. 7. Simulation results of DC-link voltage with different K_p values. (a) Start-up stage. (b) Load change.



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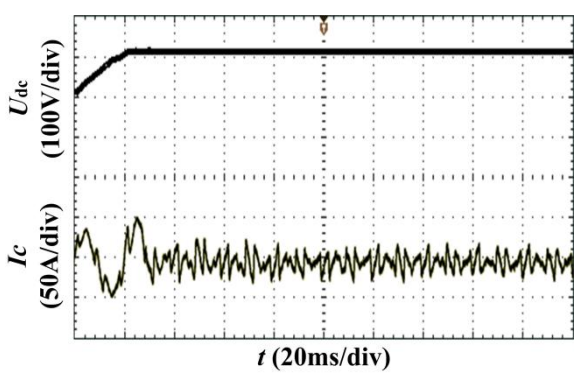

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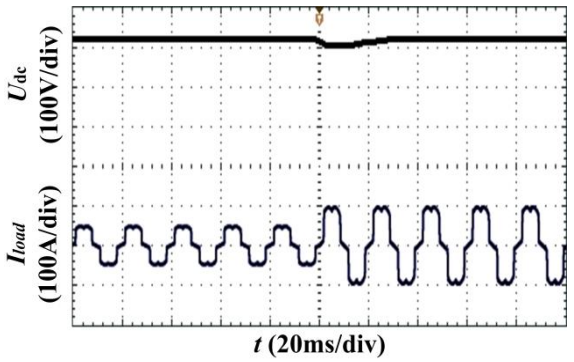
Fig. 8. Experimental results for DC-link voltage in the start-up stage with different K_p values. (a) K_p = 1, (b) K_p = 10.



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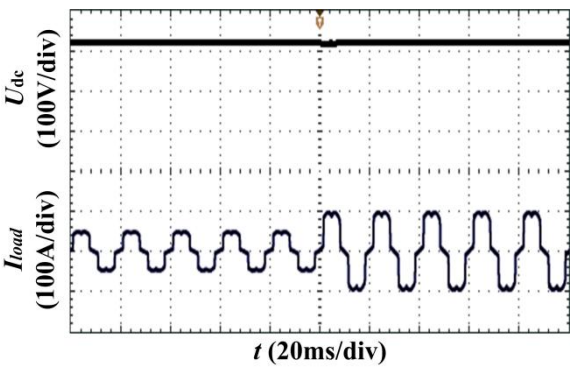


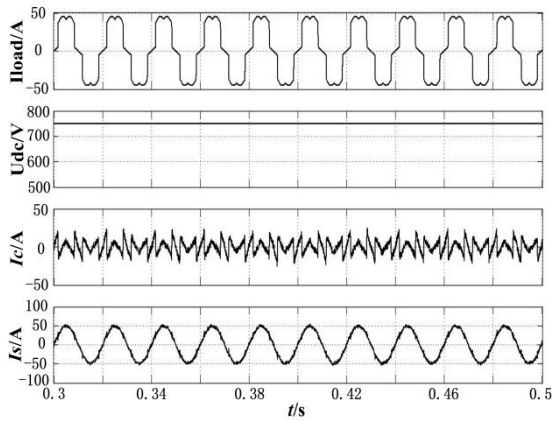
(b)

Fig. 9. Experimental results for DC-link voltage when load changes under different K_p values. (a) K_p = 1, (b) K_p = 10.

TABLE II
HARMONIC CURRENTS

Harmonic Order	Simulation	Experiment
5th	8.58 A	8.58 A
7th	4.28 A	4.29 A
11th	3.43 A	3.43 A
13th	2.43 A	2.43 A
17th	2.14 A	2.14 A
19th	1.70 A	1.71 A
23rd	1.55 A	1.35 A
25th	1.30 A	1.11 A
29th	1.21 A	1.02 A

When the value of the voltage controller parameter is K_p = 1, the simulated and the experimental THD values of the source current after compensation are 3.26% and 4.45%, respectively. The simulation and experiment waveforms are exhibited in Fig. 10. When K_p increases to 2.5, 5, 7.5, and 10, the simulated THD values of the source current after compensation increase to 3.48%, 3.80%, 4.26%, and 4.73%, respectively. The corresponding experimental values are 4.85%, 5.32%, 5.86%, and 6.22%. The diagram of variations in THD with K_p is shown in Fig. 11. When the current controller is set, the THD of the source current after compensation increases with K_p. Therefore, changes in K_p affect steady-state compensation performance.



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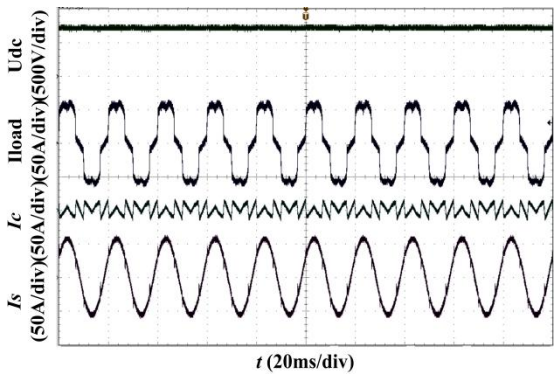


(b)

Fig. 10. Waveforms generated when K_p = 1. (a) Simulation. (b) Experiment.

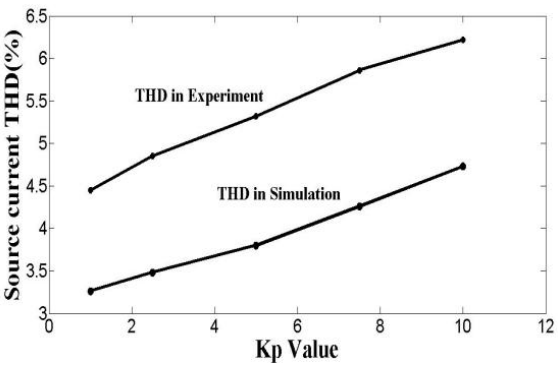


Fig. 11. THD values of the source current after compensation when K_p varies.

Assuming that the three phases of the APF are balanced using the id–iq harmonic detection algorithm, Table III lists the simulated value of each reference current order in the abc coordinate. The value in each reference current order is equal to the value in each load harmonic order when the DC-link voltage control signal is disregarded. The simulation results show that the harmonic detection algorithm is effective and that the reference current is the specific harmonic that should be compensated when the DC-link voltage control signal is disregarded.

TABLE III
SIMULATION REFERENCE CURRENTS IN THE ABC COORDINATES

Current Order	Simulation
1st	0.01 A
5th	8.58 A
7th	4.28 A
11th	3.43 A
13th	2.43 A
17th	2.14 A
19th	1.70 A
23rd	1.55 A
25th	1.30 A
29th	1.21 A

TABLE IV
REFERENCE CURRENTS IN DQ0 COORDINATES WITH VARIED VOLTAGE CONTROLLER PARAMETERS

	Orders	Kp = 1	Kp = 5	Kp = 10
I_d*	6th	4.58 A	4.59 A	4.58 A
	12th	1.02 A	1.01 A	1.01 A
	18th	0.45 A	0.44 A	0.44 A
	24th	0.25 A	0.24 A	0.24 A
	30th	0.16 A	0.15 A	0.16 A
I_d*+ΔI_d	6th	4.30 A	4.14 A	3.67 A
	12th	0.99 A	0.98 A	0.95 A
	18th	0.44 A	0.43 A	0.43 A
	24th	0.25 A	0.24 A	0.24 A
	30th	0.16 A	0.15 A	0.15 A

Tables IV and V list the values of each reference current order in the dq0 and abc coordinates with different voltage controller parameters once the DC-link voltage control signal is incorporated into the harmonic detection algorithm as the active component. Table IV shows that the values in the d-axis are mainly in the $6k^{th}$ order (k = 1,2,3,…) and that the i_d value varies after integrating the DC-link voltage control signal. The accuracy of the final reference currents in the dq0 coordinate is thus affected. Table V indicates that a fundamental current is used to maintain the DC-link voltage in the final reference current and that the values of each reference current order change. The $6k^{th}$ order values in the d-axis of the dq0 coordinate affect the values in the abc coordinate. Specifically, these $6k^{th}$ order values reduce the values of the $(6k-1)^{th}$ order and increase the values of $(6k+1)^{th}$ order in the abc coordinate. The magnitude of variation increases with the increase in K_p. In this case, the final reference current deviates from the accurate harmonic current, and the situation is aggravated with the increase in K_p.

As per the compensation current presented in Table VI, the APF output compensation currents effectively follow the final reference currents, regardless of the variation in K_p value.

TABLE V
FINAL REFERENCE CURRENTS IN ABC COORDINATES WITH VARIED VOLTAGE CONTROLLER PARAMETERS

Current Order	*Kp* = 1	*Kp* = 5	*Kp* = 10
1st	0.88 A	0.83 A	0.86 A
5th	8.57 A	8.41 A	8.01 A
7th	4.28 A	4.52 A	5.02 A
11th	3.43 A	3.41 A	3.37 A
13th	2.44 A	2.45 A	2.49 A
17th	2.14 A	2.14 A	2.17 A
19th	1.70 A	1.70 A	1.71 A
23rd	1.55 A	1.55 A	1.55 A
25th	1.30 A	1.30 A	1.30 A
29th	1.21 A	1.21 A	1.21 A

TABLE VI
COMPENSATION CURRENTS GIVEN A VOLTAGE CONTROLLER WITH VARYING PARAMETERS

Current Order	*Kp* = 1	*Kp* = 5	*Kp* = 10
1st	0.89 A	0.84 A	0.85 A
5th	8.52 A	8.33 A	7.95 A
7th	4.25 A	4.54 A	4.97 A
11th	3.41 A	3.35 A	3.39 A
13th	2.39 A	2.42 A	2.48 A
17th	2.21 A	2.16 A	2.15 A
19th	1.65 A	1.70 A	1.74 A
23rd	1.56 A	1.51 A	1.56 A
25th	1.30 A	1.28 A	1.29 A
29th	1.18 A	1.17 A	1.02 A

Hence, changes in controller parameter value does not affect current controller performance. Rather, these changes affect the accuracy of the final reference current with respect to the load harmonic. Thus, changes in controller parameter affect the steady-state compensation performance of APF.

Thus, the influence of the DC-link voltage controller can be confirmed as indicated by the aforementioned simulation and experiment results. A large K_p value improves the dynamic characteristic in DC-link voltage control. However, this large value also increases ΔI_d value, which was added to the harmonic detection algorithm as an active component. As a result, an additional value is incorporated into the final reference currents in both dq0 and abc coordinates. Therefore, the final reference currents deviate from the accurate harmonic currents and limit the precision of the final reference current. Although tracking capability remains excellent due to the set current controller, the steady-state compensation performance of APF may worsen with the increase in K_p.

VI. SIMULATION AND EXPERIMENTAL VERIFICATION OF THE PROPOSED DC-LINK VOLTAGE CONTROLLER

According to the aforementioned analysis and experiment results, an increase in K_p improves the dynamic performance of DC-link voltage control but deteriorates the steady-state compensation performance of APF. By contrast, a decrease in K_p value generates an excellent steady-state compensation performance but does not satisfy the dynamic characteristic of DC-link voltage control. A DC-link voltage controller with variable parameters is proposed to satisfy both the dynamic characteristic of DC-link voltage control and steady-state compensation performance. In the proposed controller, the P parameter varies according to the difference between the actual and the reference DC-link voltages.

Parameter value increases with the voltage difference once the DC-link voltage controller with variable parameters is applied and when the discrepancy between the actual and the reference DC-link voltages is large in the start-up stage. Moreover, the rise time of the DC-link voltage is shorter than that of the conventional fixed-parameter voltage controller with small parameters. Figs. 12 and 13 depict the simulation and experiment results for the process of DC-link voltage increase to the preset reference value given the conventional fixed PI controller and the proposed controller, respectively.

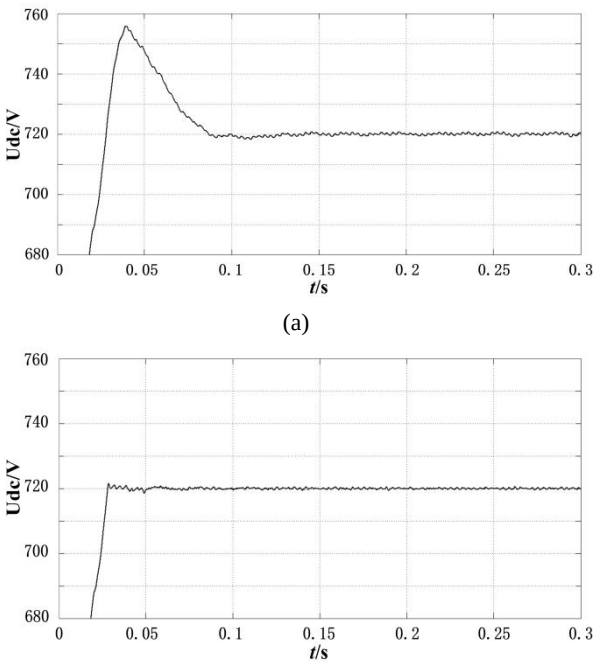
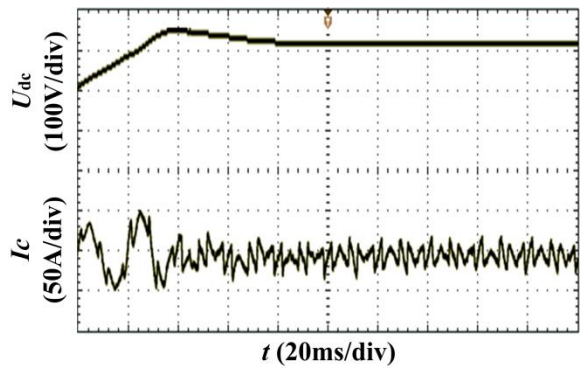


Fig. 12. Simulation results for the process of DC-link voltage increase. (a) With the conventional fixed PI controller. (b) With the proposed voltage controller.

Parameter value also increases with the difference in voltages when the load changes suddenly. Furthermore, the resume time of the DC-link voltage is shorter than that of the conventional fixed-parameter voltage controller with small parameters. Figs. 14 and 15 show the simulation and



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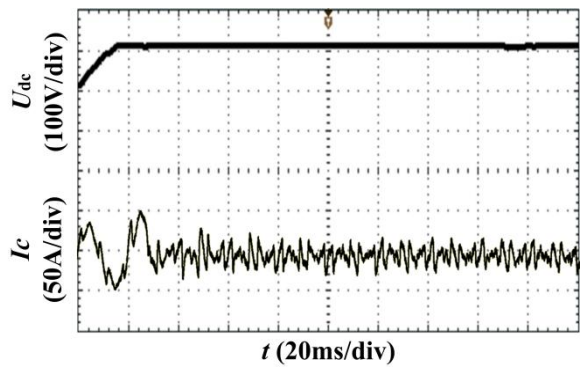

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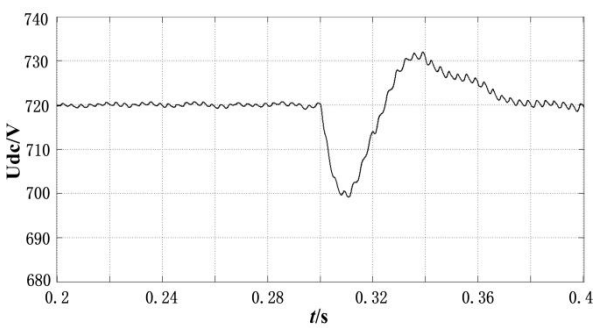
Fig. 13. Experimental results for the process of DC-link voltage increase. (a) With the conventional fixed PI controller. (b) With the proposed voltage controller.



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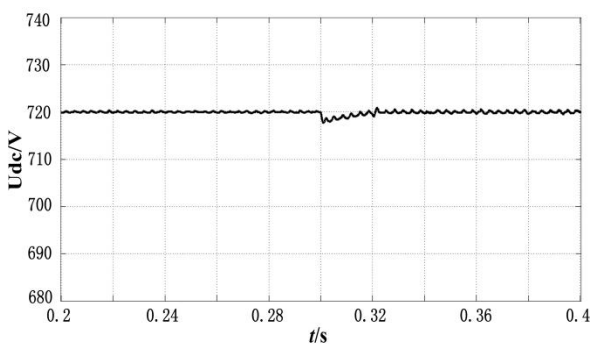
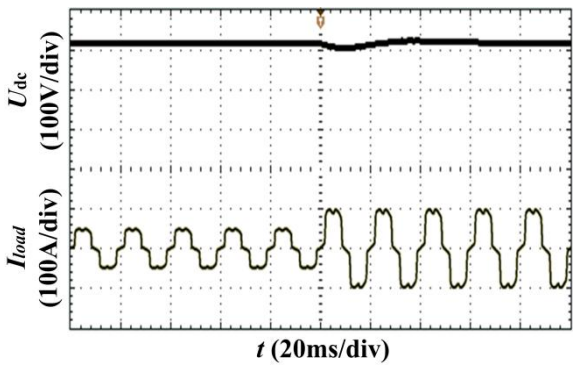
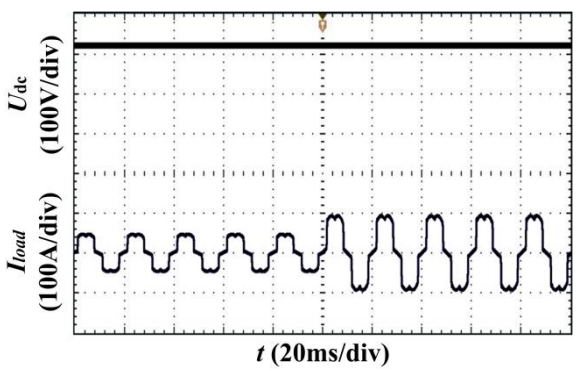


(b)

Fig. 14. Simulation results for the process of resuming DC-link voltage. (a) With the conventional fixed PI controller. (b) With the proposed voltage controller.



(a)



(b)

Fig. 15. Experimental results for the process of resuming DC-link voltage. (a) With the conventional fixed PI controller. (b) With the proposed voltage controller.

experimental results for the process of resuming DC-link voltage with the conventional fixed PI controller and the proposed controller when load changes. The voltage controller with variable parameters improves the dynamic characteristic in DC-link voltage control.

When the actual DC-link voltage differs only slightly from the reference DC-link voltage in the steady running stage, parameter value is small. Given the load change situation presented in Figs. 14(b) and 15(b), the simulated THD values of the source current are 3.44% and 3.33% before and after load change, respectively. The corresponding experimental values are 4.45% and 4.37%. APF not only improves the dynamic characteristic in the DC-link voltage control when the DC-link voltage controller with variable parameters is employed, but this filter also maintains excellent steady-state compensation performance. Therefore, the dynamic characteristic of DC-link voltage control and APF steady-state compensation performance are both satisfied when the nonlinear DC-link voltage controller with variable parameters is utilized.

VII. Conclusion

An adaptive DC-link voltage controller in a three-phase four-wire shunt APF is proposed in this paper. To implement this controller, the required minimum DC-link voltage for APF

is reduced. Moreover, a design block is constructed for this minimum DC-link voltage. The simulation and experiment results prove that once the DC-link voltage exceeds the minimum value, increasing DC-link voltage alone does not strengthen compensation effect significantly. However, this increase enhances power consumption and switch loss. Thus, the DC-link voltage reference is initially set to the required minimum value. Power consumption and switch loss can be reduced effectively if APF operates normally. Then, a block is built for adaptive reference DC-link voltage control given different harmonic currents and grid voltage levels. This block can adjust the reference value of DC-link voltage adaptively when the harmonic current and the grid voltage level fluctuate. Thus, this block guarantees the operation of APF and maintains ideal compensation performance. This block also reduces power consumption and switch loss in comparison with traditional fixed DC-link voltage control. Simulation and experimental results verify the viability and effectiveness of the required deduction in minimum DC-link voltage and the proposed adaptive DC-link voltage controller in the three-phase, four-wire shunt APF. Therefore, the proposed adaptive DC-link voltage controller is an optimal solution for practical situations.

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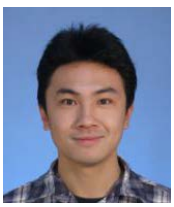

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