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An Effective Carrier-Based Modulation Strategy to Reduce the Switching Losses for Indirect Matrix Converters

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Abstract

In this paper, an effective carrier-based modulation (CBM) strategy to reduce the switching losses for indirect matrix converters (IMCs) is presented. The discontinuous pulse width modulation method is applied to decrease the switching numbers in one carrier cycle, and an optimum offset voltage is selected to avoid commutations of the high output phase currents. By decreasing the switching numbers along with avoiding commutation of the high currents, the proposed CBM strategy significantly reduces the switching losses in IMCs. In addition, the proposed CBM strategy is independent of load conditions, such as load power and power factor, and it has good performance in terms of the input/output waveforms. Simulation and experimental results are provided to verify the effectiveness of the proposed CBM strategy.

Key words: AC/AC converter, Carrier-based modulation method, Indirect Matrix Converter (IMC), Switching losses

I. INTRODUCTION

A matrix converter (MC) is a direct AC-to-AC power converter capable of generating an output voltage with an arbitrary amplitude and frequency from an AC power supply [1]. The MC has recently become more attractive because it has a number of advantages such as sinusoidal input/output current waveforms, a controllable input power factor, a simple and compact structure due to the absence of energy storage devices, and a bidirectional power flow [2]-[4]. MCs are generally divided into two types: the direct matrix converter (DMC) and the indirect matrix converter (IMC). IMCs and DMCs have similar performance in terms of their input/output current waveforms and voltage transfer ratios. Recently, the IMC in Fig. 1 has received more interest when compared to the DMC, due to its additional advantages, such as a simpler commutation and clamp circuit and an option to reduce the number of power switches for low-cost applications [5]-[12].

Despite their many interesting features, industrial applications for MCs are still not equivalent to their capability because they also have inherent problems. In terms of converter efficiency, the MC is known as an all-silicon power converter, and it causes higher switching losses than other AC/AC converter topologies. MC topologies usually use 18 insulated gate bipolar transistors (IGBTs) and 18 diodes compared to 6 IGBTs and 12 diodes in the diode rectifier/voltage source inverter (VSI) topology, and 12 IGBTs and 12 diodes in the back-to-back converter. A large number of semiconductor devices in a topology increases the switching losses of the converter. Switching losses reduce the efficiency of the system , and increase the need for cooling devices.

Several solutions have been proposed in order to reduce switching losses and increase efficiency in MCs. Kolar et al introduced a new modulation scheme to minimize the switching losses of a sparse MC in the low modulation range by using medium and minimum input line voltages to generate DC-link voltage [13]. A similar method, based on the space vector approach, can reduce switching losses from 15% to 35%, depending on the output power factor angle [14]. However, these methods are only applicable when the voltage transfer ratios are lower than 0.5.

Casadei et al [15] and Bradaschia et al [16] developed effective techniques to reduce switching losses based on discontinuous modulation. Casadei et al [15] exploited the features of the duty cycle space vector approach to reduce

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switching losses. This can decrease the switching numbers in one cycle and preserve the maximum voltage transfer ratio when compared with other methods. However, some of the switching states appear at high currents and high voltages, which results in high switching losses. Using generalized scalar pulse width modulation (PWM) to reduce switching losses in direct MCs was proposed by Bradaschia et al [16]. Although this technique can avoid commutation of the high output currents, the reduction of the switching numbers is not guaranteed during some sampling cycles. Itoh et al [17] introduced a control method that eliminates the switching losses in the inverter stage of an IMC. However, the total switching losses in the converter do not decrease, because the switching losses of the inverter stage are moved to the rectifier stage by adopting the zero voltage switching operation in the inverter stage instead of the rectifier stage. A predictive control approach to reduce the switching losses of direct MCs was presented by Vargas et al [18]. Most of the aforementioned research is focused on direct MCs. Switching loss reduction in IMCs has not been sufficiently studied until now.

This paper presents a modulation strategy based on the CBM method to minimize the switching losses in an IMC. The proposed CBM strategy uses a discontinuous modulation technique to clamp each output leg of the IMC while it conducts the largest current. This achieves a reduction in the switching numbers when compared with the traditional modulation strategy. Furthermore, the proposed CBM strategy can avoid commutation at the high magnitude of the output phase current by selecting a proper offset voltage. This significantly reduces the switching losses in the IMC. Therefore, this strategy reduces the switching numbers and guarantees only medium and low current commutations. Nevertheless, the proposed CBM strategy generates good performance in terms of the input/output current waveforms and keeps the maximum output voltage transfer ratio of the IMC, which are the drawbacks of previous modulation methods that minimize switching losses. The feasibility of the proposed CBM strategy is verified by simulation and experiment results.

II. Conventional CBM Strategy and Switching Losses Analysis in an IMC

The IMC topology is composed of two stages, as shown in Fig. 1. It has a rectifier stage and an inverter stage, and is well-known as a two-stage MC. The main objective of the rectifier stage is to provide a positive DC-link voltage and to generate sinusoidal input phase currents. The inverter stage is similar to that of a three-phase two-level inverter. In addition, an input filter is used to mitigate the high-frequency components to make the input phase currents sinusoidal and to avoid over-voltages. The conventional CBM for IMCs, which was first introduced by Wang and Venkataramanan

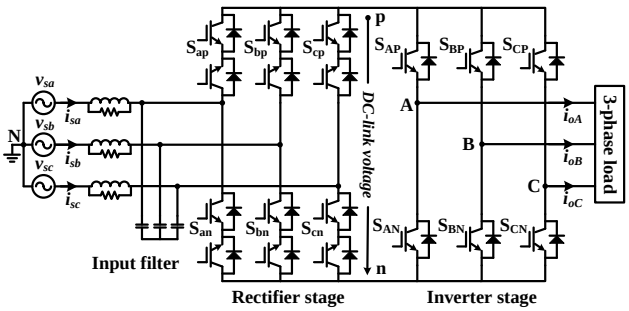

Fig. 1. Indirect matrix converter topology.

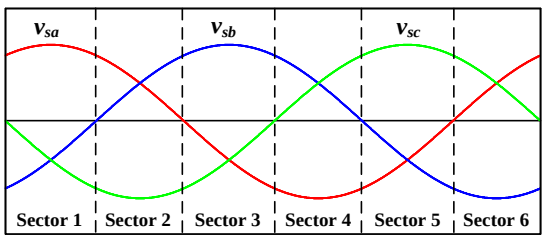

Fig. 2. Sector definition of input phase voltages.

[9], is a decoupling modulation method for both the rectifier stage and the inverter stage. The carrier signal used for the rectifier stage is different from that of the inverter stage. The carrier signal usually uses a saw-tooth carrier signal for the rectifier stage, while an asymmetrical triangular signal with different slopes at the rising and falling edges is used for the inverter stage. Then, the PWM signals for all of the switches are generated by comparing the modulation signals with the high-frequency carrier signal.

A. Rectifier Stage Modulation

It is assumed that the input voltages are balanced three-phase sinusoidal voltage sources:

$$v_{sa} = V_s \cos(\omega_s t) = V_s \cos(\theta_a) \quad (1)$$

$$v_{sb} = V_s \cos(\omega_s t - 2\pi/3) = V_s \cos(\theta_b) \quad (2)$$

$$v_{sc} = V_s \cos(\omega_s t + 2\pi/3) = V_s \cos(\theta_c) \quad (3)$$

where V_s is the amplitude and ω_s is the angular frequency of the input phase voltage.

Since the input voltages are balanced, there are two possible categories for the six sectors during one fundamental cycle of the input phase voltages, as shown in Fig. 2. In the first category, one input phase voltage is positive and two input phase voltages are negative (sectors 1, 3, and 5). In the second category, two input phase voltages are positive and one is negative (sectors 2, 4, and 6). In general, the control rules for all of the switches in each sector are as follows: the upper switch of the phase associated with a positive voltage is controlled to connect to the positive DC-bus *p*, while the lower switch of the phase associated with a negative voltage is controlled to connect to the negative DC-bus *n*. All of the other switches are kept in the OFF state.

To explain the modulation technique, it is assumed that the IMC operates at a unity input power factor, and that the input

TABLE I
SWITCHING STATES AND MODULATION SIGNALS FOR RECTIFIER STAGE

Sector	ON switch	Modulated switches		Modulation signals	
1	S_{ap}	S_{bn}	S_{cn}	$-v_{sb}/v_{sa}$	$-v_{sc}/v_{sa}$
2	S_{cn}	S_{ap}	S_{bp}	$-v_{sa}/v_{sc}$	$-v_{sb}/v_{sc}$
3	S_{bp}	S_{cn}	S_{an}	$-v_{sc}/v_{sb}$	$-v_{sa}/v_{sb}$
4	S_{an}	S_{bp}	S_{cp}	$-v_{sb}/v_{sa}$	$-v_{sc}/v_{sa}$
5	S_{cp}	S_{an}	S_{bn}	$-v_{sa}/v_{sc}$	$-v_{sb}/v_{sc}$
6	S_{bn}	S_{cp}	S_{ap}	$-v_{sc}/v_{sb}$	$-v_{sa}/v_{sb}$

phase voltages are located in sector 1. In this sector, the input phase voltage v_{sa} is positive, whereas the input phase voltages v_{sb} and v_{sc} are negative. Therefore, the upper switch of phase *a*, S_{ap}, is ON, and the lower switches of phase *b* and phase *c*, S_{bn} and S_{cn}, are modulated with the modulation signals given by:

$$v_{bn} = \frac{-v_{sb}}{v_{sa}} \quad \text{and} \quad v_{cn} = \frac{-v_{sc}}{v_{sa}} \tag{4}$$

It is obvious that the two modulation signals are always a sum of unity. Hence, the conducting states of the two modulated switches complement each other in this sector. Table I summarizes the modulation signals and the switching states for all of the sectors.

The average value of the DC-link voltage for each sector is:

$$\bar{V}_{dc} = \frac{3V_s}{2\cos(\theta_{in})} \tag{5}$$

where $\cos(\theta_{in}) = \max(|\cos(\theta_a)|, |\cos(\theta_b)|, |\cos(\theta_c)|)$.

Once the modulation signals are derived, the PWM signals for the switches are generated by comparing these modulation signals with a saw-tooth carrier signal, which is illustrated in Fig. 3.

B. Inverter Stage Modulation

In order to control the inverter stage, the conventional CBM methods for VSIs are adopted. However, in the IMC topology, the DC-link voltage generated by the rectifier stage is not constant. The average value of the DC-link voltage vacillates with a frequency that is six times the input voltage frequency. Therefore, the adoption of VSI modulation techniques should be modified to control the inverter stage of the IMC.

At first, the reference modulation signals of the three output phases are given by:

$$v_{oAref} = \frac{V_{oref}}{\bar{V}_{dc}}\cos(\omega_o t) \tag{6}$$

$$v_{oBref} = \frac{V_{oref}}{\bar{V}_{dc}}\cos(\omega_o t - 2\pi/3) \tag{7}$$

$$v_{oCref} = \frac{V_{oref}}{\bar{V}_{dc}}\cos(\omega_o t - 4\pi/3) \tag{8}$$

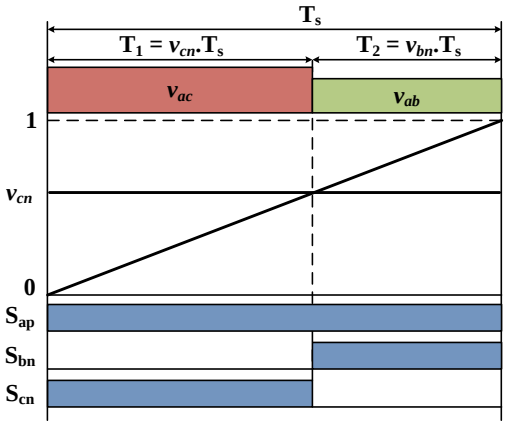

Fig. 3. Carrier-based modulation technique for the rectifier stage.

where V_{oref} and ω_o are the amplitude and angular frequency of the desired output phase voltages, respectively.

It is well-known that a zero-sequence signal can be injected into the reference modulation signals to improve the performance of the CBM methods for VSIs and IMCs. The zero-sequence signal, which is usually called an offset voltage component, v_{offset}, can be arbitrarily selected. A proper offset voltage selection will extend the voltage linearity range, improve the waveform quality, and reduce the switching losses significantly. Therefore, many researchers have investigated the offset voltage component with CBM methods [19]-[22].

The modified modulation signals of the inverter stage are as follows:

$$v_{oA} = v_{oAref} + v_{offset} \tag{9}$$

$$v_{oB} = v_{oBref} + v_{offset} \tag{10}$$

$$v_{oC} = v_{oCref} + v_{offset} \tag{11}$$

To obtain balanced output voltages and input currents in each carrier cycle, the switching events of the inverter stage should be synchronized with those of the rectifier stage. Fig. 4 shows an example of the switching sequence of the inverter stage synchronized with the commutation in the rectifier stage. The falling and rising slopes of the carrier signal in the inverter stage are determined by the intervals T_1 and T_2, which are the switching intervals in the rectifier stage. Fig. 4 also shows that the switching events in the rectifier stage always happen during the zero state of the inverter stage, i.e., the rectifier stage commutation takes place when the DC-link current is zero. As a result, the switching losses in the rectifier stage are naturally eliminated.

C. Switching Losses Analysis

The switching losses in PWM converters have been analyzed very well [14], [23]-[25]. In general, assuming that the current and voltage turn-on and turn-off characteristics of the switching devices are linear with respect to time, the switching losses P_{sw} of a PWM converter are determined as follows:

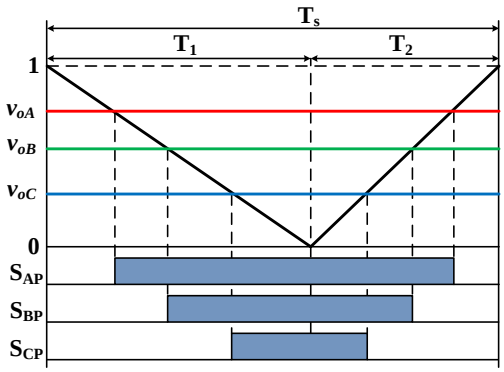

Fig. 4. Carrier-based modulation technique for the inverter stage.

$$P_{sw} \propto v_{sw}\, i_{sw}\, (T_{on} + T_{off})\, f_{sw} \tag{12}$$

where v_{sw} is the switched voltage, i_{sw} is the switched current, f_{sw} is the switching frequency, and T_{on} and T_{off} are the turn-on and turn-off times of the switching devices, respectively.

From Equation (12), the switching losses are reduced by reducing the switched voltage/current and switching frequency or by improving the characteristics of the switching devices, such as minimizing the turn-on/turn-off processes of the power semiconductor devices. As a simple solution, the switching losses can easily be reduced if the switched voltage is decreased at the switching instant. However, this solution attenuates the voltage modulation range. In PWM converters, a low switching frequency also results in reducing the switching losses. However, this solution diminishes the performance of the converters. Considering these factors, minimization of the switching current is a useful solution to reduce switching losses. For the IMC, because the switching losses of the rectifier stage are eliminated in a straightforward manner by commutating at the zero DC-link current, the total switching losses are consequently dependent on the switching sequence of the power switches in the inverter stage and are proportional to the output phase current magnitude at the switching instant.

III. Proposed Carrier-Based Modulation Method to Reduce Switching Losses

A. Discontinuous CBM Strategy

CBM methods can be classified into two groups: continuous PWM (CPWM) and discontinuous PWM (DPWM) [20], [21]. In the CPWM methods, the magnitude of the modulation signals is always smaller than that of the carrier signal. As a result, the switching state changes between ON and OFF within each carrier cycle. Meanwhile, the modulation signals in the DPWM methods are saturated with the upper or lower boundaries of the carrier signal. Therefore, the switches associated with the saturation are kept ON or OFF during the carrier cycle and consequently the switching numbers are decreased. Therefore, the DPWM methods are widely used to reduce the switching losses in PWM converters.

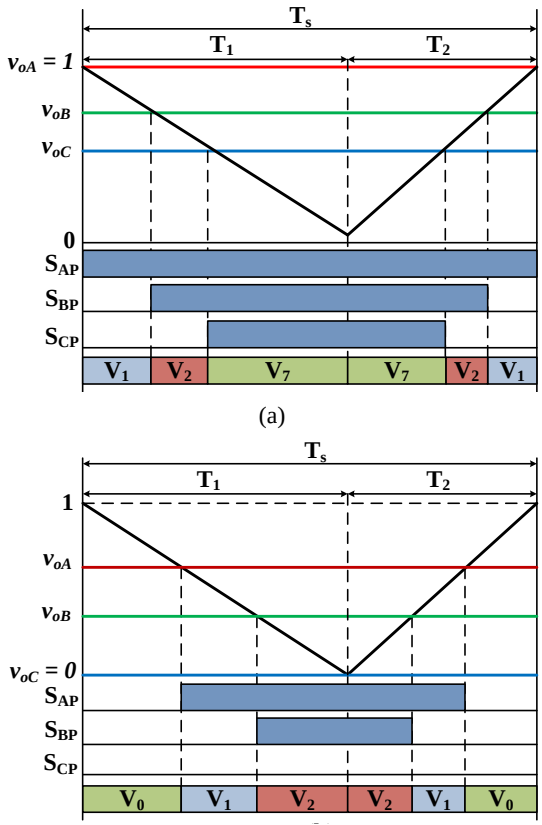

Fig. 5. Switching sequences. (a) The DPWM-MAX method. (b) The DPWM-MIN method.

PWM methods can be classified into three groups: sinusoidal PWM (SPWM), space vector PWM (SV-PWM), and the DPWM-MAX and DPWM-MIN methods according to the offset voltage value, v_{offset}.

With SPWM, the offset voltage is set at zero.

With SV-PWM, the offset voltage is chosen as follows:

$$v_{offset} = \frac{v_{max} + v_{min}}{2} \tag{13}$$

where:

$$\begin{cases} v_{max} = 1 - v_{omax} \\ v_{min} = -v_{omin} \end{cases} \tag{14}$$

and:

$$\begin{cases} v_{omax} = \max(v_{oAref}, v_{oBref}, v_{oCref}) \\ v_{omin} = \min(v_{oAref}, v_{oBref}, v_{oCref}) \end{cases} \tag{15}$$

The DPWM-MAX and DPWM-MIN methods are realized with the switching sequences illustrated in Fig. 5(a) and Fig. 5(b), respectively. Their offset voltages are as follows:

$$v_{offset} = v_{max} \quad \text{and} \quad v_{offset} = v_{min} \tag{16}$$

The distributions of the thermal stresses on the power switches in these methods are unbalanced because the conduction times of the upper switches and lower switches are different. As can be seen, the switching numbers of the DPWM methods in Fig. 5 are smaller than the switching

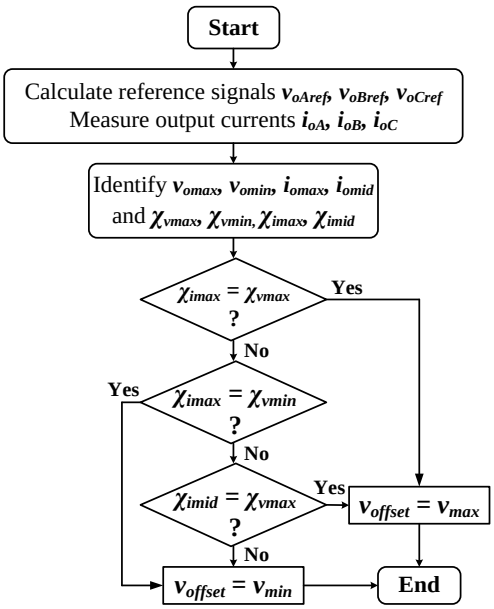

Fig. 6. The flow chart of the offset voltage selection algorithm.

number of the SV-PWM in Fig. 4. However, the DPWM-MAX and DPWM-MIN methods cannot use the zero DC-link current commutation in the rectifier stage.

On the other hand, in order to choose a phase to clamp the switches ON or OFF, most of the DPWM methods presented to reduce switching losses for the MC and the VSI [14]-[16], [23]-[25] need to know the output displacement angle before choosing a suitable offset voltage value. Thus, the offset voltage changes if the load condition changes. In order to overcome this problem, an effective CBM strategy is introduced with an additional algorithm to select an appropriate offset voltage, which is independent of the output displacement angle.

B. Offset Voltage Selection

In order to choose an offset voltage regardless of the load power factor, the offset voltage selection principle for a VSI [26] is applied to select the offset voltage for the modulation of the IMC inverter stage. The switching losses are reduced by adjusting the offset voltage to avoid commutation at the high magnitude of the output phase current. In this paper, an optimal voltage offset selection algorithm is proposed by considering the output phase current magnitude.

First, the maximum and minimum values in Equation (15) are determined from the modulation signals in equations (6)-(8). Then χ_{vmax} and χ_{vmin} are defined so that they represent phases that have the maximum and minimum modulation signals, respectively:

$$\begin{cases} \chi_{vmax} = M \ \text{ if } \ v_{oMref} = v_{omax} \\ \chi_{vmin} = N \ \text{ if } \ v_{oNref} = v_{omin} \end{cases} \tag{17}$$

where M, $N = \{A, B, C\}$, one of three output phases.

Second, the maximum and medium output current magnitudes are identified as follows:

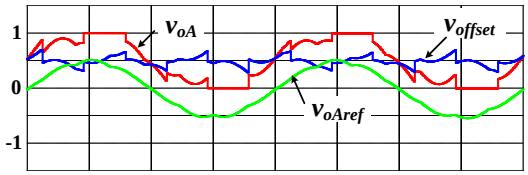

Fig. 7. The waveforms of the reference modulation signal, the offset voltage, and the modified modulation signal in the proposed CBM method.

$$\begin{cases} i_{omax} = \max\left(|i_{oA}|, |i_{oB}|, |i_{oC}|\right) \\ i_{omid} = \text{mid}\left(|i_{oA}|, |i_{oB}|, |i_{oC}|\right) \end{cases} \tag{18}$$

Then χ_{imax} and χ_{imid} are defined as the phases to conduct the maximum and medium output phase currents, respectively:

$$\begin{cases} \chi_{imax} = X \ \text{ if } \ |i_{oX}| = i_{omax} \\ \chi_{imid} = Y \ \text{ if } \ |i_{oY}| = i_{omid} \end{cases} \tag{19}$$

where X, $Y = \{A, B, C\}$, one of three output phases.

Fig. 6 shows how to select an optimal offset voltage that can reduce the switching losses. Fig. 7 illustrates the waveforms of the reference modulation signal, the offset voltage and the modified modulation signal of the proposed CBM strategy.

C. Case Study

In order to explain the principle of the proposed algorithm, two examples are introduced. First, it is assumed that the magnitudes of the three reference modulation signals are defined as $v_{oAref} > v_{oBref} > v_{oCref}$. In this case, the maximum and minimum allowable values of the offset voltage are given as v_{max} and v_{min}, as in Fig. 8(a).

In the first case, the magnitudes of the three output phase currents are assumed to be $|i_{oA}| \geq |i_{oB}| \geq |i_{oC}|$, i.e., the largest current flows in phase *A*. In order to avoid maximum current commutation, the reference modulation signals are shifted with the maximum offset voltage, v_{max}, as shown in Fig. 8(b), to cease commutation in phase *A*. The modulation signal of phase *A* reaches the upper boundaries of the carrier signal, and the switching state of phase *A* is held.

In the second case, with different load conditions, the magnitudes of the output phase currents are $|i_{oB}| \geq |i_{oC}| \geq |i_{oA}|$, i.e., the maximum and medium currents flow in phase *B* and phase *C*, respectively. In order to avoid commutation in phase *B*, the modulation signal of phase *B* should be moved to the upper boundary or moved down to the lower boundary of the carrier signal. However, if phase *B* is moved, the modulation signals of phase *A* or phase *C* leave the upper or lower boundary of the carrier signal, as shown in Fig. 8(a). Therefore, the offset voltage v_{offset} is chosen as v_{min} to avoid commutation in phase *C*, which flows with the medium current, as shown in Fig. 8(c).

As a result, an optimum offset voltage can be selected regardless of the load condition without any information

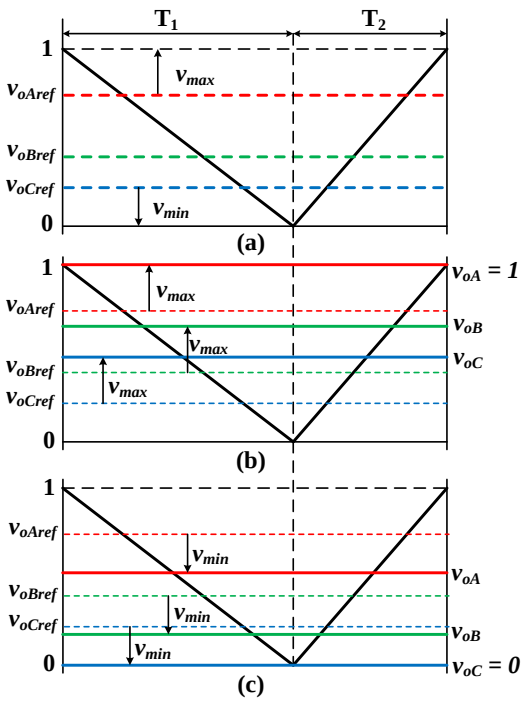

Fig. 8. Examples of the offset voltage selection. (a) Initial modulation signals and modified modulation signals when (b) $v_{offset} = v_{max}$ and (c) $v_{offset} = v_{min}$ in one cycle of the carrier signal.

about the output displacement angle. As a result, the switching losses are reduced when compared to the previous switching methods.

IV. Simulation Results

Simulations were carried out using PSIM 9.0 software in order to verify the effectiveness of the proposed CBM method. The system was simulated with the following parameters:

1) Power supply (line-to-line voltage) is 122 V/60 Hz.
2) Three-phase *RL* load has $R = 20\ \Omega$ and $L = 15$ mH.
3) Input filter parameters are $L = 1.4$ mH and $C = 25$ μF.
4) Output frequency f_{out} is 50 Hz.
5) Voltage transfer ratio q is 0.7.
6) All of the switches in the IMC are ideal.
7) Frequency of the saw-tooth carrier signal is 10 kHz.

In order to investigate the reduced switching losses, the Thermal Module in PSIM was used. In the simulation model, the SPA21N50C3 power switch, manufactured by Infineon, was used to implement the power circuits for both the rectifier and inverter stages with the following specifications: $V_{DS,max} = 560$ [V], $I_{D,max} = 21$ [A] and $T_{j,max} = 150^{o}$C. The power switching losses are calculated under the same conditions according to different voltage transfer ratios and load power factor angles for the SV-PWM method, the

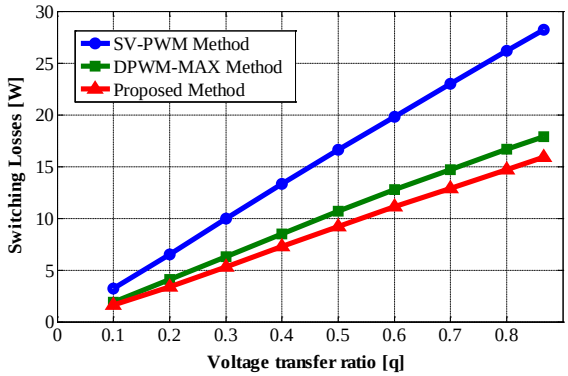

Fig. 9. Power switching losses with different voltage transfer ratios.

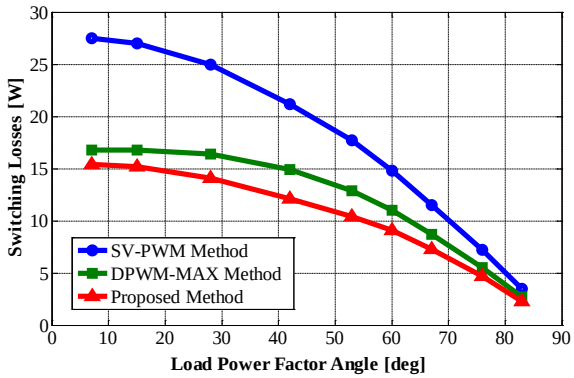

Fig. 10. Power switching losses with different load power factor angles.

DPWM-MAX method, and the proposed CBM method. They are plotted in Fig. 9 and Fig. 10, respectively. The lowest power switching losses are achieved with the proposed CBM strategy. These figures validate the effectiveness of the proposed CBM strategy as a switching loss reduction technique.

The DC-link voltage waveform of the proposed CBM method is shown in Fig. 11. It can be seen that the DC-link voltage is modulated between the two line-to-line input voltages. Its waveform is not affected by the inverter stage modulation and it does not decrease to zero because the zero states are not used in the rectifier stage.

Figs. 12, 13, and 14 show the currents and voltages of the input and output sides with the SV-PWM method, the DPWM-MAX method and the proposed CBM method, respectively. From these results, it can be seen that the waveforms of the input currents and output currents are sinusoidal and balanced. The output line voltage performance of the proposed CBM method is similar to other methods.

The output phase-to-neutral voltages with the SV-PWM method, the DPWM-MAX method and the proposed CBM method are shown in Fig. 15 (a), (b), and (c), respectively. As shown in Figs. 12 to 14, all of the methods have the same output line-to-line voltages. However, the waveforms of the output phase-to-neutral voltages in Fig. 15 are different from each other due to the different offset voltage values.

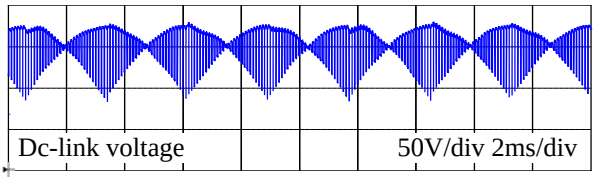

Fig. 11. DC-link voltage waveform.

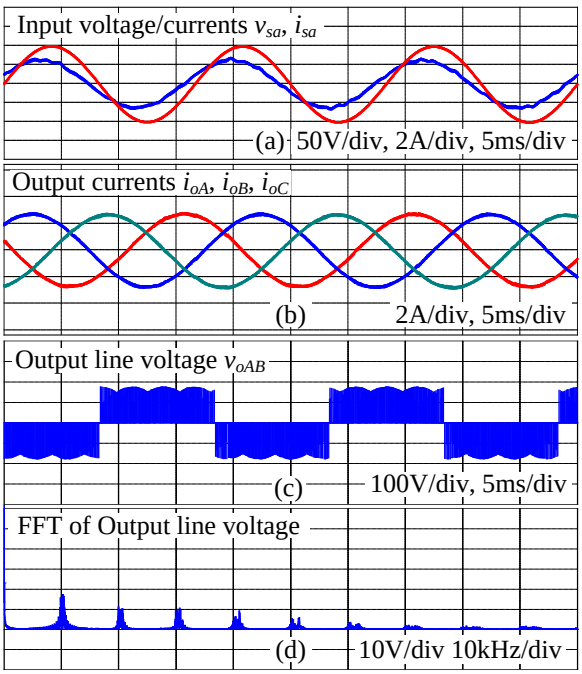

Fig. 12. Simulation results. (a) Input voltage/current. (b) Three-phase output current. (c) Line-to-line output voltage. (d) FFT of line-to-line output voltage with the SV-PWM method.

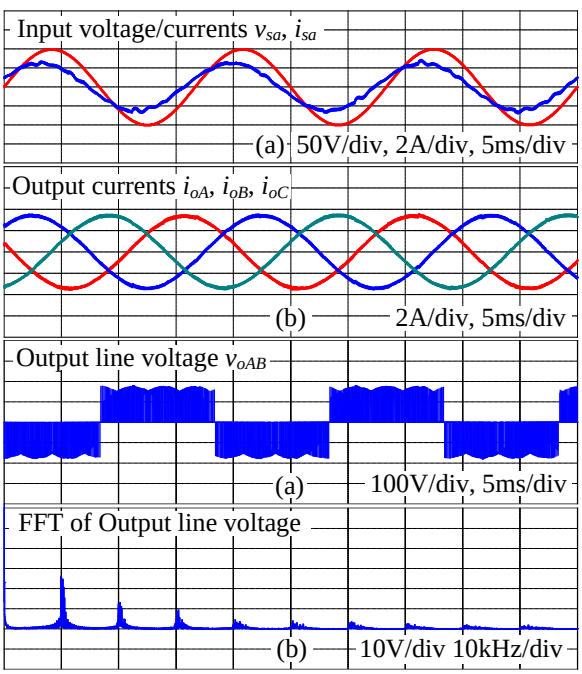

Fig. 13. Simulation results. (a) Input voltage/current. (b) Three-phase output current. (c) Line-to-line output voltage. (d) FFT of line-to-line output voltage with the DPWM-MAX method.

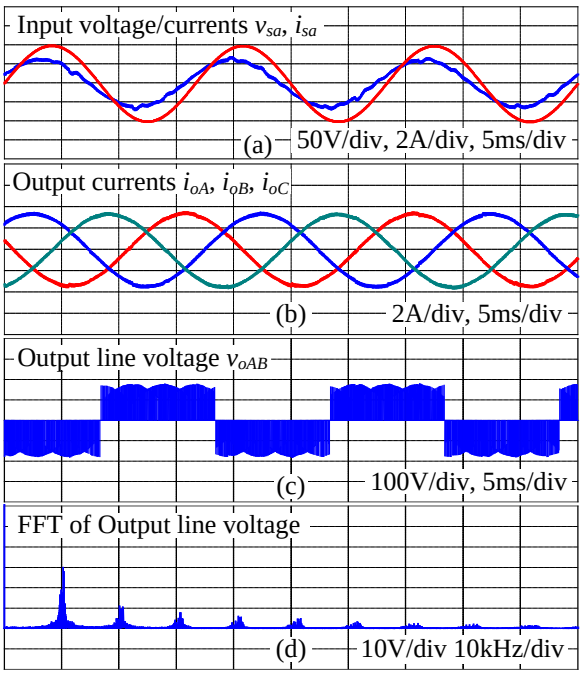

Fig. 14. Simulation results. (a) Input voltage/current. (b) Three-phase output current. (c) Line-to-line output voltage. (d) FFT of line-to-line output voltage with the CBM method.

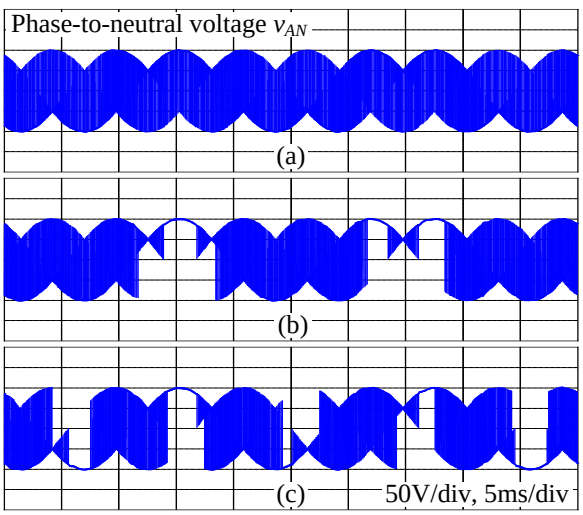

Fig. 15. Simulation results of phase-to-neutral output voltage. (a) With the SV-PWM method. (b) With the DPWM-MAX method. (c) With the proposed CBM method.

V. Experimental Results

In order to validate both the proposed CBM strategy and the simulation results, an experimental setup was implemented in the laboratory. A block diagram of the experimental system, including a control board, measurement boards, IGBT driver boards, and a power circuit board, is shown in Fig. 16. The control board is designed with a 32-bit DSP TMS320F28335 with a clock speed of 150 MHz and a CPLD Altera EPM7128SLC84-15. The parameters used in the experiment are the same as those used in the simulation.

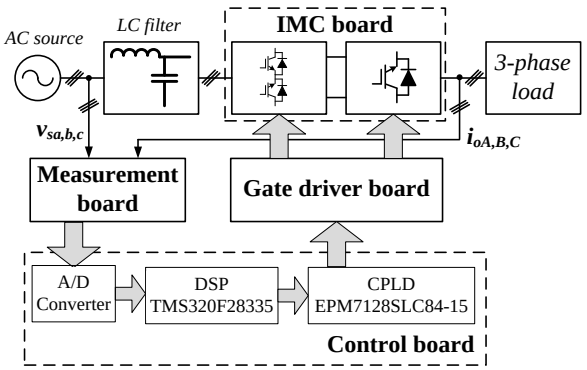

Fig. 16. Block diagram of the hardware configuration.

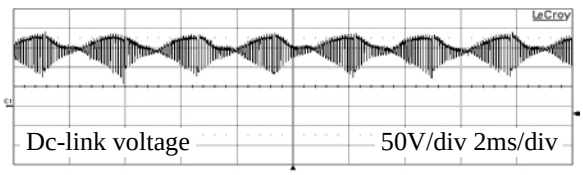

Fig. 17. Experimental results of the DC-link voltage waveform.

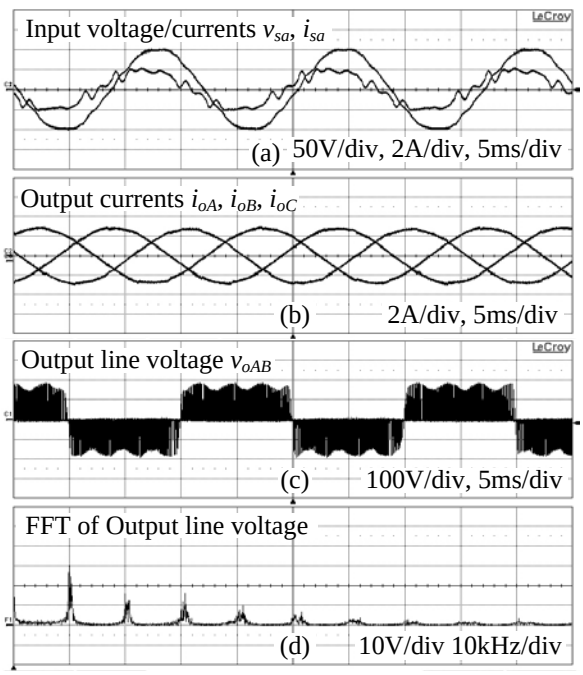

Fig. 18. Experimental results. (a) Input voltage/current. (b) Three-phase output current. (c) Line-to-line output voltage. (d) FFT of line-to-line output voltage with the SV-PWM method.

The experimental result shown in Fig. 17 is the DC-link voltage waveform. The DC-link voltage is switched to the maximum and medium line-to-line voltages in order to achieve the maximum average DC-link voltage.

Figs. 18 to 20 show the experimental results of the currents and voltages of the rectifier stage and inverter stage with the SV-PWM method, the DPWM-MAX method and the proposed CBM method. As shown in these figures, the input phase current of the proposed CBM method is nearly sinusoidal. However, it contains a ripple, and there is a displacement angle

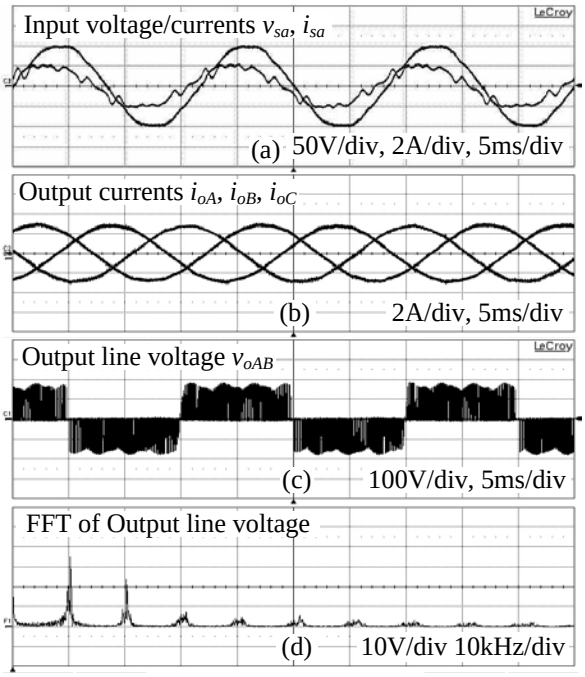

Fig. 19. Experimental results. (a) Input voltage/current. (b) Three-phase output current. (c) Line-to-line output voltage. (d) FFT of line-to-line output voltage with the DPWM-MAX method.

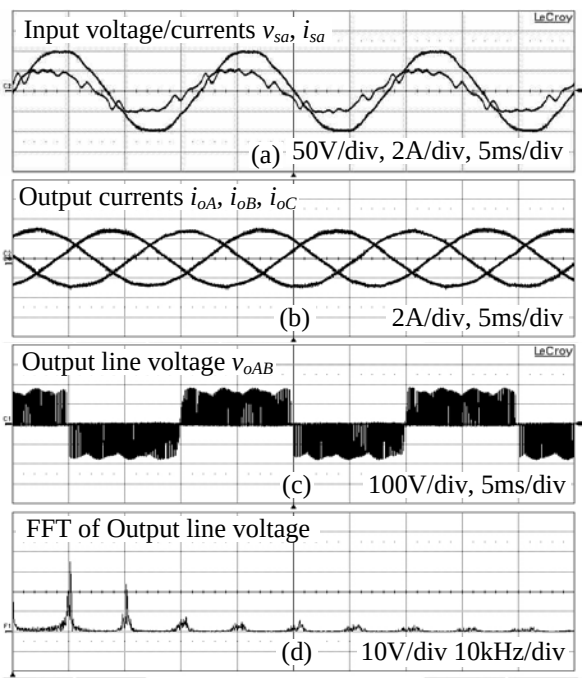

Fig. 20. Experimental results. (a) Input voltage/current. (b) Three-phase output current. (c) line-to-line output voltage, and (d) FFT of line-to-line output voltage with the proposed CBM method.

between the input current and the voltage due to the *LC* input filter. The proposed CBM method does not consider the input power factor compensation. The output phase currents and line voltages of the three methods are the same.

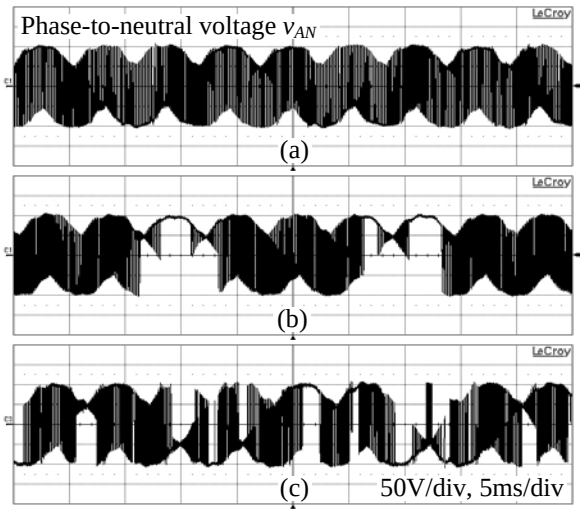

Fig. 21. Experimental results of line-to-neutral output voltage. (a) With the SV-PWM method. (b) With the DPWM-MAX method. (c) With the proposed CBM method.

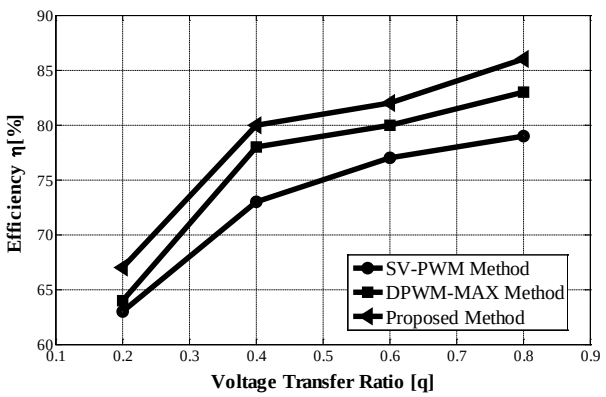

Fig. 22. Experimental results of system efficiency.

The experimental results of the output phase-to-neutral voltage with the SV-PWM method, the DPWM-MAX method and the proposed CBM method are shown in Fig. 21 (a), (b), and (c), respectively. From Fig. 21, even though the waveforms are slightly different due to the different offset voltage values, the experimental results are in complete agreement with the simulation results.

In order to compare the efficiency of the proposed CBM method with those of the other methods, the input active power and output active power of the system are measured by using a HIOKI 3193 Power HiTester. The system efficiency of the three methods with different voltage transfer ratios are plotted in Fig. 22. The proposed CBM method has the highest efficiency due to the minimum switching losses, as shown in the simulation results.

VI. CONCLUSION

This paper presented an effective CBM strategy for an IMC to reduce the switching losses and to increase efficiency. The proposed CBM strategy decreased the switching numbers by using the DPWM technique to cease the switching sequence of one output leg of the IMC during a carrier signal cycle. In order to reduce the amount of switching losses, this paper also introduces a way to select an optimum offset voltage component to avoid commutations of the high output phase currents. The proposed CBM strategy can be applied to reduce switching losses regardless of the voltage transfer ratio or the load condition of an IMC. Simulation and experimental results are provided to demonstrate the effectiveness of the proposed CBM strategy.

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