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Hybrid ZVS Converter with a Wide ZVS Range and a Low Circulating Current

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Abstract

This paper presents a new hybrid soft switching dc-dc converter with a low circulating current and high circuit efficiency. The proposed hybrid converter includes two sub-converters sharing two power switches. One is a three-level PWM converter and the other is a *LLC* converter. The *LLC* converter and the three-level converter share the lagging-leg switches and extend the zero-voltage switching (ZVS) range of the lagging-leg switches from nearly zero to full load since the *LLC* converter can be operated at f_{sw} (switching frequency) $\approx f_r$ (series resonant frequency). A passive snubber is used on the secondary side of the three-level converter to decrease the circulating current on the primary side, especially at high input voltage and full load conditions. Thus, the conduction losses due to the circulating current are reduced. The output sides of the two converters are connected in series. Energy can be transferred from the input voltage to the output load within the whole switching period. Finally, the effectiveness of the proposed converter is verified by experiments with a 1.44*k*W prototype circuit.

Key words: Hybrid three-level PWM converter, *LLC* converter, Phase-shift PWM, ZVS

I. INTRODUCTION

Full-bridge converters with a high power density and high efficiency have been proposed and used in many industry products such as server power units [1], telecommunication power units [2], and electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) battery chargers [3], [4]. Single-phase power factor correction (PFC) is normally adopted in the front stage to eliminate the current harmonics, increase the input power factor and keep the dc bus voltage at a constant voltage against line voltage and load current variations. For medium/high power ratings, power converters with a three-phase ac utility are adopted to reduce the current rating from the ac source. The power factors of these converters are normally required to improve the power quality of utility systems. Three-phase PFC with a unidirectional or bidirectional power flow and bridge/bridgeless circuit topologies can be adopted in the front stage. However, the dc bus voltage of the three-phase PFC will be higher than 750V or 800V. Thus, the power switches in the dc-dc converters of the rear stage must have 900V or 1200V voltage stress. Three-level dc-dc converters [5]-[7] with low voltage stress of the active switches are widely used in industry applications due to their high switching frequency and small size demands. Phase-shift pulse-width modulation (PWM) is normally adopted to generate the gate voltages of three-level converters. The main drawback of phase-shift PWM is that the lagging-leg switches have a narrow range of ZVS operation due to the limited energy stored in the primary leakage inductance. To overcome this problem, a large leakage inductance [8] or an external resonant inductance [3] can be placed on the primary side to extend the ZVS range of the lagging-leg switches. However, this approach also increases the duty cycle loss and decreases the effective duty cycle on the secondary side. In [9], [10], auxiliary circuits are added on the primary side to increase the ZVS load range. The switching power losses of the switches are improved. However, the power losses of the additional auxiliary circuits will decrease the total circuit efficiency. Recently, an *LLC* converter and a full-bridge converter sharing lagging-leg switches have been studied in [11], [12]. Thus, the ZVS range of the switches can be extended from zero to full load conditions. The other main problem of the phase-shift PWM scheme for full-bridge converters and three-level converters is its high circulating

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current during the freewheeling interval. To overcome this drawback, active or passive clamp circuits [4] and [13] can be added on the secondary side to limit voltage overshoots and oscillations across the output diodes when they are turned off, and to improve the circulating current losses on the primary side. However, an additional gate driver is needed to control the secondary active switch which will increase the circuit complexity and decrease the circuit reliability.

A hybrid three-level ZVS converter is studied in this paper to have the advantages of wide range of ZVS operation and low circulating current losses. The proposed hybrid converter combines a conventional three-level PWM converter and a half-bridge *LLC* converter with fixed switching frequency sharing of the lagging-leg switches to reduce the switch counts. Since the switching frequency of the *LLC* converter is greater than the series resonant frequency, the active switches at the lagging-leg can be turned on under ZVS from zero to full load conditions. The output voltages of the half-bridge *LLC* converter and the three-level PWM converter are connected in series. Thus, energy can be transferred from the input to the output load within the whole switching cycle. A passive snubber is adopted on the secondary side to provide a positive rectified voltage during the freewheeling interval to decrease the primary side current. Thus, the high circulating current in the conventional three-level PWM converter is rapidly reduced and the converter efficiency is improved. In the meantime, the rectified voltage on the secondary side during the freewheeling interval is positive instead of zero in the conventional three-level converter. The output inductance in the proposed hybrid converter can also be reduced. Finally, experiments with a 1.44*k*W prototype circuit are provided to demonstrate the performance of the proposed converter.

II. PROPOSED CONVERTER

Fig. 1 shows a general three-phase ac-dc converter for industry power units. The front-stage is a three-phase power factor corrector to achieve a low total harmonic distortion of the three-phase line currents, a high power factor and a stable high dc bus voltage. The second stage is a high frequency link dc-dc converter based on a full-bridge converter with IGBT power switches or a three-level PWM converter with power MOSFETs to provide a stable low dc bus voltage and high load current. In order to reduce the converter size and weight, a three-level PWM converter with power MOSFETs and a high switching frequency is generally used to achieve this demand. Fig. 2 shows a circuit diagram of the proposed high frequency dc-dc converter to overcome the disadvantages of conventional three-level PWM converters. There are two sub-converters in the proposed dc-dc converter. One is a three-level PWM converter (C_{d1}, C_{d2}, D_1, D_2, C_f, S_1-S_4, T_1, L_{r1}, D_{r1}, D_{r2}, C_c, D_a, D_b, L_o and C_{o1}) and the other is an *LLC* circuit (C_f, S_2, S_3, L_{r2}, C_r, T_2, D_{r3}, D_{r4} and C_{o2}). S_1 and

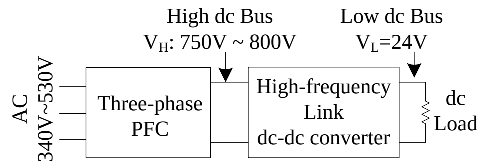


Fig. 1. Three-phase ac-dc converter with two-stage conversion.

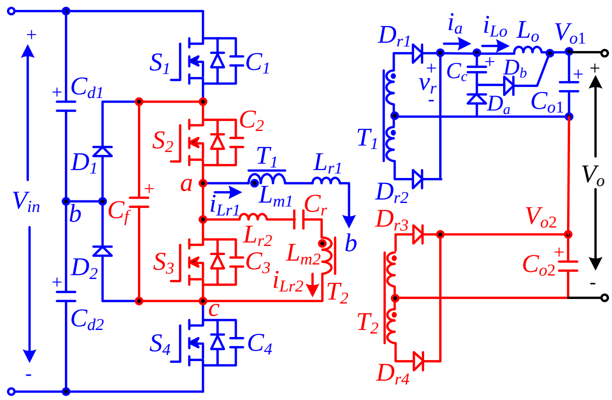


Fig. 2. Circuit diagram of the proposed hybrid ZVS converter.

S_4 are in the leading-leg, and S_2 and S_3 are in the lagging-leg. The *LLC* circuit is operated at a fixed switching frequency so that the output voltage V_{o2} is un-regulated. However, the total output voltage V_o is regulated by the three-level PWM circuit using the phase-shift PWM scheme. The energy stored in the output inductor L_o is reflected to the primary side to help the leading-leg switches turn-on at ZVS from light load to full load conditions. The *LLC* circuit, sharing the lagging-leg switches S_2 and S_3 of the three-level PWM circuit, is operated at a fixed switching frequency. The adopted switching frequency f_{sw} is close to the series resonant frequency f_r in the *LLC* circuit. The lagging-leg switches S_2 and S_3 can be turned on at ZVS from nearly zero to full load conditions. Thus, power switches S_1-S_4 in the proposed circuit have a wide range of ZVS operation when compared to the ZVS range in the conventional three-level converter. In order to reduce the circulating current of the three-level converter, a passive snubber circuit including C_c, D_a and D_b is used on the secondary side to provide a dc voltage during the freewheeling interval. During the freewheeling interval, the rectified voltage v_r=v_{Cc}. The reflected voltage n_1v_r is applied to L_{r1} on the primary side to reduce the circulating current to zero, and the output inductor voltage v_{Lo}=v_{Cc}-v_{o1} instead of -v_{o1}. Thus, the high circulating current losses in the conventional three-level converter are improved in the proposed converter. Since the output voltages of the three-level circuit and the *LLC* circuit are connected in series, the input energy of the *LLC* circuit can be delivered to the output load in the whole switching cycle.

III. OPERATION PRINCIPLES

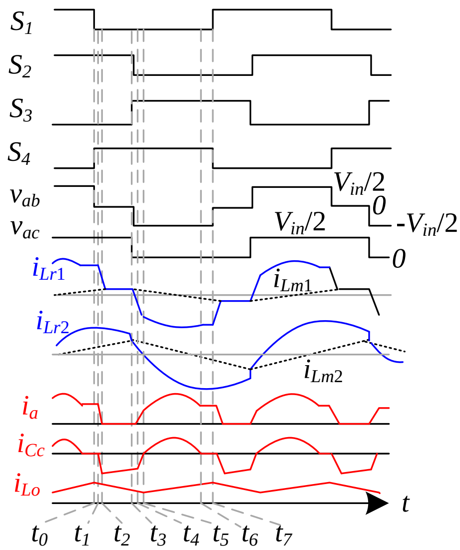


Fig. 3. Key waveforms of the proposed converter during one half of switching cycle.

In the proposed converter, the turn-on time of each power switch is equal to half of a switching period. The PWM signal of S_2 (S_3) is phase-shifted with respect to the PWM signal of S_1 (S_4). S_1 (S_2) and S_4 (S_3) operate complementarily with a short dead time to avoid short circuits. The operation principles of the proposed converter are based on the following assumptions. 1) MOSFETs S_1-S_4 and rectifier diodes D_{r1}-D_{r4}, D_1-D_2 and D_a-D_b are ideal, 2) capacitor voltages v_{Cd1}, v_{Cd2}, v_{Cf}, V_{o1} and V_{o2} are constant, the turns ratios of T_1 and T_2 are n_1=n_{p1}/n_{s1} and n_2=n_{p2}/n_{s2}, respectively, and 3) C_1=C_2=C_3=C_4=C_{oss} and V_{Cd1}=V_{Cd2}=V_{Cf}=$V_{in}/2$. Fig. 3 illustrates the key PWM waveforms of the proposed converter in a switching cycle. According to the switching states of S_1-S_4, D_{r1}-D_{r4}, D_1-D_2 and D_a-D_b, the converter has seven operation modes in each half of a switching period. Fig. 4 gives the equivalent circuits for the seven operation modes.

Mode 1 [t_0 - t_1]: Prior to t_0, the power semiconductors S_1, S_2, D_{r1} and D_{r3} are conducting. Both of the inductor currents i_{Lr1} and i_{Lr2} are positive. S_1 is turned off at t_0. C_1 and C_4 are charged and discharged, respectively, by i_{Lr1}. The energy stored in the output inductor L_o and the primary inductor L_{r1} is used to discharge C_4 to zero voltage. The ZVS condition of S_4 is illustrated in (1).

$$(L_{r1}+n_1^2L_o)i_{Lr1}^2(t_0)\geq\frac{C_{oss}V_{in}^2}{2} \tag{1}$$

This mode ends at t_1 when v_{C1}=$V_{in}/2$ and v_{C4}=0. The time interval of mode 1 is given in (2).

$$\Delta t_{01}=t_1-t_0=\frac{C_{oss}V_{in}}{i_{Lr1}(t_0)}\approx\frac{C_{oss}V_{in}}{i_{Lo,\max}/n_1} \tag{2}$$

The dead time between S_1 and S_4 must be greater than Δt_{01} to achieve the ZVS operation of S_4.

Mode 2 [t_1 - t_2]: Mode 2 starts at t_1 when v_{C1}=$V_{in}/2$, v_{C4}=0, and D_1 and D_a are on. Since i_{Lr1} is positive, the output diode of S_4 is conducting. At this moment, S_4 can be turned on under ZVS. In this mode, the primary side voltages v_{ab}=0 and v_{ac}=v_{Cf}=$V_{in}/2$ in the steady state. Since D_a is on, the rectified voltage v_r=v_{Cc} and v_{Lo}=v_{Cc}-V_{o1}<0. The inductor current i_{Lo} decreases with a slope of (v_{Cc}-V_{o1})/L_o. The reflected secondary windings voltage -n_1v_{Cc} is applied to L_{r1} so that the primary side current i_{Lr1} rapidly decreases to zero with a slope of -n_1v_{Cc}/L_{r1}. The time interval in mode 2 is obtained in (3).

$$\Delta t_{12}=t_2-t_1=\frac{L_{r1}i_{Lo}(t_2)/n_1}{n_1v_{Cc}}\approx\frac{L_{r1}I_o}{n_1^2v_{Cc}} \tag{3}$$

In the conventional three-level converter, the primary current i_{Lr1} in this mode is kept at the same value of $i_{Lr1}(t_1)$ because v_{Lr1}=0. Thus, the conventional three-level converter has large circulating current losses during the freewheeling interval. The energy stored in the clamped capacitor C_c is transferred to the output load through L_o and D_a. The secondary winding current i_a decreases in this mode. The *LLC* converter is still in the resonant mode to transfer energy from the input to the output load.

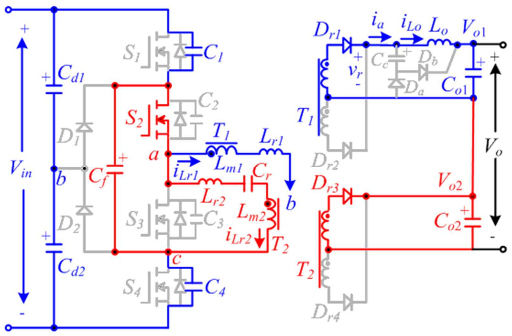
Mode 3 [t_2 - t_3]: Mode 3 starts at t_2 when the secondary winding current i_a decreases to zero, and the capacitor current i_{Cc}=-i_{Lo}. The primary side current i_{Lr1} is approximately zero and the primary and secondary sides of T_1 are disconnected. There is no circulating current loss in this mode. The output inductor voltage v_{Lo}=v_{Cc}-V_{o1}<0 and i_{Lo} decreases. The *LLC* circuit continuously transfers energy from C_f to the output load.

Mode 4 [t_3 - t_4]: Mode 4 starts at t_3 when S_2 is turned off. i_{Lr2} charges C_2 to $V_{in}/2$ and discharges C_3 to zero. The *LLC* converter is operated at f_{sw} (switching frequency) ≈ f_r (series resonant frequency). Thus, the inductor current i_{Lr2} is lagging with respect to the input fundamental voltage $v_{ac,f}$.

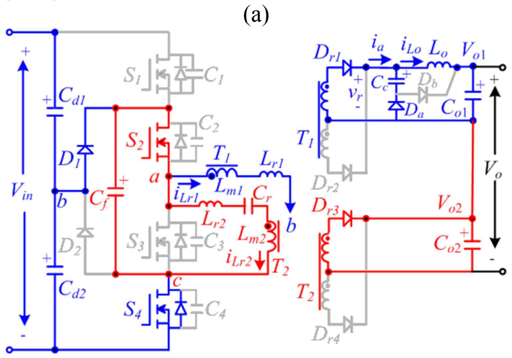
Mode 5 [t_4 - t_5]: Mode 5 starts at t_4 when the capacitor C_3 is discharged to zero. Since $i_{Lr1}(t_4)$+$i_{Lr2}(t_4)$>0, the anti-parallel diode of S_3 is conducting. S_3 can be turned on under ZVS due to the help of the *LLC* converter. In this mode, D_a, D_{r2} and D_{r4} are on, v_{ab}=-$V_{in}/2$, v_{ac}=0, and v_r=v_{Cc}. The output inductor voltage v_{Lo}=v_{Cc}-V_{o1}<0 and i_{Lo} decreases. The primary inductor voltage v_{Lr1}=n_1v_{Cc}-$V_{in}/2$<0 so that i_{Lr1} decreases with a slope of (n_1v_{Cc}-$V_{in}/2$)/L_{r1} until i_a=i_{Lo}. In the *LLC* converter, C_r and L_{r2} are resonant with the input voltage v_{ac}=0, and i_{Lr2} decreases in this mode. During this time interval, i_a increases from zero to i_{Lo}, and i_{Cc} increases from -i_{Lo} to zero. The time interval in this mode is given as:

$$\Delta t_{45}=t_5-t_4\approx\frac{L_{r1}I_{Lo}}{n_1V_{in}/2-n_1^2v_{Cc}} \tag{4}$$

In this mode, the three-level converter and the *LLC* converter transfer energy from the input to the output load. The ac terminal voltage v_{ab}=-$V_{in}/2$ and diode D_a conducts to obtain the rectified voltages v_r=v_{Cc}. The duty loss in mode 5 is given as:



(a)



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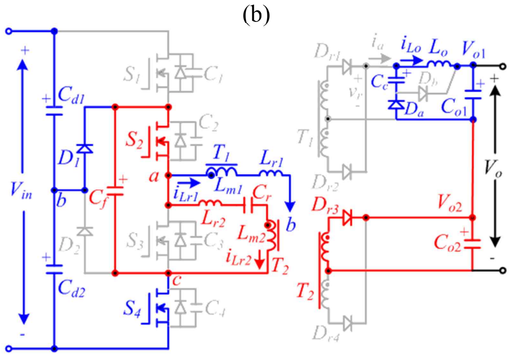

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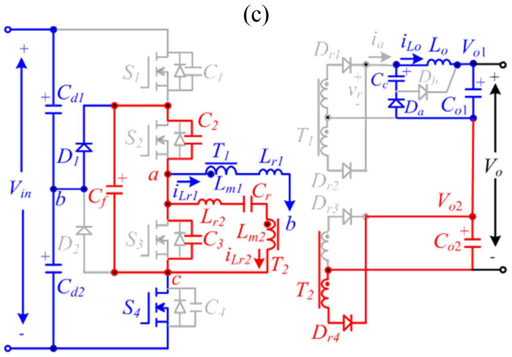
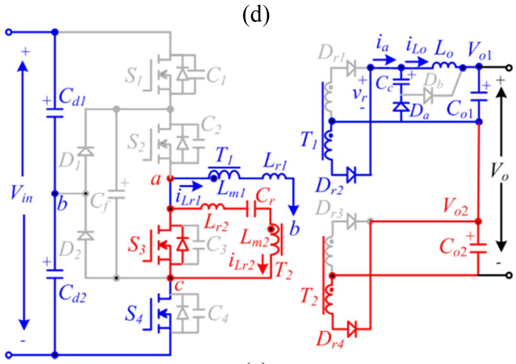


(d)



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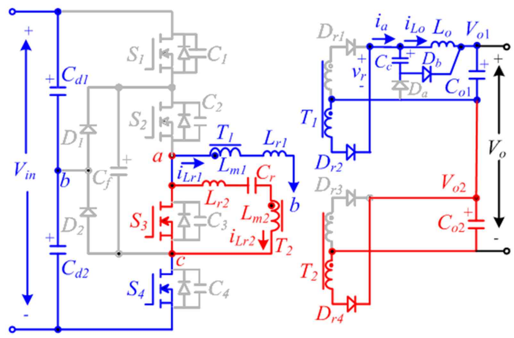
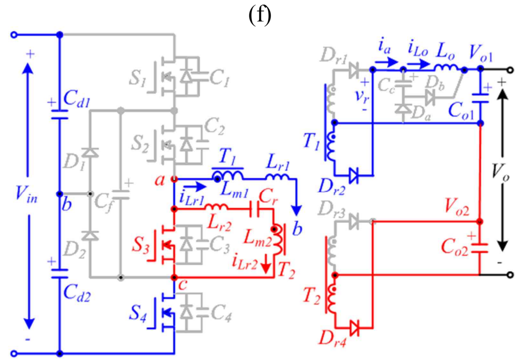


(f)



(g)

Fig. 4. Operation modes of the proposed converter in a half switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6. (g) Mode 7.

$$\delta_5 = \Delta t_{45} / T_s \approx \frac{L_{r1} I_{Lo} f_{sw}}{n_1 V_{in} / 2 - n_1^2 v_{Cc}} \tag{5}$$

Mode 6 [t_5 - t_6]: Mode 6 starts at t_5 when i_a=i_{Lo} and i_{Cc}=0. Diode D_a is off. The reflected primary inductance $L_{r1}/(n_1)^2$ and C_c are resonant with the resonant frequency $f_R = n_1 / (2\pi\sqrt{L_{r1}C_c})$. Thus, the diode D_b is conducting in this mode. The output inductor current i_{Lo} increases with a slope of v_{Cc}/L_o. The half of a resonant period, $1/(2f_R)$, is designed to be less than the minimum effective duty cycle time ($\delta_{eff,min}T_{sw}/2$). Then, the capacitor current i_{Cc} will be decreased to zero before S_4 is turned off. The rectified voltage v_r=v_{Cc}+V_{o1}, and the primary inductor current i_{Lr1}=-(i_{Lo}+i_{Cc})/n_1. In this mode, energy is transferred from the input voltage to the output load through both the three-level converter and the *LLC* circuit.

Mode 7 [t_6 - t_7]: Mode 7 starts at t_6 when i_{Cc}=0, and diode D_b is off. The rectified voltage $v_r \approx V_{in}/(2n_1) > v_{Cc}$, and D_a is reverse biased. The output inductor voltage v_{Lo}=$V_{in}/(2n_1)$-V_{o1}>0, and i_{Lo} increases in this mode. This mode ends at t_7 when S_4 is turned off. Then, the circuit operations of the proposed converter in the first half of a switching period are completed.

IV. CONVERTER PERFORMANCE ANALYSIS

There are two circuits, a three-level PWM circuit and an *LLC* circuit, in the proposed converter. The three-level converter transfers energy from the input voltage V_{in} to the output V_{o1} in modes 5-7 during the first half of the switching cycle. The *LLC* converter transfers energy from the capacitor C_f to the output V_{o2} within a full switching period. Since the *LLC* converter is operated as an unregulated dc-dc converter with a switching frequency f_{sw} that is close to the series resonant frequency f_r, the lagging-leg switches S_2 and S_3 are easily turned on at ZVS from zero to full load, and the circulating current of the *LLC* converter is at its minimum due to $f_{sw} \approx f_r$. Based on the fundamental frequency analysis of the *LLC* converter, the ac voltage gain of the *LLC* converter at the switching frequency is equal to unity. Thus, the designed dc voltage gain of the *LLC* circuit is equal to the ac voltage gain of the *LLC* circuit at the series resonant frequency, i.e. $M_{dc,LLC}=4n_2V_{o2}/V_{in}=1$. The unregulated output voltage V_{o2} of the *LLC* converter is obtained as:

$$V_{o2} = V_{in}/(4n_2) \tag{6}$$

The ZVS condition of the leading-leg switches S_1 and S_4 is achieved by the primary inductance L_{r1} and output inductance L_o given in (1). The other ZVS condition of S_1 and S_4 is that the dead time between S_1 and S_4 must be greater than Δt_{01} given in (2). The charge and discharge times of S_1-S_4 are much less than the time intervals in the other modes, and only modes 2, 3, 5, 6 and 7 are considered in the following analysis. In mode 6, the average capacitor voltage $V_{Cc}=V_{in}/(2n_1)-V_{o1}$. The flux balance condition on the output inductance L_o is given as:

$$\begin{aligned}&(\delta-\delta_5-\delta_6)(V_{in}/(2n_1)-V_{o1})+\delta_6 V_{Cc}\\&=(0.5-\delta+\delta_5)(V_o-V_{Cc})\end{aligned} \tag{7}$$

where δ_6 is the duty cycle in mode 6. Substitute $V_{Cc}=V_{in}/(2n_1)-V_{o1}$ into (7). Then, the output voltage V_{o1} of the three-level converter is obtained as:

$$V_{o1} = \frac{V_{in}}{4n_1(1-\delta+\delta_5)} = \frac{V_{in}}{4n_1(1-\delta_{eff})} \tag{8}$$

where the effective duty cycle $\delta_{eff}=\delta-\delta_5$, and δ is the duty ratio of the proposed converter when (S_1 and S_2) or (S_3 and S_4) are in the on-state. The output voltages of the three-level converter and the *LLC* converter are connected in series so that the output voltage V_o of the proposed converter is expressed as:

$$V_o = V_{o1}+V_{o2} = \frac{V_{in}}{4n_1(1-\delta_{eff})}+\frac{V_{in}}{4n_2} \tag{9}$$

The dc voltage conversion ratio of the proposed converter is obtained as:

$$M_{dc} = V_o/V_{in} = \frac{n_2+(1-\delta_{eff})n_1}{4n_1n_2(1-\delta_{eff})} \tag{10}$$

The ripple current of the output inductor L_o is approximated as:

$$\begin{aligned}\Delta i_{Lo} &= (V_{o1}-V_{Cc})(0.5-\delta_{eff})T_{sw}/L_o\\&\approx(2V_{o1}-\frac{V_{in}}{2n_1})(0.5-\delta_{eff})T_{sw}/L_o\end{aligned} \tag{11}$$

From (11), the output inductance L$_o$ is obtained in (12).

$$L_o \geq (2V_{o1}-\frac{V_{in}}{2n_1})(0.5-\delta_{eff})T_{sw}/\Delta i_{Lo} \tag{12}$$

The ripple currents, the maximum currents and the minimum currents of the magnetizing inductances L_{m1} and L_{m2} are obtained as:

$$\Delta i_{Lm1} \approx V_{in}\delta_{eff}T_{sw}/(2L_{m1})\,,\ \ \Delta i_{Lm2} \approx V_{in}T_{sw}/(8L_{m2}) \tag{13}$$

$$i_{Lm1,\max}V_{in}\delta_{eff}T_{sw}/(4L_{m1})\,,\ \ i_{Lm1,\min} = -V_{in}\delta_{eff}T_{sw}/(4L_{m1}) \tag{14}$$

$$i_{Lm2,\max} = V_{in}T_{sw}/(16L_{m3})\,,\ \ i_{Lm2,\min} = -V_{in}T_{sw}/(16L_{m3}) \tag{15}$$

The average diode currents of D_1-D_4 D_b are shown in (16) and (17).

$$i_{D1,\mathrm{av}} = i_{D2,av} \approx \delta I_o \tag{16}$$

$$i_{D3,\mathrm{av}} = i_{D4,av} \approx (0.5-\delta)I_o \tag{17}$$

The voltage stresses of D_1-D_4, D_a and D_b are given as:

$$v_{D1,\mathrm{stress}} = v_{D2,\mathrm{stress}} \approx V_{in}/n_1 \tag{18}$$

$$v_{D3,\mathrm{stress}} = v_{D4,\mathrm{stress}} \approx 2V_{o2} = V_{in}/(2n_2) \tag{19}$$

$$v_{Da,\mathrm{stress}} = v_{Db,\mathrm{stress}} \approx V_{o1} = \frac{V_{in}}{4n_1(1-\delta_{eff})} \tag{20}$$

V. EXPERIMENTAL RESULTS

First, the design procedure of the proposed converter is shown in this section to derive the main circuit components in a laboratory prototype. The electric specifications of the prototype circuit are V_{in}=750V-800V, V_o=48V and $I_{o,rated}$=30A. The switching frequency f_{sw}=100*k*Hz. The output voltage of the *LLC* converter is assumed as 20V. The selected series resonant frequency of the *LLC* converter is equal to the switching frequency f_{sw}. The DC gain of the *LLC* converter at f_r is equal to unity. Based on (6), the turns ratio of T_2 is obtained in (21).

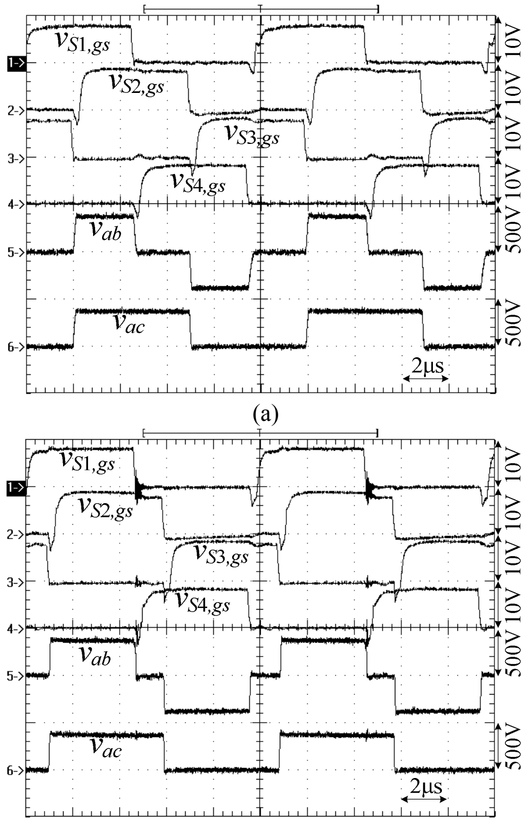
$$n_2 = V_{in,\max}/(4V_{o2}) = 800/(4\times 20) = 10 \tag{21}$$

The primary inductance, primary winding turns and secondary winding turns of T_2 are 480μH, 30 turns and 3 turns, respectively. In the *LLC* converter, the series resonant inductance L_{r2}=80μH and the series resonant capacitance C_r =32nF. The series resonant frequency of the *LLC* converter is close to 100*k*Hz. The maximum effective duty cycle δ_{eff} is assumed to be 0.4. From (9), the turns ratio of T_1 is derived in (22).

$$n_1 = \frac{V_{in,\min}}{4(1-\delta_{eff})(V_o-\frac{V_{in,\min}}{4n_2})} = 10.68 \tag{22}$$

The magnetizing inductance, primary winding turns and secondary winding turns of T_1 are 1.3mH, 64 turns and 6 turns, respectively. The assumed duty cycle loss in mode 5 is 0.01. The necessary primary inductance L_{r1} can be obtained from (5) and is given in (23).

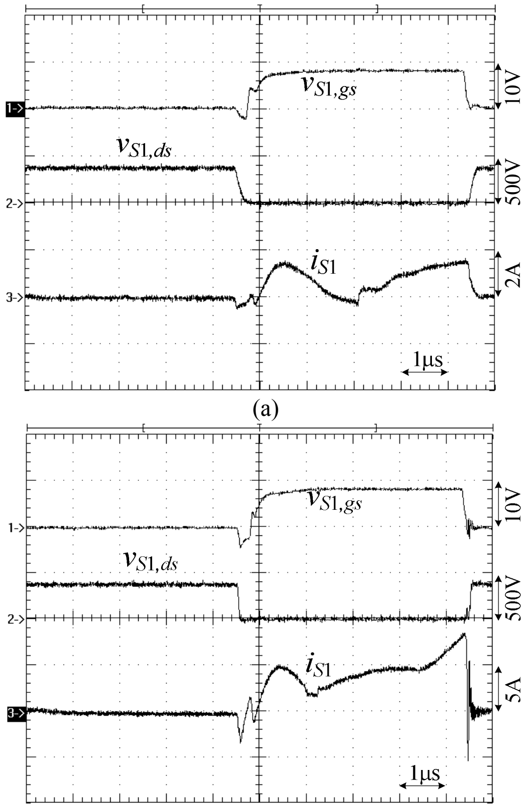
$$L_{r1} = \frac{\delta_5(n_1V_{in,\min}/2-n_1^2v_{Cc})}{I_{Lo,rated}\,f_{sw}} \approx 10.6\mu\mathrm{H} \tag{23}$$



(a)

(b)

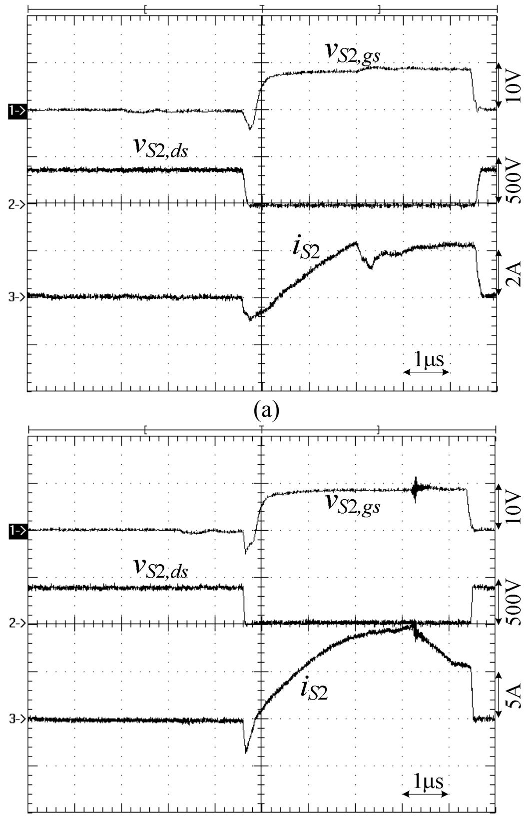
Fig. 5. Measured PWM signals of S_1-S_4 and ac side voltages v_{ab} and v_{ac} at (a) 25% load. (b) 100% load.



(a)

(b)

Fig. 6. Measured voltage and current of S_1 (leading-leg switch) at (a) 15% load (b) 100% load.



(a)

(b)

Fig. 7. Measured voltage and current of S_2 (lagging-leg switch) at (a) 15% load (b) 100% load.

The selected primary inductance L_{r1} is 10μH in the prototype circuit. From (12), the output inductance L_o is obtained in (24) with $\Delta i_{Lo}/I_{o,rated}$=0.2.

$$L_o \geq (2V_{o1} - \frac{V_{in,\min}}{2n_1})(0.5-\delta_{eff})T_{sw}/\Delta i_{Lo} = 3.5\mu H \quad (26)$$

In the prototype circuit, the adopted output inductance L_o is 5μH. Power MOSFETs (IRFP460) with V_{DS}=500V and $I_{D,rms}$=20A are used for the switches S_1-S_4. Fast recovery diodes (VF30200C) with V_{RRM}=200V and I_F=30A are used as the rectifier diodes D_1-D_6, D_a and D_b. The selected clamped diodes D_1 and D_2 are MUR860. The selected input split capacitances are C_{d1}=C_{d2}=360μF/450V, the flying capacitance C_f=1μF and the output capacitances are C_{o1}=C_{o2}=2200μF.

Experimental results based on a laboratory prototype with the above circuit parameters are presented to verify the circuit performance. Fig. 5 gives the measured PWM signals of S_1-S_4 and the ac side voltages v_{ab} and v_{ac} at 25% and 100% loads. It can be seen that there are three voltage levels on v_{ab} and two voltage levels on v_{ac}. The measured voltage and current of S_1 (leading-leg switch) at 15% and 100% loads are illustrated in Fig. 6. Fig. 7 gives the measured voltage and current of S_2 (lagging-leg switch) at 15% and 100% loads. From Figs. 6 and 7, S_1 and S_2 are all turned on at ZVS at a 15% load. (S_1, S_4) and (S_2, S_3) are in the leading-leg and lagging-leg,

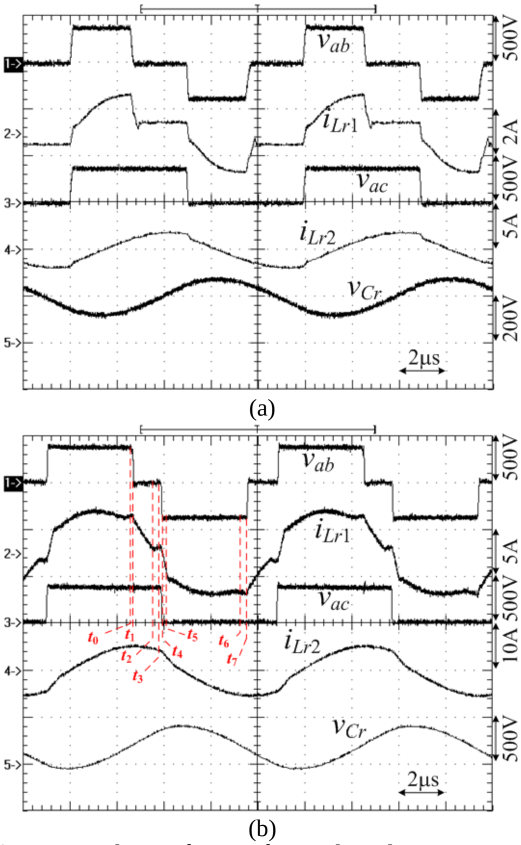


Fig. 8. Measured waveforms of ac side voltages v_{ab} and v_{ac}, resonant capacitor voltage v_{Cr}, and the primary currents i_{Lr1} and i_{Lr2} at (a) 25% load (b) 100% load.

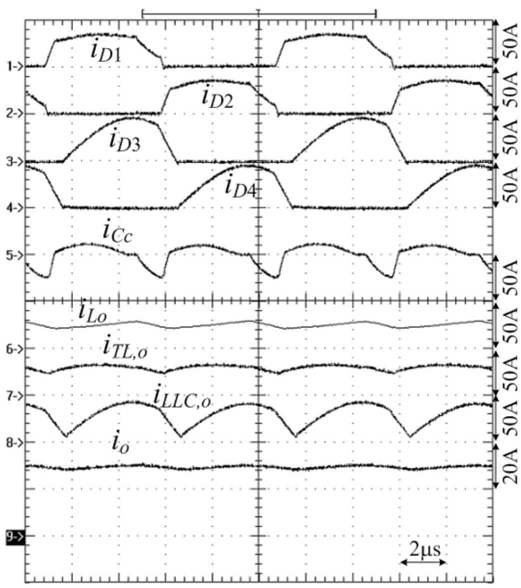


Fig. 9. Measured waveforms of diode currents i_{D1}-i_{D4}, clamped capacitor current i_{Cc}, output inductor current i_{Lo}, three-level converter output current $i_{TL,o}$, *LLC* converter output current $i_{LLC,o}$ and load current I_o at full load.

respectively. Thus, S_1-S_4 are all turned on at ZVS from 15% to full load conditions. Fig. 8 shows the test results of the ac side voltages v_{ab} and v_{ac}, the resonant capacitor voltage v_{Cr}, and the primary currents i_{Lr1} and i_{Lr2} at 25% and 100% loads. There is no circulating current on i_{Lr1} in the freewheeling interval (v_{ab}=0), and the primary current i_{Lr2} is a quasi-sinusoidal current. From the measured primary inductor current i_{Lr1} in Fig. 8(b), it is clear than there are seven operation modes in the first half switching cycle and these measured waveforms verify the operation mode discussions in section III. Fig. 9 illustrates the experimental results of the diode currents i_{D1}-i_{D4}, clamped capacitor current i_{Cc}, output inductor current i_{Lo}, three-level converter output current $i_{TL,o}$=i_{Lo}+i_{Db}, *LLC* converter output current $i_{LLC,o}$ and load current I_o at full load. The measured circuit efficiencies of the proposed converter are 94.5%, 95.3% and 93.2% at a 25% load, a 50% load and a 100% load, respectively. The measured maximum efficiency is 95.9% at an 80% load.

VI. Conclusion

A hybrid ZVS converter is presented in this paper to reduce the circulating current loss in the freewheeling interval and to extend the ZVS range of the lagging-leg switches. The proposed hybrid converter includes a conventional three-level converter and a *LLC* converter with shared lagging-leg switches. The switching frequency of the *LLC* converter is close to the series resonant frequency to reduce the circulating current at the primary side and to help the lagging-leg switches turn on at ZVS from light load to full load conditions. A passive snubber is used on the secondary side of the three-level converter to reduce the circulating current during the freewheeling interval due to the fact that a reflected rectifier voltage is applied to the leakage inductance. The outputs of the two converters are connected in series to transfer energy from the input to the output load within the whole switching cycle. When compared to the conventional three-level PWM converter, the proposed hybrid converter has less circulating current losses and a wider range of ZVS operation. Finally, the effectiveness and performance of the proposed converter are verified by experimental results with a 1.44*k*W prototype circuit.

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References

[1] I.-H. Cho, K.-M. Cho, J.-W. Kim, and G.-W. Moon, “A new phase-shifted full-bridge converter with maximum duty operation for server power system,” *IEEE Trans. Power Electron.*, Vol. 26, No. 12, pp. 3491-3500, Dec. 2011.

[2] H. Kato, H. Matsuo, T. Ito, S. Kawazu, D. Kawahara, S. Motomura, and R. Hamaguchie, “Power efficiency improvement of the full ridge current resonant dc-dc converter,” in *Proc. of IEEE INTELEC Conf.*, pp. 1-5, 2011.

[3] D. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, “An automotive on-board 3.3kW battery charger for PHEV applications,” in *Proc. of IEEE VPP Conf.*, pp. 1-6, 2011.

[4] T. Mishima, K. Akamatsu, and M. Nakaoka, “A high frequency-link secondary-side phase-shifted full-bridge soft-switching PWM DC-DC converter with ZCS active rectifier for EV battery chargerd,” *IEEE Trans. Power Electron.*, Vol. 28, No. 12, pp. 5758-5773, Dec. 2013.

[5] S.-K. Han, G.-W. Moon and M.-J. Youn, “A voltage-balanced phase-shifted three-level DC/DC converter operating from high-input voltage,” *IEEE Power Electron. Letters*, Vol. 1, No. 3, pp. 74-77, Sep. 2003.

[6] F. Canales, P. Barbosa, and F. C. Lee, “A zero-voltage and zero-current switching three-level DC/DC converter,” *IEEE Trans. Power Electron.*, Vol. 17, No. 6, pp. 898-904, Nov. 2002.

[7] J. P. Rodrigues, S. A. Mussa, I. Barbi, and A. J. Perin, “Three-level zero-voltage switching pulse-width modulation DC-DC boost converter with active clamping,” *IET Proc. Power Electron.*, Vol. 3, No. 3, pp. 345-354, 2010.

[8] J. A. Sabate, V. Vlatkovic, R. B. Ridlry, F. C. Lee, and B. H. Cho, “Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter,” in *Proc. of IEEE-APEC Conf.*, pp. 275-284, 1990.

[9] Y. Jang, M. M. Jovanovic, and Y. M. Chang, “A new ZVS-PWM full-bridge converter,” *IEEE Trans. Power Electron.*, Vol. 18, No. 5, pp. 1122-1129, Sep. 2003.

[10] X. Wu, J. Zhang, X. Xie, and Z. Qian, “Analysis and optimal design considerations for an improved full-bridge ZVS dc-dc converter with high efficiency,” *IEEE Trans. Power Electron.*, Vol. 21, No. 5, pp.1225-1233, Sep. 2006.

[11] W. Yu, J. S. Lai, W.-H. Lai, an H. Wan, “Hybrid resonant and PWM converter with high efficiency and full soft-switching range,” *IEEE Trans. Power Electron.*, Vol. 27, No. 12, pp. 4925-4233, Dec. 2012.

[12] Y. Chen and Y. Kang, “An improved full-bridge dual-output dc-dc converter based on the extended complementary pulse width modulation concept,” *IEEE Trans. Power Electron.*, Vol. 26, No. 11, pp. 3215-3229, Nov. 2011.

[13] L. H. Mweene, C. A. Wright, and M. F. Schlecht, “A 1kw 500kHz front-end converter for a distributed power supply system,” *IEEE Trans. Power Electron.*, Vol. 6, No. 3, pp. 398-407, Jul. 1991.

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