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An FPGA-based Fully Digital Controller for Boost PFC Converter

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Abstract

This paper introduces a novel digital one cycle control (DOCC) boost power factor correction (PFC) converter. The proposed PFC converter realizes the FPGA-based DOCC control approach for single-phase PFC rectifiers without input voltage sensing or a complicated two-loop compensation design. It can also achieve a high power factor and the operation of low harmonic input current ingredients over universal loads in continuous conduction mode. The trailing triangle modulation adopted in this approach makes the acquisition of the average input current an easy process. The controller implementation is based on a boost topology power circuit with low speed, low-resolution A/D converters, and economical FPGA development board. Experimental results demonstrate that the proposed PFC rectifier can obtain a PF value of up to 0.999 and a minimum THD of at least 1.9% using a 120 W prototype.

Key words: Continuous Current Mode, Digital Control, Power Factor Correction

I. INTRODUCTION

Using a single-phase power factor correction (PFC) boost rectifier to improve the power factor and energy quality of an electric system is necessary according to international energy standards, such as IEC1000-3-2 [1] and IEEE-519 [2]. Boost PFC converter is the most popular among many topologies because of its simplicity and significant dynamics performance [3]. Numerous research results on the boost PFC control approach have been presented. The most widely adopted control method for boost PFC converters is the average current mode [4], [5]. Despite its many advantages, such as low harmonics input current and insensitivity to noise, the inherent drawbacks of the boost PFC converter are the complicated two-loop control and three independent voltages or currents to be measured in some applications. The one-cycle control (OCC) of boost PFC converters is proposed in [6], which introduces the nonlinear control approach with a simple structure and low cost. The benefit of nonlinear control lies in eliminating the need to sense the input voltage and in using a simple integrator to replace the complicated multiplier in the average current mode control approach. The OCC approach is widely implemented in some commercial boost PFC control microchips or solutions [7], [8]. Different modifications [9]-[11] have been reported based on the OCC method. However, applications of the conventional OCC are limited mostly to the analog field. Digital implementation boost PFC converters have attracted increasing attention in recent years. Various presented converters are based on the digital realization, modification, and extension of the average current control approach [12]-[19]. Given that the most widely reported control approach of digital PFC converters is implemented on DSP or microcontrollers, the digital realization of the average current mode control approach based on FPGA is presented in [20]. Other control methods are presented in [20]-[23]. A novel detection mechanism is proposed in [23] based on the DSP implementation for mixed conduction mode (MCM) digital controllers. A simple digital control scheme is also proposed in [23] to obtain the accurate average current in discontinuous conduction mode (DCM). Other control approaches include the precalculated duty cycle control presented in [20], [21].

As previously presented, several digital OCC approaches have been reported. The most significant obstacle to implementing OCC approach is imitating the integration part in digital implementation. An accumulator is used in [22] to calculate the sum of input current samples to obtain the average input current value. This method requires fast A/D converters and adds a heavy calculation burden to the controller in every switching cycle.

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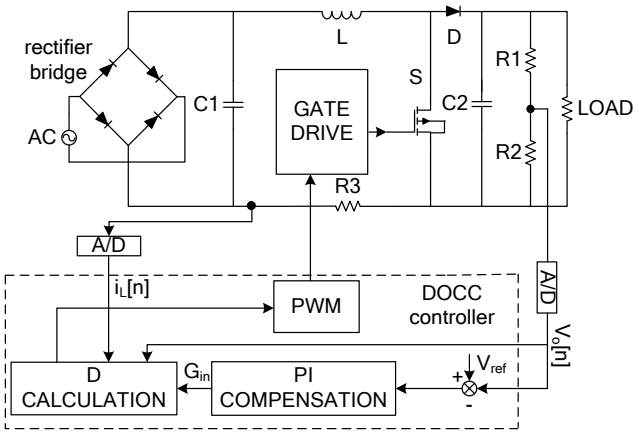


Fig. 1. Boost PFC rectifier with DOCC control.

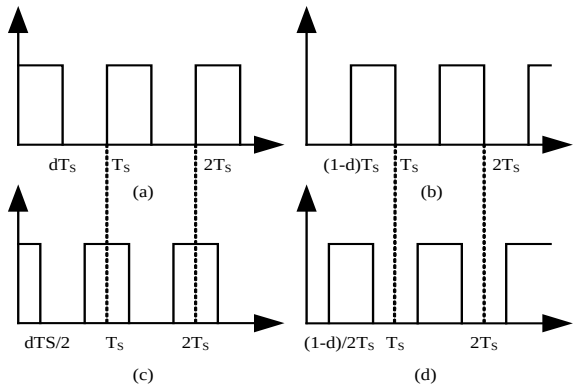


Fig. 2. Sketch map of the pulse width modulation (PWM) types. (a) Trailing edge modulation. (b) Leading edge modulation. (c) Trailing triangle modulation. (d) Leading triangle modulation.

The current paper proposes an FPGA-based digital OCC (DOCC) boost PFC operating under Continuous Current Mode (CCM) condition. This boost PFC rectifier adopts the trailing triangle modulation method to capture the average input current of every switching cycle. The compensation part of the controller is designed on a new voltage loop small signal model without an explicit current loop compensation part, but results in a high power factor and low THD level over a large load range. The rest of this paper is organized as follows. Section II introduces the principle of the DOCC approach, the input current sampling method, and the system stability analysis. Section III describes the sketchy structure of the proposed controller implemented on FPGA and the criteria of system implementation issue. Section IV presents the experimental results for a 120 W boost DOCC PFC prototype. Section V concludes this paper.

II. Analysis of the DOCC Approach

The basic objective of a PFC rectifier is to ensure that the input current is synchronized with the grid voltage (with the same frequency and phase), as shown in Fig.1. This process can be written as $i_L = v_{in} G_{in}$, where i_L is the average inductor current in one switching cycle, v_{in} is the rectified grid voltage, and G_{in} is the emulated input admittance. Using the quasi-state approximation in the CCM boost PFC operation and assuming v_{in} and v_o are constant values in one switching cycle T_s, we obtain $v_o(1-d) = v_{in}$, where d is the switching duty ratio and v_o is the output voltage. The objective of the PFC controller can be expressed as follows:

$$i_L = G_{in} v_{in} = G_{in} v_o (1-d) \quad (1)$$

Eq. (1) indicates that the duty ratio should be applied to the switching converter in every duty cycle. Given that v_{in} is expressed in terms of v_o and d, sensing the input voltage is unnecessary. v_o is sampled by a low-cost A/D converter. G_{in} is computed by the compensation part of the voltage loop, which will be analyzed in a detailed derivation in the following sections. The most tricky problem is the acquisition of the average current of the duty cycle. Four basic current sample methods (i.e., trailing edge mode, leading edge mode, trailing triangle mode, and leading triangle mode) are used in a switching power system, as shown in Fig. 2. Triangle modulation is adopted in the DOCC current sampling operation method because trailing edge modulation or leading edge modulation is unsuitable in average current acquisition. Given that the rectifier can enter the DCM mode, the current at the $T_s/2$ instant can be difficult to track and sample. Hence, the trailing triangle modulation is utilized for the prototype design in this paper.

Fig. 2 shows that the power switch is always turned on at the beginning of every switching cycle, but is turned off at the $dT_s/2$ instant. The switch is not turned on until the $(1\text{-}d/2)T_s$ instant. The sample current $i_L[n\text{-}1]$ at an instant is the average current of the $(n\text{-}1)th$ switching cycle. The quasi-state approximation shows that the switching frequency is much faster than the input current frequency. Thus, we can take the sample average current $i_L[n\text{-}1]$ at an instant as the average current criterion $i_L[n]$ in the *nth* switching cycle by assuming two consecutive switching cycles with the same average current. This approximation can provide significant convenience in control analysis and system implementation.

Adopting the trailing triangle modulation for average current $i_L[n]$ acquisition has the following primary merits. 1) The average current of the switching cycle is obtained through a relatively simple method without the need for an accumulator [22]. This condition can save on hardware consumption in FPGA implementation. The current sampled at a fixed instant on the switching frequency makes the utilization of low-cost and low-speed A/D converters possible. It also makes the design of sampling circuit easy. 2) The average current criterion is acquired at the beginning of the switching cycle. This approach leaves sufficient time to calculate the appropriate duty ratio for the switching cycle online.

Assuming that the input current is higher than the criterion

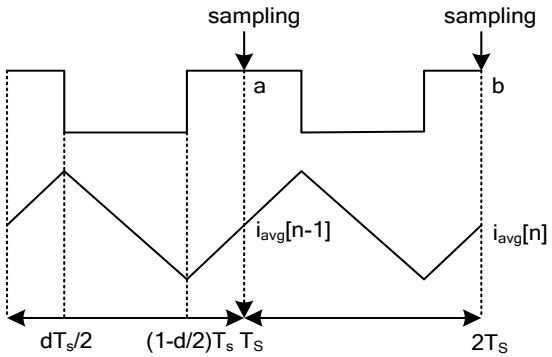


Fig. 3. Input current sample operation with trailing triangle modulation.

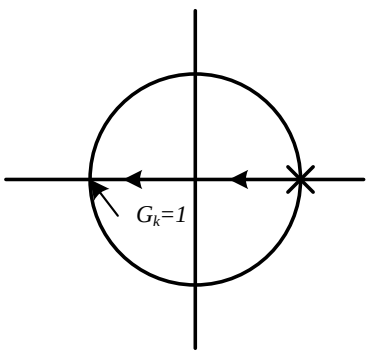


Fig. 4. Root locus plot of $T_i(z)$ for implementation on the proposed DOCC PFC controller.

value by some disturbance or other interference, the acquired average current is also higher. The duty ratio of the following switching cycle is lower than the normal level to correct the input current to the normal level based on Eq. (1). When the input current is lower than the normal level, the opposite process is implemented to correct it. This mechanism guarantees that the fluctuation of input current does not influence the system stability.

The small signal stability of control law (Eq. 1) can be analyzed based on the quasi-state approximation from another perspective. The current loop compensation transfer function is expressed in the discrete domain as follows:

$$G_{ic}(z)=\frac{\hat{d}(z)}{\hat{i}_L(z)}=-\frac{1}{G_{in}v_o} \tag{2}$$

In one switching cycle

$$i_L[n+1]=i_L[n]+\frac{v_{in}}{L}dT_s-\frac{v_o-v_{in}}{L}(1-d)T_s \tag{3}$$

The linearization of Eq. (3) yields the duty ratio to current transfer function as follows:

$$G_{id}=\frac{\hat{i}_L(z)}{\hat{d}(z)}=\frac{v_oT_s}{z-1} \tag{4}$$

The discrete time current open loop transfer function is obtained in Eq. (5) by combining Eq. (2), Eq. (4), and the input

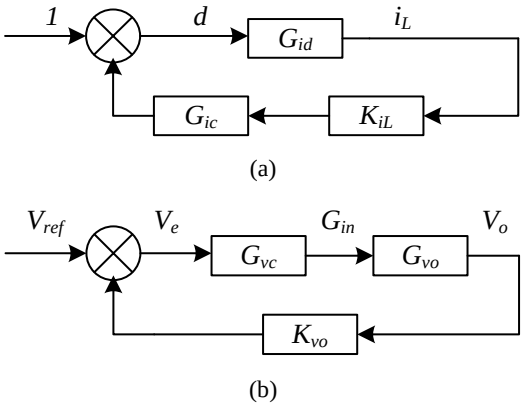


Fig. 5. Sketch maps. (a) Current-loop structure. (b) Voltage-loop structure.

current sampling coefficient K_{iL}. The sketch map of the current loop is shown in Fig. 5(a).

$$T_i(z)=-K_{iL}G_{id}(z)G_{ic}(z)=\frac{K_{iL}T_s}{G_{in}L(z-1)} \tag{5}$$

The root locus technique in Fig. 4 shows that the current loop is stable when the parameter $G_k = K_{iL}T_s/G_{in}L < 1$, whereas the condition that guarantees the boost PFC converter that operates in CCM is $G_c = T_s/G_{in}L < 1$ [24]. Fig. 6 illustrates the CCM, DCM, and MCM current operating modes for boost PFC converters. We can conclude that the current loop of the DOCC boost PFC rectifier is always stable without any explicit compensation part when it always operates in the CCM condition [24]. The current rectifier loop is still possibly stable ($G_k < 1$) because the current sampling gain K_{iL} is generally less than 1 when the DOCC boost PFC operates in MCM or DCM ($G_c > 1$).

The emulated input admittance G_{in} can be obtained through an analysis of the system voltage loop, as shown in Fig. 5(b). Although most analyses of the nonlinear-control boost PFC is based on the small signal introduced in [24], the current study simplifies the analysis by assuming that the power system efficiency closely approximates 1. Thus,

$$V_{inrms}I_{inrms}=v_oi_o=P \tag{6}$$

The V_{inrms} in Eq. (5) represents the root mean square (RMS) value of input voltage v_{in}, I_{inrms} represents the RMS value of the input current, and i_o denotes the output current of the system. Fig. 6 can be expressed as follows:

$$I_{inrms}=\frac{I_{inref}}{K_{iL}}=\frac{K_{vo}V_{inrms}G_{in}}{K_{iL}} \tag{7}$$

I_{inref} denotes the RMS value of the input reference current, and K_{vo} is the output voltage sampling coefficient. Combining Eqs. (6) and (7) results in the following:

$$\frac{K_{vo}V_{inrms}^2}{K_{iL}}G_{in}=v_oi_o \tag{8}$$

The following equation is obtained when the disturbance to Eq. (8) is added:

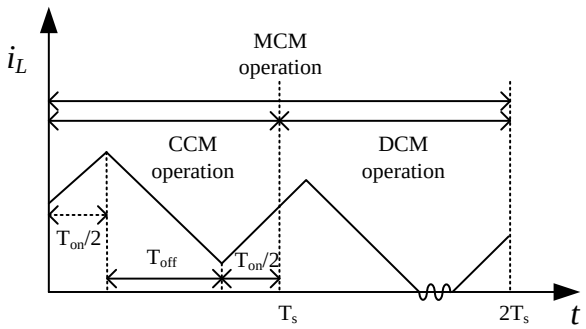


Fig. 6. Illustration of the PFC operating in CCM, DCM, and MCM.

$$\frac{K_{vo}V_{inrms}^2}{K_{iL}}(G_{in}+\hat{g}_{in})=(V_o+\hat{v}_o)(I_o+\hat{i}_o) \tag{9}$$

We then obtain the following after the small signal analysis of Eq. (9):

$$\hat{i}_o=\frac{K_{vo}V_{inrms}^2}{K_{iL}V_o}\hat{g}_{in}-\frac{I_o}{V_o}\hat{v}_o \tag{10}$$

The output current can be expressed as follows:

$$i_o=C\frac{dv_o}{dt}+\frac{P}{v_o} \tag{11}$$

The small signal expression of Eq. (10) is as follows:

$$\hat{i}_o=C\frac{d\hat{v}_o}{dt}-\frac{I_o}{V_o}\hat{v}_o \tag{12}$$

Combining Eqs. (10) and (12), the small signal relationship between v_o and G_{in}, after the discretization of the transfer function by the zero-order hold method is obtained in Eq. (13), where T_{ss} represents the sampling time of the discretization process.

$$G_{vo}(z)=\frac{\hat{v}_o(z)}{\hat{g}_{in}(z)}=\frac{K_{vo}V_{inrms}^2T_{ss}}{K_{iL}CV_o(z-1)} \tag{13}$$

Designing a stable feedback voltage loop is necessary to respond to the load variation, parameter offset of power devices, and input voltage V_{inrms} fluctuation. A tradeoff exists between the output voltage dynamics performance and limited loop bandwidth in this part. The proportion-integration compensation part G_{vc} is used in this study to set the crossover frequency of the voltage loop at approximately 20 Hz (with a 60° phase margin) to suppress the second harmonics of the output voltage while guaranteeing the required voltage-loop dynamics performance. The compensated voltage loop gain and phase margin are shown in Fig. 7.

III. Implementation Issues

Determining the switching frequency f_s is dependent on specific application circumstances. A high switching frequency generally means a low output voltage ripple level under the same capacitor and inductor condition. A more serious

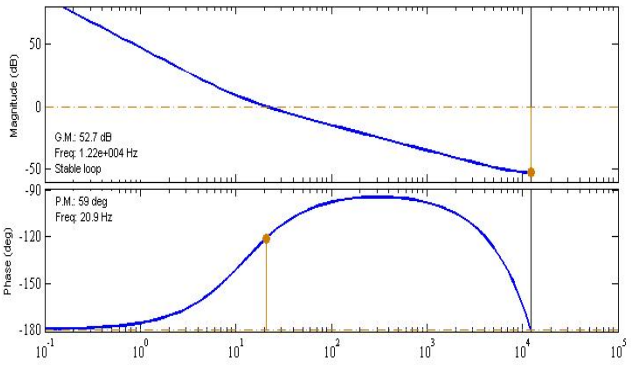


Fig. 7. Closed voltage-loop gains $T_v(z)$ with the G_{vc} compensation scheme.

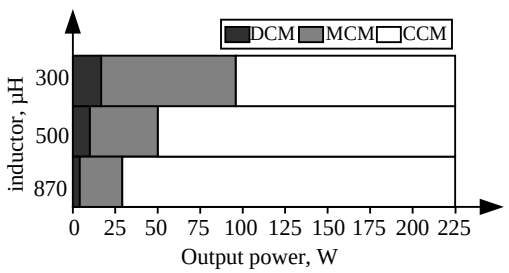


Fig. 8. Illustration of the boost PFC operating in different modes.

electromagnetic interference problem also occurs, which causes lower system efficiency. We set the switching frequency at approximately 50 kHz after the tradeoff process. The switching period being the integer multiples of the controller clock period is simpler for the design of the digital PWM (DPWM) function. Thus, we determine f_s = 48.8 kHz in this prototype implementation.

The input inductor value affects the ripple level of the input current, as well as the current operating mode of the system shown in Fig. 8. Eq. (1) shows that the entire control system is based on the assumption that the rectifier operates in the CCM mode. Eq. (14) divides the CCM and MCM regions as obtained from [24]. It determines the minimum inductor value for the CCM operation. Eq. (15) divides the DCM and MCM regions. We represent the boundaries between CCM, MCM, and DCM over load variation in Fig. 8 while maintaining the input voltage V_{inrms} (50 V), switching frequency f_s (48.8 kHz), and output voltage V_o (80 V) constant.

$$G_{in}\geq\frac{1}{2Lf_s} \tag{14}$$

$$G_{in}<\frac{(1-\frac{V_{in\max}}{V_o})}{2Lf_s} \tag{15}$$

The inductor L should satisfy the following relation to guarantee the continuous input current during the operation:

$$L\geq\frac{V_{in\max}}{2f_sI_{in\max}} \tag{16}$$

We obtain L > 420 μH with P_{max} = 128 W, V_{inmax} = 71.7 V,

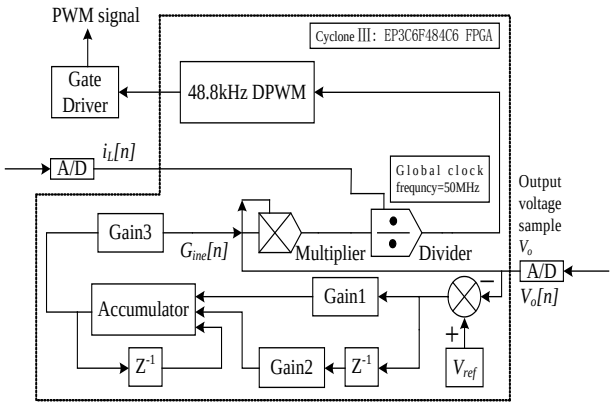


Fig. 9. Diagram of the proposed PFC controller scheme.

TABLE I
CONVERTER SPECIFICATIONS

Parameter	Value	Parameter	Value
f_s	48.8 kHz	L	500 μH
T_s	20.5 μs	*R1*	390 kΩ
V_{inrms}	50 V	*R2*	10 kΩ
V_o	80 V	*R3*	0.1 Ω
C1	0.1 μF	*Gain1*	22
C2	1000 μF	*Gain2*	899
P	120 W	*Gain3*	2×10^{-15}

I_{inmax} = 3.6 A, and f_s = 97.6 kHz. We then take L = 500 μH with a certain safety margin.

The value of the output capacitor C2 is calculated according to its hold time Δ*t*. Hold time expresses the time duration for the capacitor voltage hold in a prescribed range without any of the power source income. The said value can be expressed based on the law of conservation of energy:

$$\frac{1}{2}C(V_{o\max}^2 - V_{o\min}^2) = \Delta t \cdot P_{\max} \quad (17)$$

The output voltage ripple should generally be σ < 5%. Given that the reference output voltage is V_o = 80 V, V_{omax} = 84 V and V_{omin} = 76 V are obtained. In this study, the output capacitor value is calculated as 1000 μF when the hold time Δt is set as 5 ms.

The controller implementation based on FPGA can achieve multi-model system integration with few peripheral devices and routings. The parallel computing character of FPGA can also guarantee the real-time requirement of several complex algorithms.

Table I lists the parameters of the proposed boost PFC prototype. We only utilize the upper eight-bit digital output of the selected A/D converter LTC1412. The MSB of the digital output indicates the output value sign. Thus, the output range of LTC1412 is -2.5 V to 2.5 V, and the gain of the selected A/D converters is $K_{ad} = 2^7/2.5 \approx 51$. Fig. 1 and Table I show that the gain of the output voltage divider network that consists of R1 and R2 is K_{vo} = 0.025, and the output voltage amplification coefficient is K_{av} = 1. The equivalent coefficient

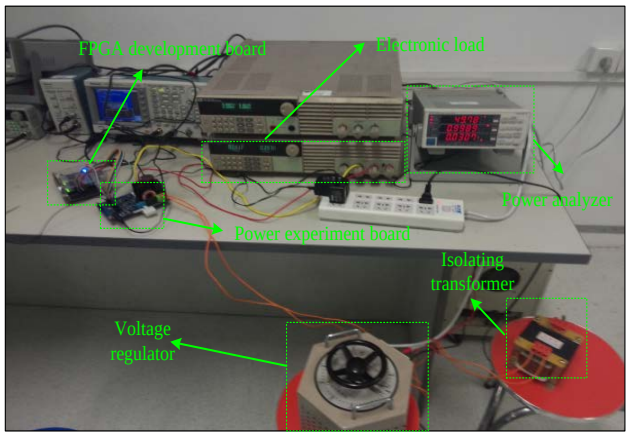


Fig. 10. Photo of the experiment set-up for the proposed boost PFC.

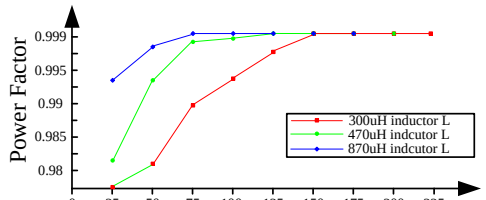
of the output voltage sampling part is $K_{voe} = K_{ad}K_{vo}K_{av}$ = 1.275. With the same principle (i.e., the sampling resistor *R3* = 0.1 Ω, input current amplification coefficient K_{ai} = 5, and gain of the sampling resistance is set at K_{iL} = 0.5), we obtain the equivalent gain of input current sampling part $K_{iLe} = K_{ad}K_{iL}K_{ai}$ = 25.5.

Fig. 10 illustrates the experiment set-up of the proposed boost PFC rectifier. An isolating transformer with a transformer ratio of 1:1 is used for safety consideration. V_{inrms} = 50 V is obtained by the voltage regulator. We use the IT8514 DC electronic load to generate the system load and load step. The PF and THD are measured by a WT210 digital power meter. The equivalent emulated input admittance $G_{ine}[n]$ is the indicator of load condition for the proposed prototype in Fig. 11. $G_{ine}[n]$ can be used to assess the load condition and judge the load variation. In this study, the value range of $G_{ine}[n]$ is approximately 500 to 800 for an optimal boost PFC performance. $G_{ine}[n]$ < 500 indicates that the PFC rectifier enters the MCM/DCM. Eq. (14) divides the CCM and MCM regions [24], whereas Eq. (15) divides the DCM and MCM regions. Fig. 11(a) shows that the PF significantly decreases because the entire control system is based on the assumption that the rectifier operates in the CCM mode. The system THD descends when $G_{ine}[n]$ < 500 because the harmonics current proportion increases as shown in Fig. 11(b). Fig. 11(c) shows the relation between emulated input admittance $G_{ine}[n]$ and output power *P* under different inductor values.

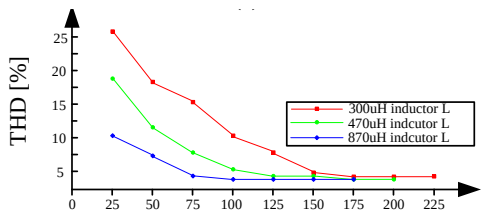
IV. EXPERIMENTAL RESULTS

Fig. 12 shows the PWM waveform (upper, ch1) and conversion signal waveform (under, ch2). The falling edge of the conversion signal waveform triggers the input current sampling process instantaneously. The input current is always sampled at a fixed instant on the switching frequency.

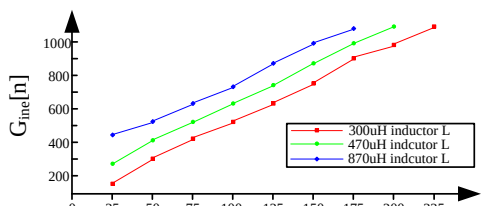
Fig. 13 shows the input voltage waveform (upper, ch2) and average input current waveform (under, ch1) after the proposed PFC that operates in a 120 W load. The average input current is



(a)



(b)



(c)

Fig. 11. Proposed digital controller performance with input inductor. (a) Power factor. (b) THD, and (c) $G_{ine}[n]$.

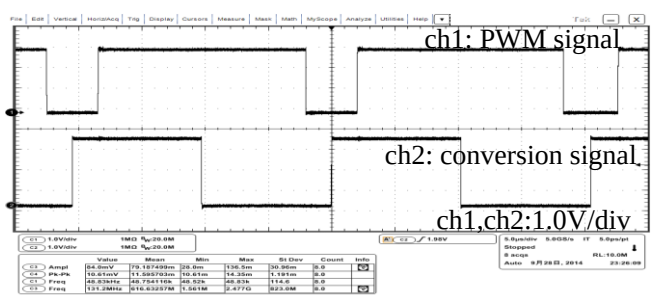


Fig. 12. DPWM and conversion signal waveform.

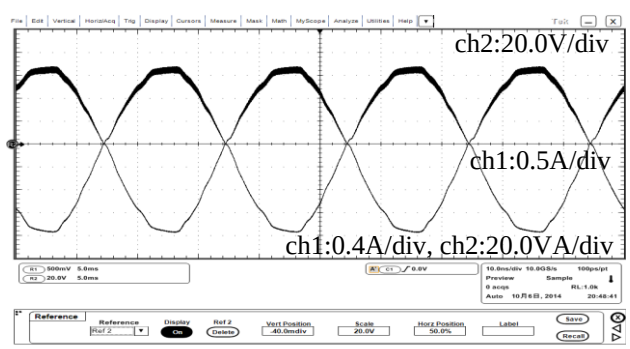


Fig. 13. Input current and voltage waveform with PFC.

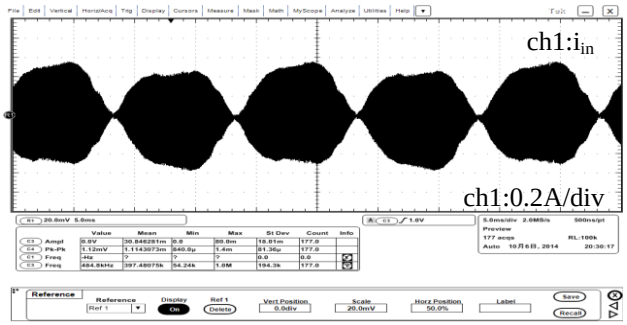


Fig. 14. Input current envelope waveform in a 120 W load.

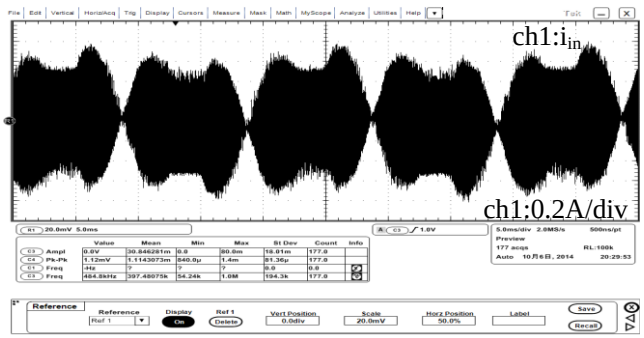


Fig. 15. Input current envelope waveform in a 40 W load.

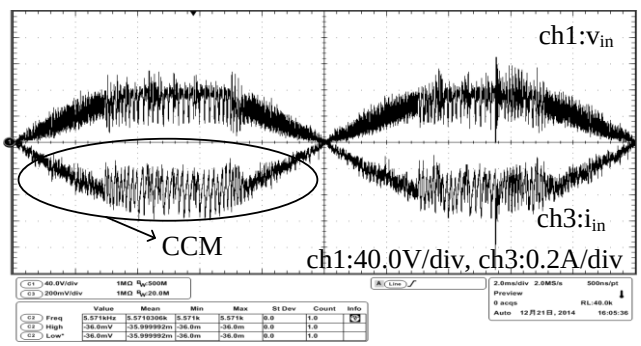


Fig. 16. Input current waveform in a 120 W load.

perfectly synchronized with the input voltage.

Fig. 14 shows the input current envelope captured by the hall current sensor at a 120 W load. Fig. 15 is the input current waveform at a 40 W load. As previously analyzed, the PFC rectifier enters the MCM/DCM mode.

Fig. 16 shows the waveform of the input current captured at sampling resistance R3 (under, ch3) and input voltage waveform (upper, ch1) at a 120 W load. The system always operates in CCM under this load level.

Fig. 17 show the waveform of the input current captured at sampling resistance R3 (under, ch3) and input voltage waveform (upper, ch1) at a 40 W load. The system operates in CCM when the input voltage is near the peak value of the rectified cycle, whereas it operates in DCM when the input voltage is near the minimum value. This scenario indicates that the system enters the MCM under this load level, which results in a high harmonics level and low PF value (Fig. 11).

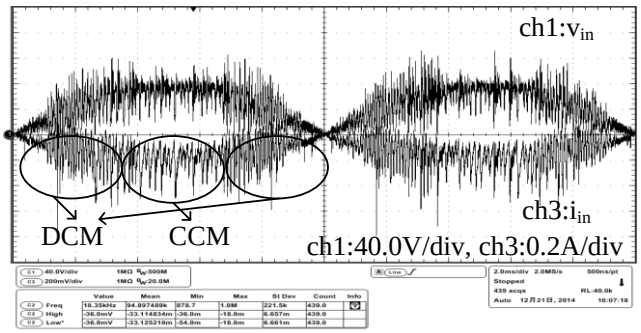


Fig. 17. Input current waveform in a 40 W load.

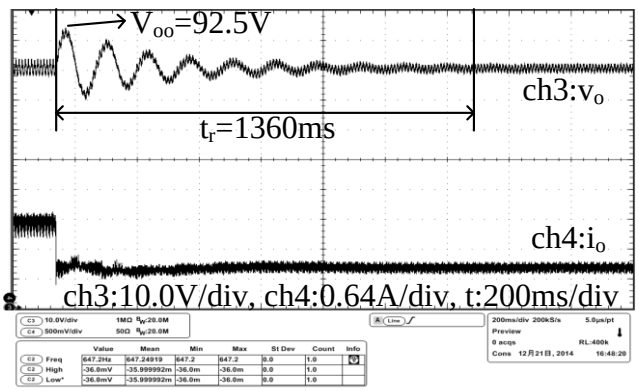


Fig. 18. Output voltage regulation from 120 W to 64 W load step.

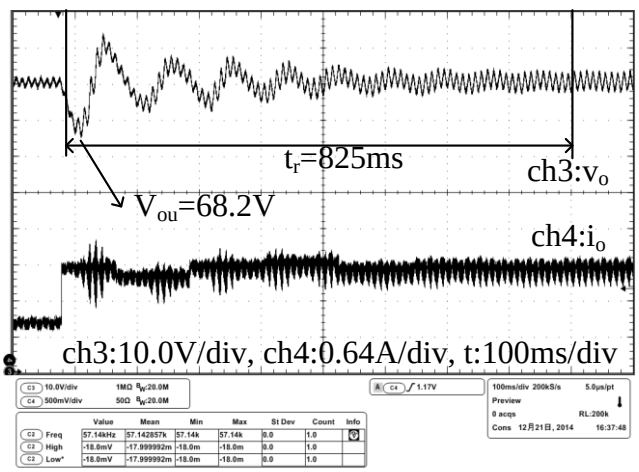


Fig. 19. Output voltage regulation from 64 W to 120 W load step.

We exhibit the output voltage v_o waveforms to verify the validity of the voltage loop. Fig. 18 shows the output voltage regulation process from 120 W to 64 W load step. The said figure shows that the maximum overshoot output voltage is V_{oo} = 92.5 V, and the system takes approximately 1360 ms to regulate the voltage to steady state (80 V). Fig. 19 shows the output voltage regulation process from the 64 W to 120 W load step, which is the reverse process of the load step in Fig. 4. The output voltage elapses by 825 ms before it recovers to 80 V, and the minimum undershoot output voltage is V_{ou} = 68.2 V. Notably, the system takes a longer regulation time to return to stability when the load step is from 120 W to 64 W compared with reverse load step process from 64 W to 120 W. This scenario is the typical phenomenon for single-ended boost topology because it has no energy release path in the load drop step process.

V. CONCLUSION

This paper presents an FPGA-based fully digital controller for boost PFC converters. The proposed PFC converter realizes the DOCC control approach, which requires no input voltage sensing, two-loop compensation part design, or complicated average current sampling and calculation process. It obtains a high power factor and the operation of low harmonic input current ingredients over a large load range under CCM. Implementation of the proposed PFC system and structure of the FPFA-based controller are discussed in detail. Experimental results demonstrate that the proposed PFC rectifier can obtain a PF value of up to 0.999, and the minimum THD decreases to 1.9% by a 120 W prototype that operates in 50 V input line voltage. The feasibility and suitable dynamics response under variable load conditions of the proposed prototype are satisfactory.

REFERENCES

[1] *Electromagnetic Compatibility Part 3: Limits—Section 2: Limits for Harmonic Currents Emissions (equipment input current_16 A per phase)*, IEC1000-3-2, 1995.

[2] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Std. 519-1992, 1992.

[3] F. Q. Wang, H. Zhang, and X. K. Ma, "Intermediate-scale instability in two-stage power-factor correction converters," *IET Power Electron.*, Vol. 3, No. 3, pp.438-448, May 2010.

[4] L. Dixon, "High power factor switching preregulator design optimization," in *Proc. Unitrode Power Supply Design Sem.*, pp. 7.1-7.12, 1990.

[5] M. Rodriguez, M. V. M. Lopez, F. J. Azcondo, J. Sebastian, and D. Maksimovic, "Average inductor current sensor for digitally controlled switched-mode power supplies," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3795-3806, Aug. 2012.

[6] D. Maksimovíc, Y. Jang, and R. W. Erickson, "Nonlinear-carrier control for high-power-factor boost rectifiers," *IEEE Trans. Power Electron.*, Vol. 11, No. 4, pp. 578-584, Jul. 1996.

[7] IR1150 DATASHEET NO.PD60230, International Rectifi er.

[8] ICE1PCS01 DATASHEET V1.2 18 Feb 2005, Infineon Technologies AG.

[9] J. P. Gegner and C. Q. Lee, "Linear peak current mode control: A simple active power factor correction control technique for continuous conduction mode," in *Proc. IEEE Power Electron. Spec. Conf.*, Vol. 1, pp. 196-202, 1996.

[10] S. Ben-Yaakov and I. Zeltser, "PWM converters with resistive input," *IEEE Trans. Ind. Electron*., Vol. 45, No. 3, pp. 519-520, Jun. 1998.

[11] Z. Lai and K. A. Smedley, "A family of continuous-conduction-mode power-factor-correction controllers based on the general pulse-width-modulator," IEEE Trans. Power Electron., Vol. 13, No. 3, pp. 501-510, May 1998.

[12] J. Rajagopalan, F. C. Lee, and P. Nora, "A general technique for derivation of average current mode control laws for single-phase power-factor-correction circuits without input voltage sensing," *IEEE Trans. Power Electron*., Vol. 14, No. 4, pp. 663-672, Jul. 1999.

[13] J. Zhou, Z. Lu, Z. Lin, Y. Ren, Z. Qian, and Y. Wang, "Novel sampling algorithm for DSP controlled 2 kW PFC converter," *IEEE Trans. Power Electron*., Vol. 16, No. 2, pp. 217-222, Mar. 2001.

[14] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche, and J. A. A. Melkebeek, "A sampling algorithm for digitally controlled boost PFC converters," *IEEE Trans. Power Electron*., Vol. 19, No. 3, pp. 649-657, May 2004.

[15] A. Olayiwola, B. Sock, M. R. Zolghadri, A. Homaifar, M. Walters, and C. Doss, "Digital controller for a boost PFC converter in continuous conduction mode," *Proc. IEEE Conf. on Industrial Electronics and Applications*, pp. 1-8, 2006.

[16] S. Buso, P. Mattavelli, L. Rossetto, and G. Spiazzi, "Simple digital control improving dynamic performance of power factor preregulators," *IEEE Trans. Power Electron*., Vol. 13, No. 5, pp. 814-823, Sep. 1998.

[17] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche, and J. A. A. Melkebeek, "Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Trans. Ind. Electron*., Vol. 52, No. 1, pp. 108-115, Feb. 2005.

[18] S. Bibian and H. Jin, "Digital control with improved performance for boost power factor correction circuits," *Proc. IEEE Applied Power Electronics Conf. and Exposition*, pp. 137-143, 2001.

[19] W. Zhang, Y. F. Liu, and B. Wu, "A new duty cycle control strategy for power factor correction and FPGA implementation," *IEEE Trans. Power Electron.*, Vol. 21, No. 6, pp. 1745-1753, Nov. 2006.

[20] A. Garcia, A. de Castro, O. Garcia, and F. Azcondo, "Pre-calculated duty cycle control implemented in FPGA for power factor correction," in *Proc. IEEE 35th Annu. Ind. Electron. Conf.*, pp. 2955-2960, 2009.

[21] S. Moon, L. Corradini, and D. Maksimovic, "Autotuning of digitally controlled boost power factor correction rectifiers," *IEEE Trans. Power Electron*., Vol. 26, No. 10, pp. 3006-3018, Oct. 2011.

[22] A. de Castro, P. Zumel, O. Garcia, T. Riesgo, and J. Uceda, "Concurrent and simple digital controller of an AC/DC converter with a power factor correction based on an FPGA," *IEEE Trans. Power Electron*., Vol. 18, No. 1, pp. 334-343, Jan. 2003.

[23] C. W. Clark, F. Musavi, and W. Eberle, "Digital DCM detection and mixed conduction mode control for boost PFC converters," *IEEE Trans. Power Electron*., Vol. 29, No. 1, pp. 996-1005, Jan. 2014.

[24] R. W. Erickson and D. Maksimovíc, *Fundamentals of Power Electronics*, Norwell, MA: Kluwer, 2001.

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