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High Efficiency Design Considerations for the Self-Driven Synchronous Rectified Phase-Shifted Full-Bridge Converters of Server Power Systems

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Abstract

This paper presents a high frequency design approach for improving efficiency over a wide load range in the self-driven phase-shifted full-bridge converters for server power systems. In the proposed approach, a detailed ZVS analysis of the lagging leg switches in both the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) is presented. The optimum dead time and the determination of the appropriate operation mode are given for high efficiency according to the load conditions. Finally, the optimum operation conditions are defined to achieve a high-efficiency. A laboratory prototype operating at 80 kHz, rated 1 kW (12 V-83.3 A), is built to verify proposed theoretical analysis and evaluations. The experimental results show that the maximum efficiency is achieved as 95% and 83.5% at full load and 5% load conditions, respectively.

Key words: CCM-DCM operation, Phase shifted full bridge converter, Self-driven synchronous rectifier, Wide load range efficiency

I. INTRODUCTION

Recently, research efforts on the power converters used in server power systems have focused on achieving a high efficiency over a wide load range due to the worldwide depletion of energy sources and global warming. In addition, in server power systems, increasing energy consumption due to higher energy demand and rising energy costs require a high-efficiency power conversion. Furthermore, the server power systems utilized in information technology usually use parallel structures that share the total load in the case of a failure. This structure also increases the reliability of the system. Therefore, high-efficiency power conversion over a wide load range is becoming an important key parameter in converter design in order to save energy and reduce the size of cooling elements[1]-[6].

The phase-shifted full-bridge (PSFB) converter is widely used for server power systems and data center applications due to its high conversion efficiency, high power density, simple control structure and low electromagnetic interference (EMI) [2]-[16]. In general, the PSFB converter is used as the second stage dc-dc conversion of two-stage server power systems with a low output voltage and a high output current. In these systems, the conduction loss of the rectifiers is dominated into the total conversion losses under heavy load conditions. Thus, only designs where the secondary side conduction losses are taken into consideration can achieve a high conversion efficiency [4].

However, under the light load conditions, the switching and core losses constitute the main part of the total losses [5]-[7]. Since the zero voltage switching (ZVS) turn-on of the primary switches depends on the load conditions, the lagging leg switches are turned on with hard switching under light load conditions. In order to improve the light load efficiency, various methods have been proposed in the literature [6]-[11]. However, these methods require additional circuit components and complex control circuit designs to achieve extended ZVS turn-on for the lagging leg switches. Operation in the DCM under light load conditions is another simple option to maintain the ZVS turn-on of the lagging leg switches. Besides, DCM operation reduces the core loss by extending the dead time [5], [12]. In [5], an active control method for the synchronous rectifiers at the secondary side was developed and it was found to improve the efficiency

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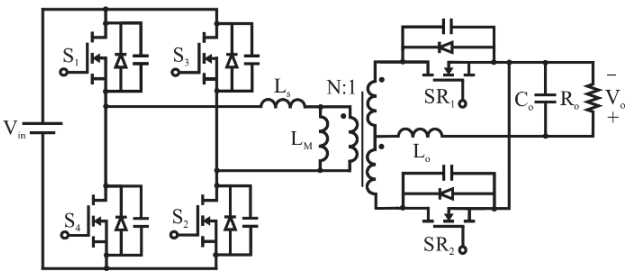


Fig. 1. The power stage circuit diagram of PSFB PWM DC-DC converter.

under light load conditions. However, the self-driven method was not discussed.

The use of a synchronous rectifier (SR) is a well-known option to reduce the high conduction losses especially in the low output voltage applications. In [4], a design optimization achieving 99% efficiency at 25 kHz operation frequency was reported. In that study, parallel connected SRs help to reduce high conduction loss at the secondary side. However, the active gate driver design for the parallel connected SRs increases complexity of the system because large PCB surface is needed for SRs drivers and their isolated power supply. The self-driving method seems to be more attractive when compared to the active gate drive method thanks to its simplicity and easy implementation, especially for cases where SRs are connected in parallel. Various self-driving techniques using current driven or voltage driven techniques for the low output voltage and high output current applications have been proposed. The current driven methods require output current sensing with a current transformer and extra circuit components to convert the sensing current into an appropriate gate drive voltage [2], [14], [18], [19]. In these studies, cost and the complexity of the driver circuit is high due to the additional circuit components. The voltage driven method uses the power transformer directly or the auxiliary winding is used to generate driving signals which in turn results in a cheap and simple solution [17], [20]. In [20], a method using the auxiliary winding to drive the SRs was proposed. That technique provides conduction of both SRs when the primary voltage is zero during the dead time. On the other hand, the conventional self-driver method uses the secondary voltage of the power transformer directly.

In this study, a self-driven synchronous rectified PSFB converter design approach is presented in order to obtain a high efficiency over a wide load range for server power systems. A detailed ZVS analysis of the lagging leg switches in the CCM and the DCM is presented to determine the appropriate operation mode and the optimum dead time according to the load conditions. To reduce the high conduction loss, the SRs are used for the center taped rectifier on the secondary side. A self-driven circuit is considered to avoid the need for an additional active control circuit on the secondary side. The self-driver method proposed in [20] is applied to generate control signals for the SRs. Finally, a prototype operating at 80 kHz with 1 kW (12 V-83.3 A) of output power has been built to validate the theoretical performance analysis and evaluations.

The rest of this paper is organized as follows: Section II gives a ZVS analysis of the lagging leg switches in the CCM and the DCM. Section III evaluates the dead time optimization and the appropriate mode selection. Section IV presents the experimental results. Section V provides the conclusion.

II. ZVS Analysis of the Lagging Leg Switches in CCM and DCM

The general operation principle of a PSFB converter with a center tapped rectifier is well known and proposed in many papers in the literature [3], [4]. Therefore, so the analysis given here is focused on the interval achieving ZVS turn-on of the switches in the lagging leg.

A power stage circuit diagram of the synchronous rectified PSFB PWM DC-DC converter is shown in Fig. 1. Here, S_1-S_4 are the primary side switches, and they include antiparallel diodes and parasitic capacitors. SR_1 and SR_2 represent the synchronous rectifier reducing conduction losses on the secondary side. L_M is the mutual inductance, L_s is the equivalent inductance which is the sum of the leakage inductance of the transformer and additional inductance connected in series to the primary side. N is the turns ratio of the high frequency power transformer, L_o and C_o are the output filter components, V_{in} is the input voltage source, and V_o is the output voltage.

In the analysis, semiconductor devices, inductors and capacitors are accepted as ideal. It is also assumed that output inductance is high enough and its current is constant for one switching cycle. The equivalent circuit diagrams and the related key waveforms in the CCM and the DCM are shown in Fig. 2 and Fig. 3, respectively.

In the CCM, before S_2 is turned-off, S_1 is turned-off so that the output capacitor of S_1 and S_4 is charged and discharged, respectively. Then, converter starts working in the freewheeling mode. The primary side of the transformer is short circuited by the conduction of the antiparallel diode of S_4 and the conduction of the S_2 MOSFET. As shown in Fig. 2(a), after S_2 is turned off, the primary current charges and discharges the output capacitor of S_2 and S_3, respectively. The antiparallel diode of S_3 conducts after the output capacitor of S_3 discharges completely, and the ZVS turn-on for S_3 can be achieved. However, both SR_1 and SR_2 are turned on during this stage for the output current commutation. Thus, the secondary side of the transformer is short circuited and the load current cannot reflect to the primary side in this interval. Therefore, the primary current quickly decreases and the stored energy in L_s alone should be sufficient to completely

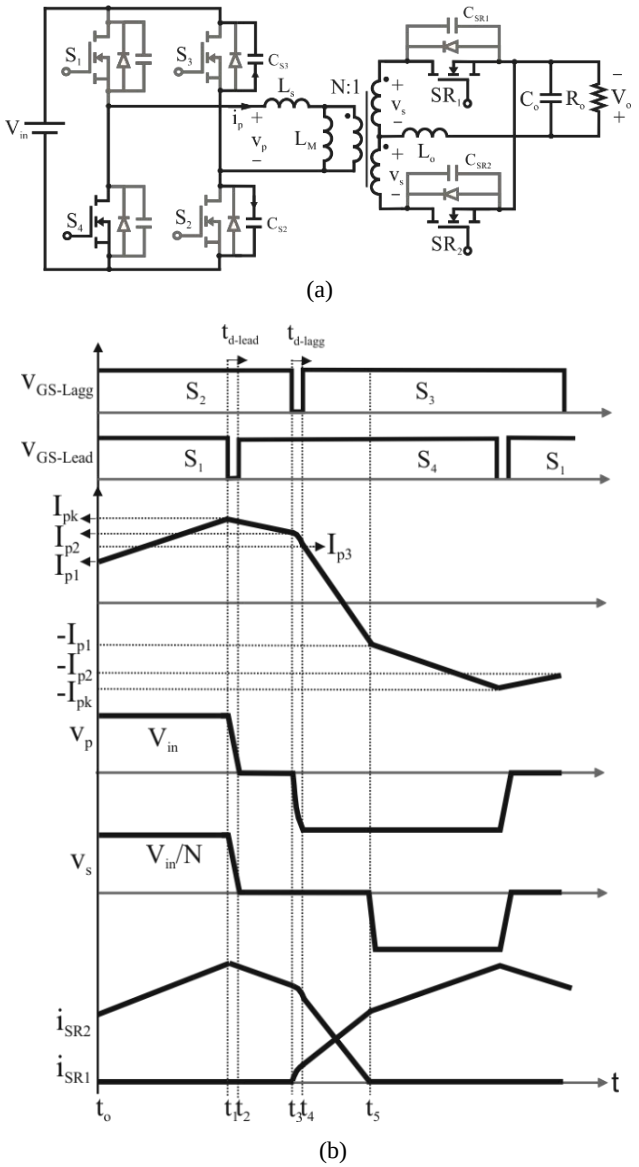


Fig. 2. (a) The equivalent circuit diagram achieving ZVS turn-on in the lagging leg. (b) The related key waveforms in CCM.

charges/discharges the output capacitor of the lagging leg switches:

$$\frac{1}{2}L_s I_{p-cr}{}^2 \geq \frac{1}{2}C_{lagg}V_{in}{}^2 . \quad (1)$$

In the above equations, $I_{p\text{-}cr}$ is the critical primary current and C_{lagg} defines the equivalent output capacitance during resonance. Thus, the required critical current value, $I_{p\text{-}cr}$, or the load condition to charge/discharge the output capacitors of the switches can be determined by:

$$I_{p-cr} = V_{in}\sqrt{\frac{C_{lagg}}{L_s}} . \quad (2)$$

In order to achieve the ZVS turn-on, the dead time in the CCM, $\delta_{R\text{-}CCM}$, should be one quarter of the resonance period as follows:

$$\delta_{R-CCM} = \frac{T_r}{4} = \frac{\pi}{2}\sqrt{L_s C_{lagg}} \quad (3)$$

During the output current commutation, there is no power transfer from the input to the output due to the fact that both of the SRs conduct at the same time and the voltage of the secondary side of transformer is zero. This time is defined as the lost duty ratio time interval. Therefore, the voltage gain can be written as:

$$V_o = \frac{V_{in}}{N}(D - \Delta D). \quad (4)$$

Where, ΔD is the lost duty ratio including $\delta_{R\text{-}CCM}$. The difference between the total duty ratio, D, and ΔD gives the effective duty ratio, D_{eff}.

$$D_{eff} = D - \frac{2L_s(I_{p3} + I_{p1})f_s}{V_{in}} - 2\delta_{R-CCM} f_s \quad (5)$$

Where I_{p1} is the minimum value of the primary current, I_{p3} is the primary current value after the capacitors of the lagging leg switches charge/discharge completely, and they can be defined as:

$$I_{p1} = \frac{1}{N}(I_o - \frac{\Delta I_o}{2}) \quad (6)$$

$$I_{p3} = \sqrt{I_{p2}{}^2 - \frac{V_{in}{}^2 C_{lagg}}{L_s}}. \quad (7)$$

In the above equation, I_o is the output current and ΔI_o is the output current variation. I_{p2} is the operation point of the primary current when freewheeling interval is completed. At this operation point, to provide ZVS turn-on of the lagging leg switches, primary current should be least equal to the critical primary current defined as:

$$I_{p2} \geq I_{p-cr}. \quad (8)$$

In the DCM, the current flowing through the SRs flows discontinuously so that both of the SRs should be turned off to prevent the discharge of the output filter capacitor with the conduction of the SRs. Therefore, the magnetizing inductance of the transformer participates to the resonance between L_S and both the output capacitors of the lagging leg switches and the SRs. Since the SRs are off during the freewheeling interval and their output capacitors are reflected to the primary side in the DCM operation, as shown in Fig. 3(a), the output capacitor of the SRs also has to be charged/discharged while the output capacitor of the lagging leg switches charges/discharges to provide the ZVS turn-on for the primary switches. In this operation, the interval for the output current commutation between the SRs does not occur and the secondary of the transformer is not short-circuited when compared to the CCM operation principle. Therefore, the current stored in the magnetizing inductance is sufficient to charges/discharges the output capacitors when compared to the conventional CCM operation. However, the charge/discharge time of the capacitors is larger than the CCM operation due to the small current value in L_M.

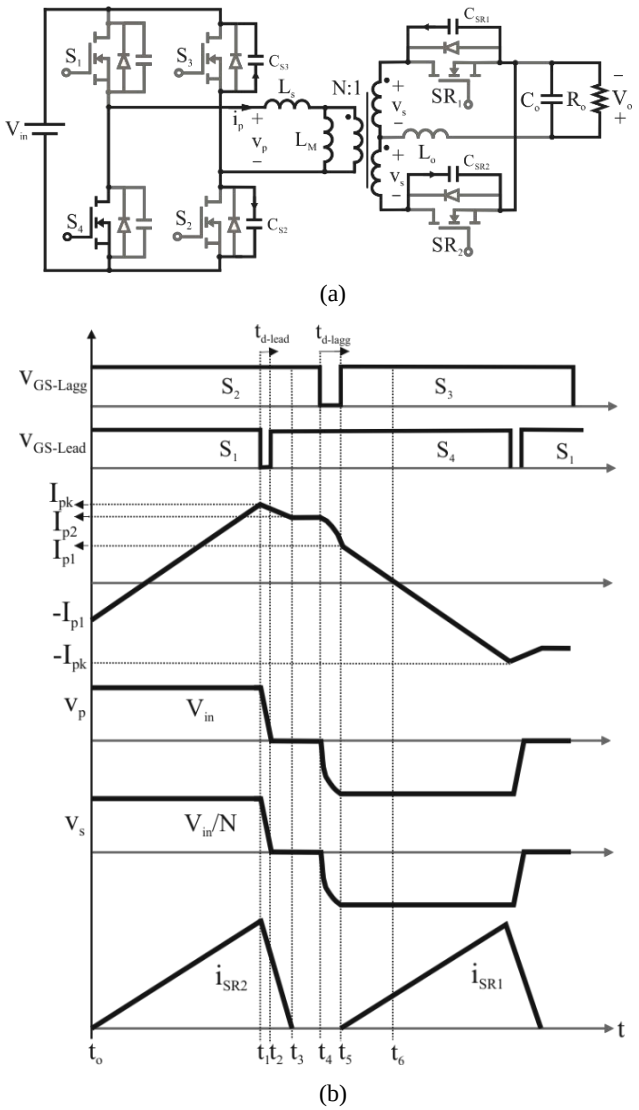


Fig. 3. (a) The equivalent circuit diagram achieving ZVS turn-on in the lagging leg. (b) The related key waveforms in DCM.

Therefore, an extended delay time can achieve the ZVS turn-on of the lagging leg switches in the DCM operation [5]. The energy required to achieve the ZVS of the lagging leg switches can be written as:

$$\frac{1}{2}L_M I_{LM-cr}{}^2 \geq \frac{1}{2}(C_{lagg}+\frac{2C_{SR}}{N^2})V_{in}{}^2. \quad (9)$$

Where I_{LM-cr} represents the critical magnetizing current value to achieve the ZVS, and it can be defined as:

$$I_{LM-cr}=V_{in}\sqrt{\frac{C_{lagg}+2C_{SR}/N^2}{L_M}}. \quad (10)$$

In the above equations, L_s is neglected because it is very small near L_M. The delay time to be extended should be least one quarter of the resonance period as defined by:

$$\delta_{R-DCM}=\frac{T_r}{4}=\frac{\pi}{2}\sqrt{L_M(C_{lagg}+2C_{SR}/N^2)}. \quad (11)$$

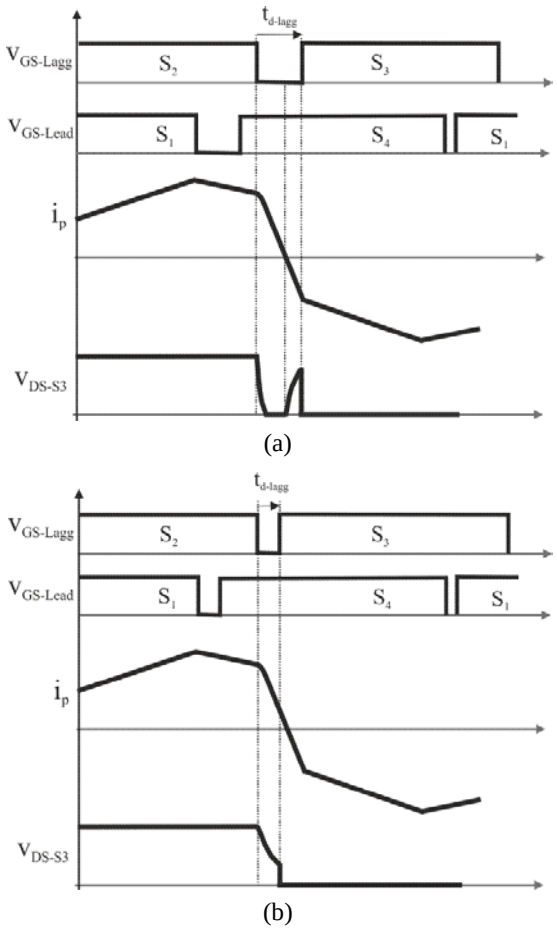


Fig. 4. (a) ZVS turn-on of S_3 with the large dead time. (b) Under the light load condition.

III. Dead Time Optimization and Appropriate Mode Determination

Under heavy load conditions, ZVS turn-on can be easily achieved. However, if the primary current reaches zero or change its direction before the dead time completes, a primary current with an inverse direction recharges the output capacitors as shown in Fig. 4(a). In a similar way, when the load gets smaller, the output capacitors cannot be charged/discharged completely before the primary current reaches zero as shown in the Fig. 4(b). Therefore, the lagging leg switches are turned on with hard switching under light load conditions and with no optimized dead time. This load dependence problem is a well-known disadvantage of PSFB DC-DC converters. Some conventional solutions are usually applied to solve this problem like increasing L_s and adding additional capacitors to the output capacitors. However, these solutions change the conduction and the switching losses in a different way. Consequently, a detailed dead time optimization taking into consideration the overall efficiency and a wide load range can help to cope with the load dependent ZVS turn-on operation of the lagging leg switches at the design stage.

TABLE I
PERFORMANCE COMPARISON OF COOL MOSFET AND SIC MOSFET IN PSFB CONVERTER

Semiconductor Switch	$t_{d\text{-}off}+t_{rv}$	$\delta_{R+}\, t_{linear}$	Required Dead Time for ZVS	Conduction Loss	Turn-off Switching Loss	Lost Duty
Cool MOSFET SPW55N80C3 800 V, 55A	209 ns	275 ns+83 ns =358 ns	209 ns<$t_{d\text{-}lagg}$<358ns	1.85 W	44.23 W	%4.7
SiC CMF20120D 1200 V, 42 A	78 ns	77 ns+83 ns =160 ns	78 ns<$t_{d\text{-}lagg}$<160 ns	1.75 W	16.57 W	%2.6

A. CCM Operation

In the conventional design procedure, the high efficiency is optimized according to a constant dead time giving a desired voltage gain to regulate the output voltage under heavy load conditions. In this approach, the ZVS turn-on of the lagging leg switches can be achieved by a suitable L_s inductor determined for a desired soft switching load range. Therefore, the ZVS turn-on of the lagging leg switches is very strongly dependent on the dead time and L_s inductance.

The required dead time is also determined by the switch characteristics. In this study, SiC MOSFETs and Cool MOSFETs are evaluated as switching components due to their capability in terms of high frequency operation when compared to IGBTs. In these switches, the dead time, $t_{dead\text{-}lagg}$, between S_2 and S_3 can be defined by:

$$t_{dead-lagg} \geq t_{d-off} + t_{rv}. \tag{12}$$

In the formula, $t_{d\text{-}off}$ defines the turn-off delay time, and t_{rv} is the rising time of the switch voltage. The dead time, $t_{dead\text{-}lagg}$, should be larger than the ZVS time interval and it should end before the primary current reaches zero. Here, the ZVS time interval is very short and it can be neglected. Thus, the linear time interval can be defined as follows:

$$t_{linear} = \frac{L_s(I_{p3} + I_{p1})}{V_{in}} \tag{13}$$

Table I shows a calculated performance comparison of Cool MOSFETs and SiC MOSFETs based on the dead time requirements and the losses. Each switch is selected for 400 V of DC input voltage, 1 kW of output power, and an 80 kHz switching frequency. In the calculations, transformer turns ratio, N, is 25, and the snubber inductance, L_s, is 10 μH.

According to results summarized in Table I, the SiC MOSFET has a lower power loss although its voltage rate is higher than the Cool MOSFET. Therefore, SiC device seems to be more suitable and reliable for server power systems using PSFB converters.

Fig. 5 shows the calculated maximum dead time variation as a function of L_s, and the critical primary current required for the ZVS of the lagging leg switches. The maximum dead time increases while L_s increases, and the critical primary current $I_{p\text{-}cr}$ decreases. If the desired ZVS range of the lagging leg switches is determined until the 60% load condition, L_s should be selected as 10 μH. According to the calculated results, the dead time for the lagging leg switches can be selected as 160 ns to achieve ZVS turn-on until the 60% load condition.

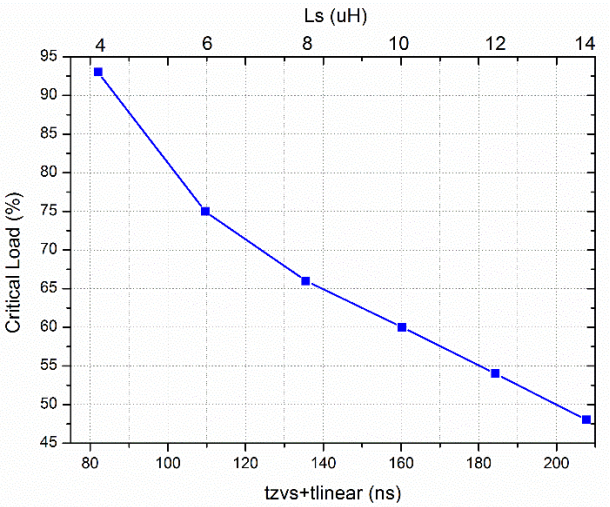


Fig. 5. The maximum dead time variation as the function of L_s and the critical primary current.

The L_s inductance variation effects on the conduction and switching losses over a wide load range should be taken into account to obtain the best efficiency for all of the load conditions. Fig. 6 shows the switching losses over a wide load range as a function of L_s. The switching losses increase slightly while L_s decreases due to reductions in the critical load conditions. Under the critical load condition, the MOSFETs are turned on with hard switching. However, SiC MOSFETs have a small output capacitance so the turn-on switching loss is not as dominant when compared to that over a wide L_s range. However, increasing the switching loss under a 20% load condition seems to be more dominant than that under 60% and 100% load conditions.

Fig. 7 shows the conduction loss variation as a function of L_s. The change in the conduction loss over a wide L_s range is very slight and almost constant. This is due to the fact that the change in the lost duty ratio is very small because of the small output capacitance of the SiC MOSFETs. The SiC

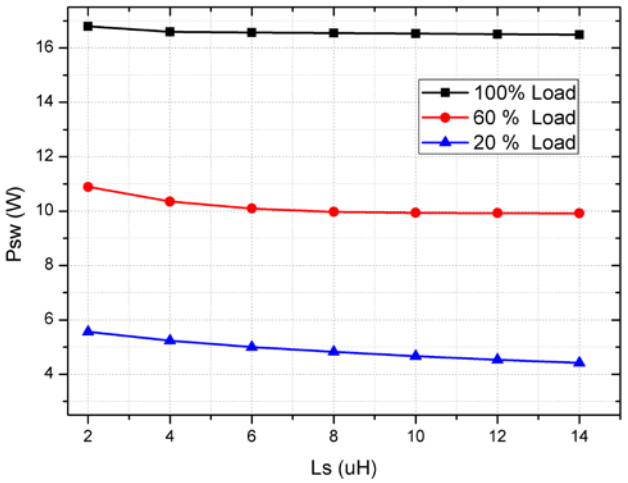


Fig. 6. The switching loss variation as the function of L_s and the load condition.

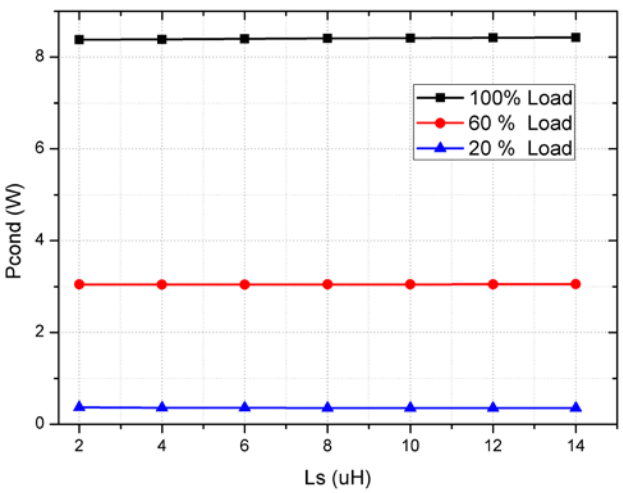


Fig. 7. The conduction loss variation as the function of L_s and the load condition.

MOSFET presents the advantages of a small lost duty ratio and a low switching loss.

B. DCM Operation

In the DCM operation, the ZVS of the lagging leg can be achieved by an extension of the dead time for load conditions that are lighter than 1% as proposed in [5]. In this approach, the effective duty ratio should be reduced according to the voltage gain and the necessary dead time should be determined to charge/discharge the output capacitors of the lagging leg switches and SRs. The voltage conversion ratio can be found by the voltage-sec balance on the output inductor as follows:

$$\frac{V_o}{V_{in}} = \frac{2D}{N\left(D + \sqrt{D^2 + \frac{4I_o L_o f_s}{V_o}}\right)} \tag{14}$$

Solving (14) for D yields:

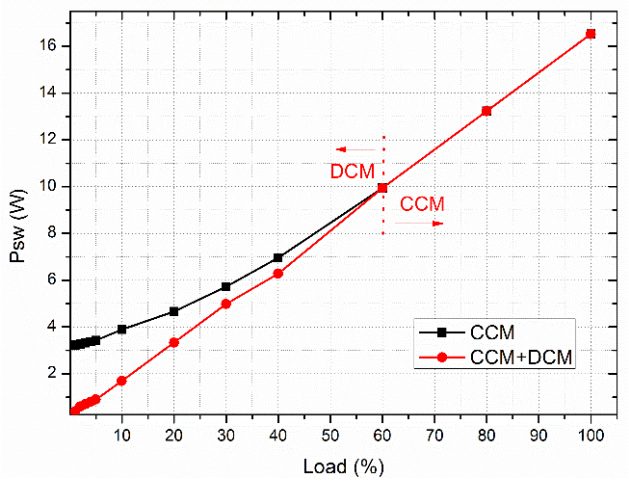


Fig. 8. The switching loss comparison of CCM and CCM+DCM operation over wide load range.

$$D = \sqrt{\frac{N^2 \frac{V_o^2}{V_{in}^2} f_s I_o L_o}{V_o\left(1 - N\frac{V_o}{V_{in}}\right)}}. \tag{15}$$

The stored energy increases while L_M and the output capacitors of the lagging leg switches and SRs decrease. Thus, the SiC MOSFETs, which have small output capacitors, can help to reduce the need for the large energy stored in L_M to achieve ZVS turn-on when compared to the Cool MOSFETs. The required dead time for the DCM operation can be calculated by (11).

Fig. 8 shows the variation of the switching loss according to the load conditions in the CCM and CCM+DCM operations. The DCM operation maintains the ZVS operation under the 60% critical load condition and switching loss is lower when compared to the CCM operation condition. However, in the DCM operation, the SRs should be turned off to prevent the discharge of the output filter capacitor through the SRs. This results in high conduction losses due to the conduction of the body diodes. Therefore, with DCM operation under a 60% load condition, it is not possible to obtain a high efficiency.

Because both of the SRs are in the off state, there is no output current commutation interval on the secondary side in the DCM. The absence of an output current commutation can compensate for the body diode's conduction losses. However, it is still not enough when compared to the parallel connected SRs implemented in this study. Fig. 9 shows the variation of the conduction losses in the CCM and CCM+DCM operations. The DCM operation is applied under the 5% load condition and the conduction loss suddenly increases when the body diodes starts to conduct. However, the reducing core loss and the switching loss are dominant in the overall loss, and the efficiency under the 5% load condition is higher than the CCM operation as shown in the Fig. 10.

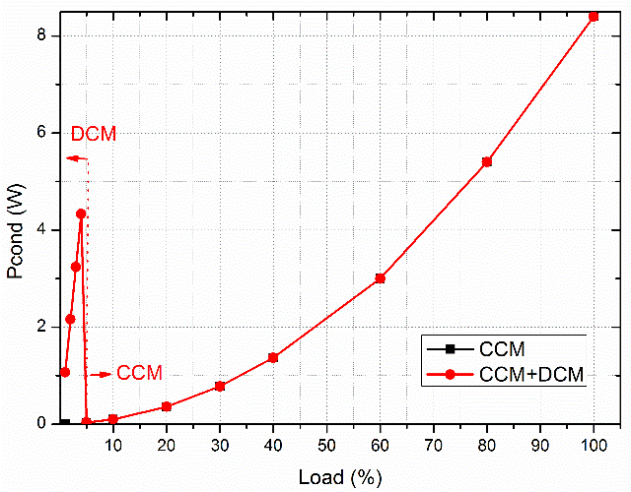


Fig. 9. Conduction loss comparison of CCM and CCM+DCM operation over wide load range.

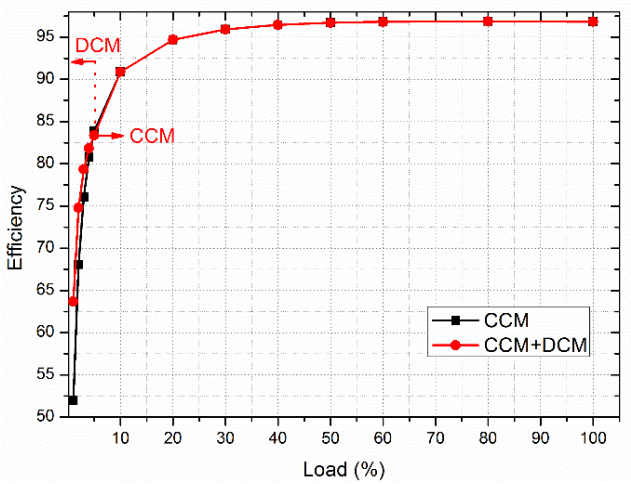


Fig. 10. Efficiency comparisons of CCM and CCM+DCM operation over wide load range.

According to the theoretical evaluation given above, the synchronous rectified PSFB DC-DC converter can be designed to operate in the CCM up to the 5% load condition, and in the DCM under the %5 load condition to obtain the best efficiency over a wide load range.

IV. Experimental Results

A server adapter with a 12 V output voltage and rated at 1 kW is built to validate the theoretical analysis given above. The components and operation conditions evaluated for the prototype are summarized in Table II. A 400 V DC input voltage is applied to the input of the self-driven synchronous rectified PSFB converter. The self-driven method proposed in [20] is used to drive five parallel connected SR at the secondary side.

TABLE II
The Components and the Operation Conditions Evaluated for the Server Adapter Prototype

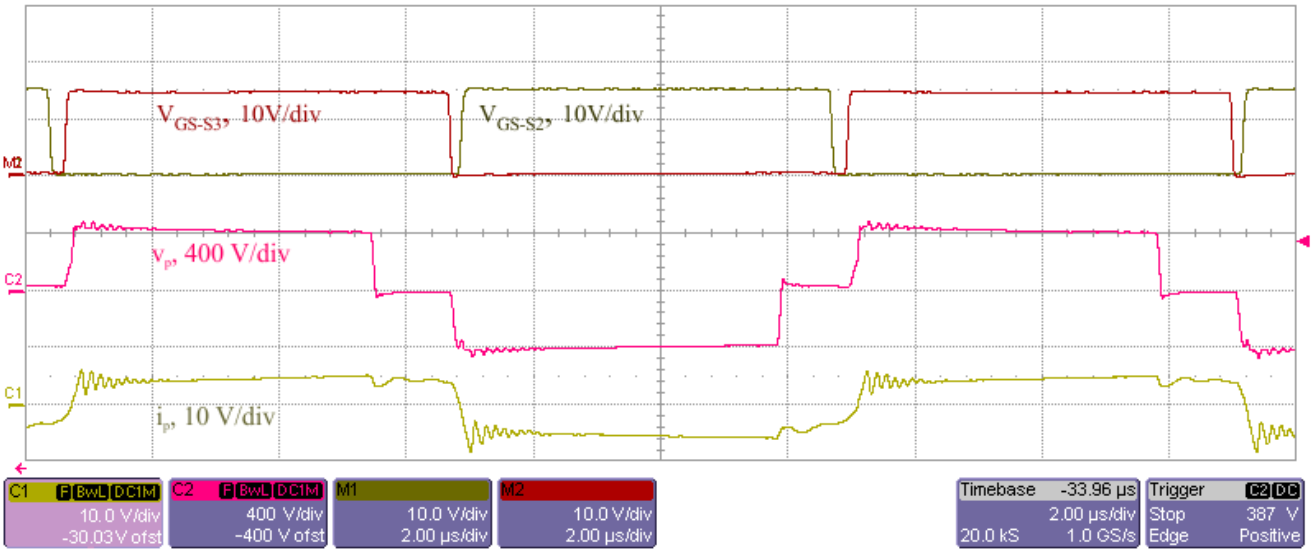
Primary Switches (S_1-S_4)	SiC CMF20120D 1200 V, 42 A
Secondary Switches (SR_1-SR_2)	IRFP4110Pbf 100 V, 180 A
Transformer	E65/32/27, N:25 N_p=25, N_s=1, $N_{aux\text{-}SR}$=1
L_o	UU-120B, Cut legs N_{Lo}=1, 1.1 µH
L_s	10 µH
L_M	5.6 mH
C_o	264 µF Ceramic Capacitor
ΔI_o	0.20
CCM	Up to 5% load
DCM	Under 5% load

The primary current and the voltage waveforms in the CCM and the DCM are given in Fig. 11(a) and Fig. 11(b), respectively. In these figures, it is observed that the experimental results are in good agreement with the theoretical analysis.

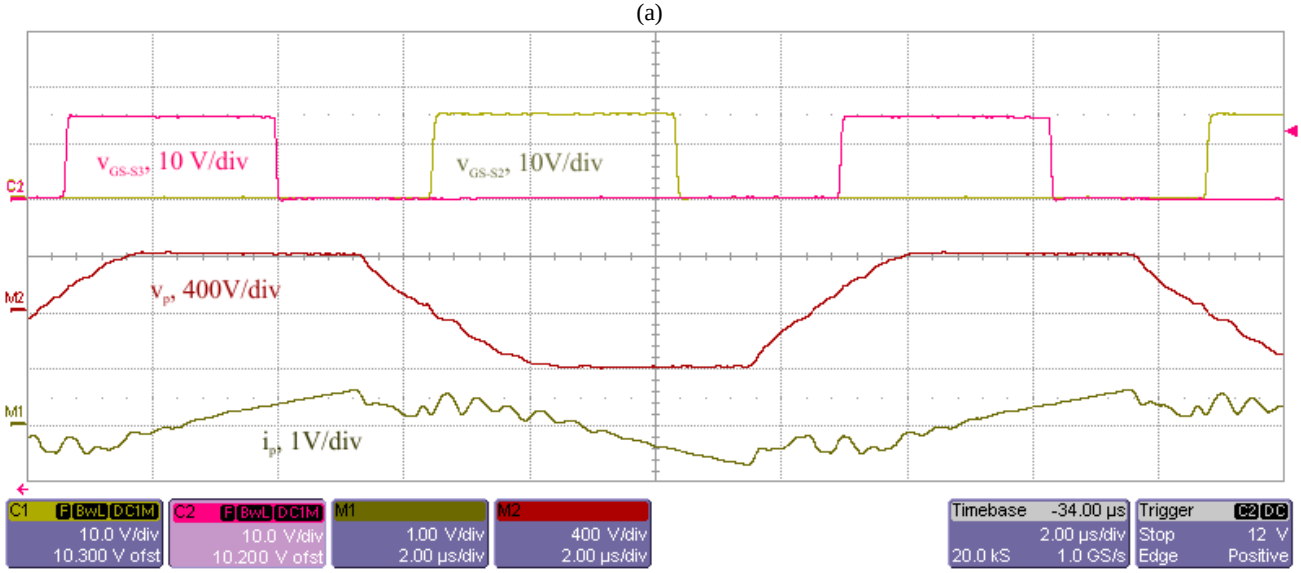
The ZVS turn on of the S_2 switch in the lagging leg while operating in the CCM, is shown in Fig. 12. The dead time is fixed at 160 ns to achieve ZVS turn-on under the full load condition. The switch is turned on while its body diode is conducting and the ZVS turn on is achieved.

In Fig. 13, the ZVS turn on of the S_2 switch in the DCM operation is given. Since both of the SRs are off in the DCM, L_M attends the resonance between L_s and the output capacitors of the primary MOSFETs and the SRs. Thus, ZVS turn on can be achieved easily by the energy stored in L_M. In the DCM operation, the dead time of the lagging leg is extended to 2.4 µs. Thus, the output capacitor of the MOSFET is discharged completely and S_2 is turned on while its body diode is conducting.

A comparison of the measured and calculated efficiency for the self-driven synchronous rectified PSFB converter operating in the CCM+DCM and the diode rectified conventional PSFB converter operating in the CCM is given in Fig. 14. In the conventional design, a Schottky diode with a 0.77 V voltage drop is used at the secondary side instead of the SRs. The proposed design approach shows better performance over a wide load range. The efficiency is 4% and 5% higher than the conventional design under 5% load and full load conditions, respectively.



(a)



(b)

Fig. 11. The primary current and the voltage waveforms in (a) CCM under the full load condition and (b) DCM under 1% load condition.

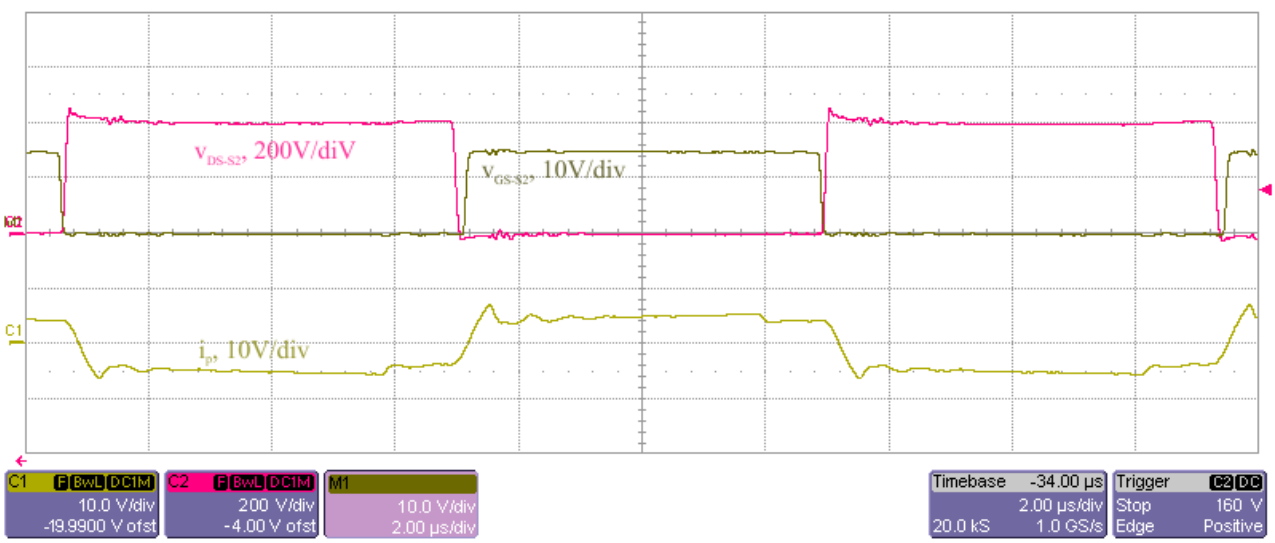


Fig. 12. ZVS turn-on of S_2 switch in CCM and under the full load condition.

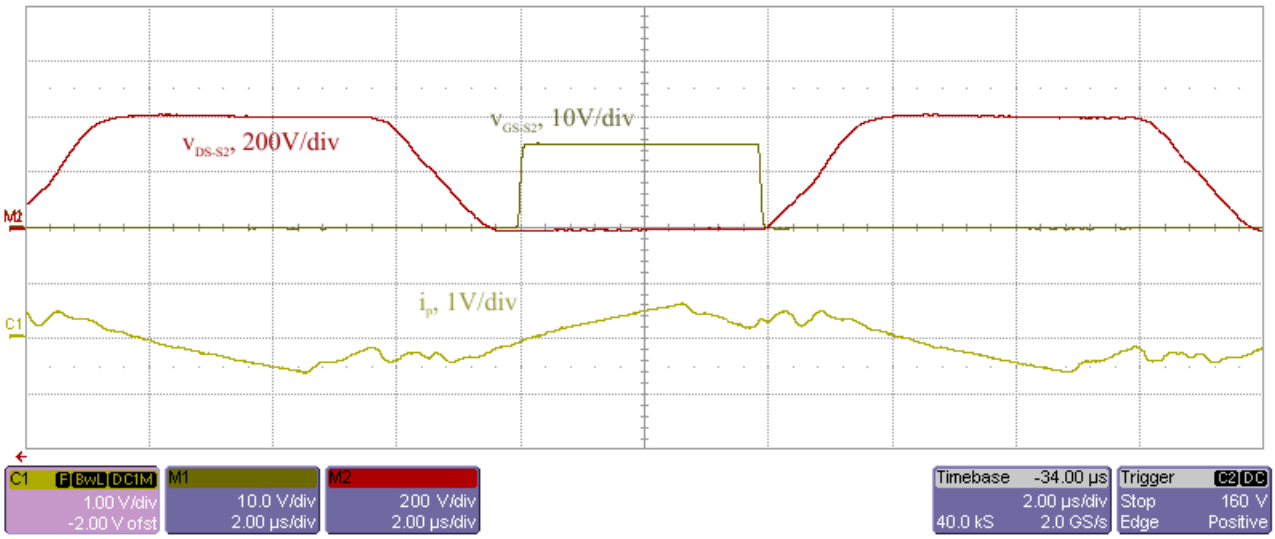


Fig. 13. ZVS turn-on of S_2 switch in DCM and at 1% load condition.

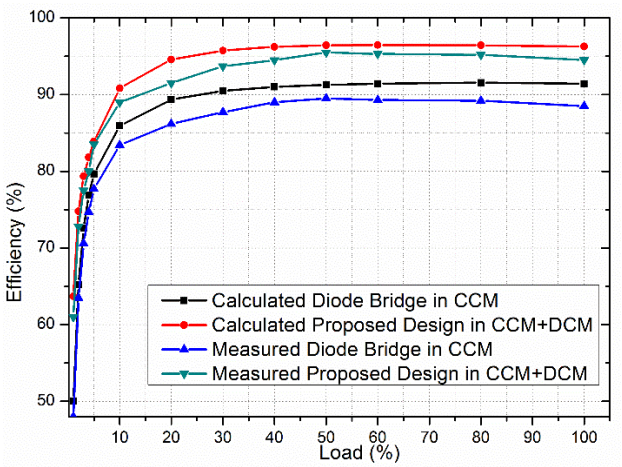


Fig. 14. The efficiency comparison for the proposed design approach and the conventional diode bridge design as analytically and experimentally.

V. CONCLUSION

A self-driven synchronous rectified PSFB converter design approach is proposed to obtain a high efficiency over a wide load range. The CCM and DCM operations are analyzed based on the ZVS turn on of the lagging leg switches. The dead time optimization in each operation mode is discussed based on the high efficiency and load condition. In addition, to reduce the conduction loss, SRs are used for the center tapped rectifier and a self-driver is applied to drive the SRs on the secondary side. Finally, the given theoretical analysis is verified by an experimental setup for 1 kW output power, 12 V output voltage and 400 V DC input voltage. The measured and calculated efficiency performance of the proposed design approach for the self-driven synchronous rectified PSFB converter is better than that of the diode rectified conventional PSFB converter. The optimization of the dead time according to the load condition can help to improve the efficiency over a wide load range in low voltage and high power applications such as server power systems. Self-driven SRs also reduce the total cost, volume and weight of the overall converter system.

REFERENCES

[1] J. W. Kolar, U. Drofenik, J. Biela, M. Heldwein, H. Ertl, T. Friedli, and S. Round, "PWM converter power density barriers," *IEEJ Trans. Ind. Appl.*, Vol.128, No.4, pp. 1-14, 2008.

[2] C. Zhao, X. Wu, P. Meng, and Z. Qian, "Optimum design consideration and implementation of a novel synchronous rectified soft-switched phase-shift full-bridge converter for low-output-voltage high-output-current applications," *IEEE Trans. Power Electron.*, Vol. 24, No. 2, pp. 388-397, Feb. 2009.

[3] U. Badstuebner, J. Biela, D. Christen, and J. W. Kolar, "Optimization of a 5-kW telecom phase-shift DC–DC converter with magnetically integrated current doubler," *IEEE Trans. Power Electron.*, Vol. 58, No. 10, pp. 4736-4745, Oct. 2011.

[4] U. Badstuebner, J. Biela, and J. W. Kolar, "An optimized, 99 % efficient, 5kW, phase-shift PWM DC-DC converter for data centers and telecom applications," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, pp. 773-780, 2010.

[5] J. W. Kim, D. Y. Kim, C. E. Kim, and G. W. Moon, "A simple switching control technique for improving light load efficiency in a phase-shifted full-bridge converter with a server power system," *IEEE Trans. Power Electron.*, Vol. 29, No. 4, pp. 1562-1566, Apr. 2014.

[6] D. Y. Kim, C. E. Kim, and G. W. Moon, "Variable delay time method in the phase-shifted full-bridge converter for reduced power consumption under light load conditions," *IEEE Trans. Power Electron.*, Vol. 28, No. 11, pp. 5120-5127, Nov. 2013.

[7] Y. Jang and M. M. Jovanovic, "Light-load efficiency optimization method," *IEEE Trans. Power Electron.*, Vol.

25, No.1, pp.67-74, Jan. 2010.
[8] B. Y. Chen, and Y. S. Lai, "Switching control technique of phase-shift controlled full-bridge converter to improve efficiency under light-load and standby conditions without additional auxiliary components," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 1001-1012, Apr. 2010.
[9] M. Pahlevaninezhad, S. Eren, P. Jain, and A. Bakhshai, "Self-sustained oscillating control technique for current-driven full-bridge DC/DC converter," *IEEE Trans. Power Electron.*, Vol. 28, No. 11, Nov. 2013.
[10] B. Gu, C.-Y. Lin, J. Dominic, and J.-S. Lai, "Zero-voltage-switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, Vol. 28, No. 10, pp. 4657-4667, Oct. 2013.
[11] A. F. Bakan, N. Altintas, and I. Aksoy, "An improved PSFB PWM DC–DC converter for high-power and frequency applications," *IEEE Trans. Power Electron.*, Vol. 28, No. 1, pp. 64-74, Jan. 2013.
[12] Y. V. Singh, K. Viswanathan, R. Naik, J. A. Sabate, and R. Lai, "Analysis and control of phase-shifted series resonant converter operating in discontinuous mode," in *Proc. Applied Power Electronics Conference and Exposition (APEC)*, pp. 17-21, 2013.
[13] B. Gu, C. Y. Lin, B. Chen, J. Dominic, and J. S. Lai, "Zero-voltage-switching PWM resonant full-bridge converter with minimized circulating losses and minimal voltage stresses of bridge rectifiers for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, Vol. 28, No. 10, pp. 4657-4667, Oct. 2013.
[14] C. Zhao, X. Wu, W. Yao, and Z. Qian, "Synchronous rectified soft-switched phase-shift full-bridge converter with primary energy storage inductor," in *Proc. Applied Power Electronics Conference and Exposition*, pp. 581-586, 2008.
[15] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kW, 1-U, 10-kW/dm3 resonant DC–DC converter for telecom applications," *IEEE Trans. Power Electron.*, Vol. 24, No.7, pp. 1701-1710, Jul. 2009.
[16] S. Cetin, "Wide load range high efficiency design consideration of a self-driven synchronous rectified phase-shifted full-bridge converter for server power system," *Int. Conference on Power Engineering, Energy and Electrical Drives*, pp. 33-43, 2014.
[17] M. Xu, Yu. Ren, J. Zhou, and F. C. Lee, "1-MHz self-driven ZVS full-bridge converter for 48-V power pod and DC/DC brick," *IEEE Trans. Power Electron.*, Vol. 20, No.5, pp. 997-1006, Sep. 2005.
[18] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, "A novel high frequency current-driven synchronous rectifier applicable to most switching topologies," *IEEE Trans. Power Electron.*, Vol. 16, No.5, pp. 635-648, Sep. 2001.
[19] J. M. Zhang, X. G. Xie, D. Z. Jiao, and Z. Qian, "A high efficiency adapter with novel current driven synchronous rectifier," in *Proc. Telecommunications Energy Conference*, pp. 205-210, 2003.
[20] P. Alou, J. A. Cobos, O. García, R. Prieto, and J. Uceda, "A new driving scheme for synchronous rectifiers: single winding self-driven synchronous rectification," *IEEE Trans. Power Electron.*, Vol. 16, No. 6, pp. 803-811, Nov. 2001.

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