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An Inherent Zero-Voltage and Zero-Current-Switching Full-Bridge Converter with No Additional Auxiliary Circuits

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Abstract

An inherent zero-voltage and zero-current-switching phase-shifted full-bridge converter with reverse-blocking insulated-gate bipolar transistor (IGBT) or non-punch-through IGBT is proposed in this paper. This converter not only ensures that the switches in the lagging leg works at zero-current switching, but also minimizes circulating conduction loss without any additional auxiliary circuits. A 1.2 kW hardware prototype is designed, fabricated, and tested to verify the proposed topology. The control loop design procedures with small-signal models are also presented. A simple, low-cost, and robust democratic current-sharing circuit is also introduced and verified in this study. The proposed converter is a suitable alternative for compact, cost-effective applications with high-voltage input.

Key words: Full bridge, Non-Punch-Through IGBT, Phase shifted, Reverse-Blocking IGBT, Zero-voltage and zero-current switching

I. INTRODUCTION

Galvanic isolated full-bridge (FB) converter is the standard topology in medium- and high-power applications, such as telecom power supplies, X-ray generators, electrical vehicles, and traction applications [1]-[4]. The main concerns in these fields are reliability, efficiency, power density, cost, and other specific specifications (e.g., wide soft-switching range, low topology-complexity, small circulating current, and minimized duty cycle loss) [1]-[3]. Three converter types can fulfill these demands: resonant FB [3], phase-shift pulse-width-modulated (PS PWM) FB [1], and hybrid resonant and PS PWM FB converters [5], [6].

Resonant circuit topologies, especially variable frequency LLC converters, have become popular in recent years. The major advantages of these topologies are zero-voltage switching (ZVS) or zero-voltage transition and nearly zero-current switching (ZCS) for primary switches, ZCS for output diodes, and eliminated output choke. In addition, a wide range of soft switching is achieved even with no-load condition. However, the extremely high runaway frequency at no-load or short-circuit condition is a potential threat to system reliability.

Alternatively, additional series inductors are often inserted but can be bulky with more duty cycle loss and circulating current to extend the ZVS range of the classic constant-frequency PS PWM FB converters [1]-[4]. Hybrid resonant and PS PWM FB converters significantly lower series inductance with true full-range soft switching and negligible duty cycle loss features [5], [6]. These converters are suitable candidates for electric vehicle chargers at the cost

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of complicated structures and control strategies.

High-voltage insulated-gate bipolar transistors (IGBTs) with constant voltage drop are often preferred in three-phase 380 Vac/440 Vac or 750 Vdc/1500 Vdc input systems. A series of zero-voltage and zero-current-switching (ZVZCS) techniques has been proposed to solve the IGBT tail current issue in the lagging leg (e.g., primary impedance blocking, primary resetting, secondary voltage clamping, and output voltage resetting) [7]-[12]. These auxiliary circuits are almost inevitable, and negative effects should also be considered (e.g., steady-state primary current overshoot and additional high-voltage stress of the rectifier during the start-up period).

These techniques were recently reviewed and reexamined to achieve the balance between performance and cost with novel commercial SiC and Si devices [13], [14]. Complex three-level FB converters that use low-voltage MOSFETs are another possible solution [15]. New high-speed generations of IGBTs have already been recognized as a cost-effective alternative to super junction MOSFETs in zero-voltage transition PS FB high-voltage to low-voltage DC/DC converters. The capacitive snubber or resonant inductor can be optimized for particular operating points, but not for required wide operating ranges as shown in [14]. Measures to improve the efficiency must be carefully selected to avoid conditions wherein a loss mechanism is lowered or partly avoided, whereas others are unintentionally increased, thus canceling the expected benefits. The analysis in [14] also shows that the best converter efficiency can be achieved without additional components in the case of IGBT_H3.

Among these next-generation IGBTs, Reverse-Blocking (RB) IGBTs have been investigated and tested in current-source inverters, resonant inverters, T-type neutral-point-clamped converters, and matrix AC/AC choppers. RB IGBTs offer more advantages over functionally comparable conventional circuits, such as loss reduction, compact structure, and lower cost [16]-[22].

The present study attempts to determine a low topology-complexity ZVZCS PS PWM FB converter with few negative effects for high-input voltage application. A novel, inherent ZVZCS PS PWM FB converter without additional auxiliary circuits is also proposed, described, designed, and tested. The proposed converter can achieve ZCS for lagging-leg switches without a circulating current with the help of RB IGBT or non-punch-through IGBT with RB feature.

II. Basic Operation Principle of the Novel Converter

Fig. 1 illustrates the circuit diagram of the proposed inherent ZVZCS PS PWM FB converter, which consists of the following four parts:

1) the leading leg, including two IGBTs S_1 and S_2 with their anti-parallel diodes Ds_1, Ds_2;
2) the lagging-leg, including two RB IGBTs S_3 and S_4 without anti-parallel diodes;
3) blocking capacitor C_B, main transformer T_r, and its leakage inductor L_{lk};
4) output rectifiers D_1, D_2, and LC filter L_f, C_0.

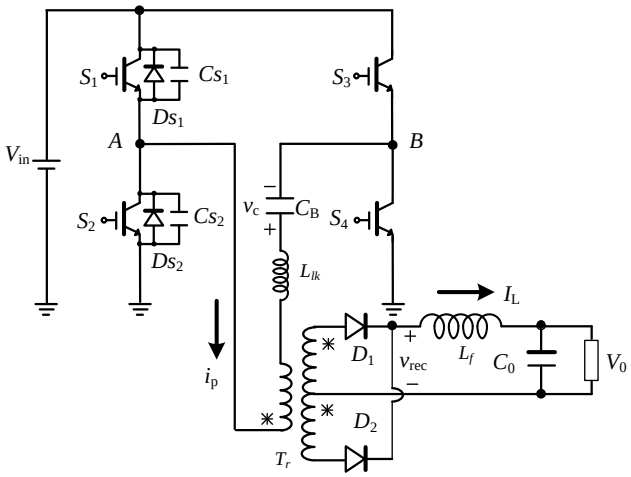

Fig. 1. Circuit diagram of the proposed inherent ZVZCS PS PWM FB converter.

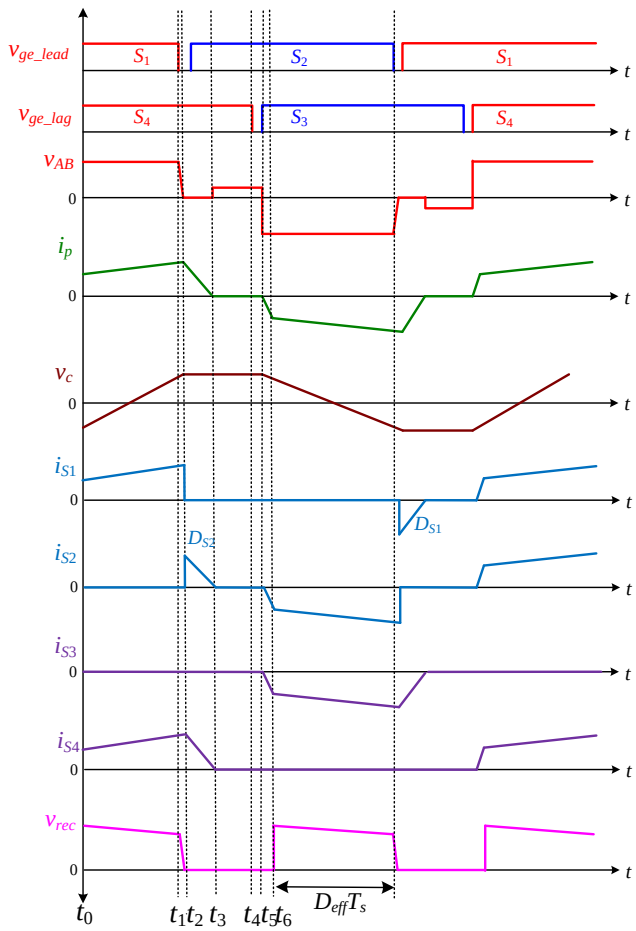

Fig. 2. Key operation waveforms of the proposed converter.

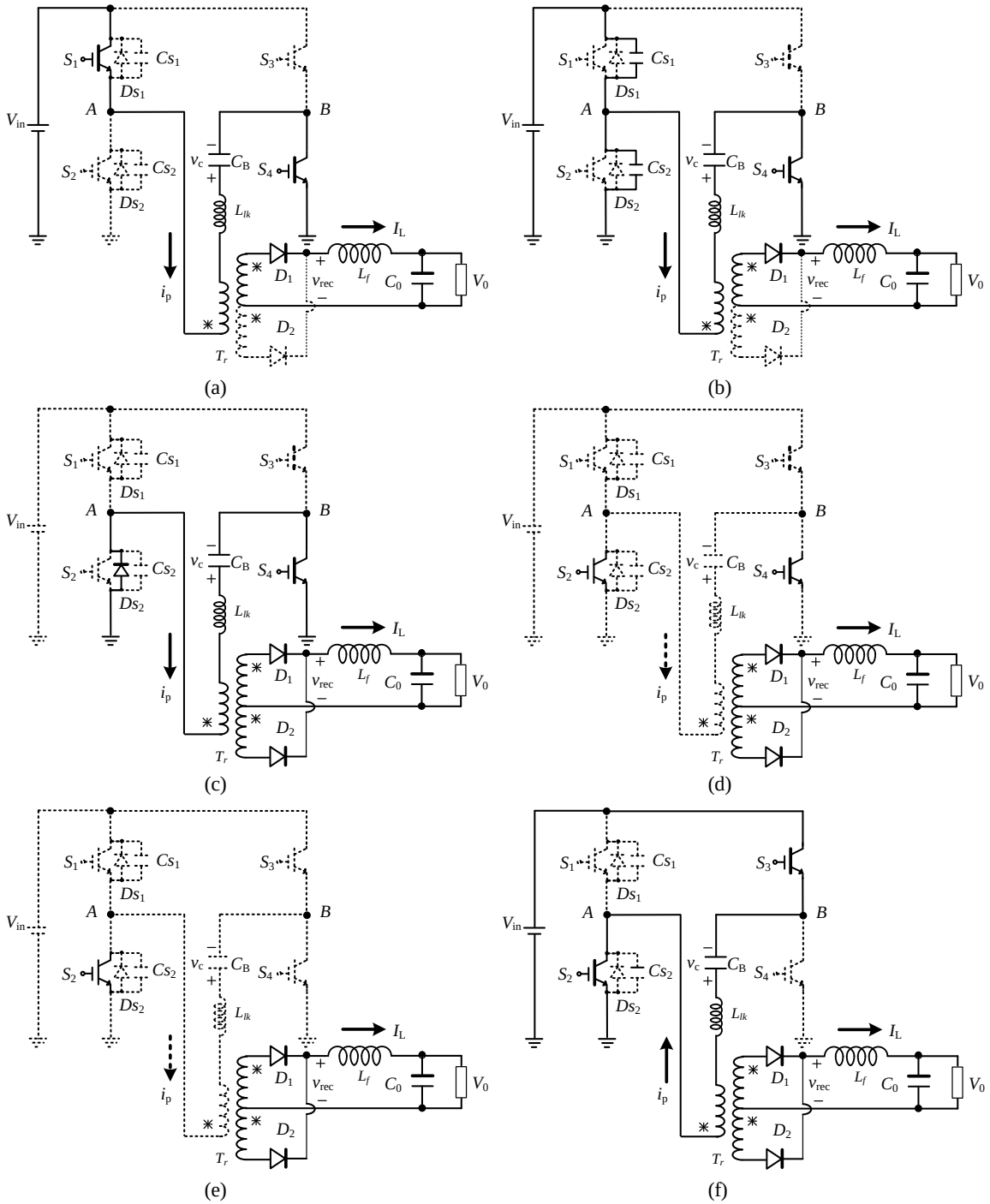

Fig. 3. Operation modes of the proposed converter.

No additional auxiliary ZVZCS circuits are used in the circuit.

The topology operation principles can also be explained by the gate sequences and associated key voltage and current waveforms illustrated in Figs. 1 and 2, where Cs_1 and Cs_2 are the equivalent capacitance of the IGBTs S_1 and S_2 respectively, v_{ge_lag} and v_{ge_lead} are the IGBT drive signals respectively, V_{in} is the input voltage, V_0 is the output voltage, v_{AB} is FB leg middle-point voltage, v_c is the voltage across the blocking capacitor C_B, v_{rec} is the rectifying voltage before the output filter, i_P is the main transformer, T_r is the primary current, I_L is the current through the choke L_f, D_{eff} is the effective duty ratio, and T_s is the switching period.

The topology in the half PWM cycle has six distinct operation modes, as shown Fig. 3. Similar operation principles in the second half PWM cycle are not provided because of the symmetric circuit structure. The following assumptions are made at this point to simplify the analysis.

1) All power devices and components are ideal.
2) The output choke is sufficiently large to be treated as a constant current source during a switching period.
3) $C_{s1} = C_{s2} = C_r$.

Mode [t_0–t_1] [Fig. 3(a)]: S_1 and S_4 conduct while S_2 and S_3 are both deactivated. The input power is delivered from the primary to the output. The primary current $i_p = I_L/n$ charges the blocking capacitor C_B at the same time, where n is the main transformer primary-to-secondary ratio.

Mode [t_1–t_2] [Fig. 3(b)]: S_1 is turned off, whereas S_4 conducts at t_1. The primary i_p (i.e., reflected load current to the primary) charges C_{s1} and discharges C_{s2} linearly. The capacitors provide the ZVS condition for S_1 as follows:

$$v_{ce\_S1}(t) = \frac{I_L}{2nC_r}(t - t_0) \tag{1}$$

$$v_{ce\_S2}(t) = V_{in} - \frac{I_L}{2nC_r}(t - t_0) \tag{2}$$

Mode [t_2–t_3] [Fig. 3(c)]: The primary i_p fully discharges C_{s2} at t_2, and the body or external diode D_{S2} of S_2 is naturally turned on. Thus, S_2 can turn on at the zero-voltage condition during this interval.

v_{AB} is clamped to zero because of the simultaneous conducting of D_{S2} and S_4. Therefore, the blocking capacitor voltage v_c decreases the primary current i_p.

$$i_p(t) = \frac{I_L}{n} - \frac{v_c(t_2)}{L_{lk}}(t - t_2) \tag{3}$$

Given that the reflected secondary i_p cannot supply the constant inductor current i_L, the secondary rectifier diodes D_1 and D_2 both conduct for the freewheeling i_L.

Mode [t_3–t_4] [Fig. 3(d)]: The primary current reaches zero at t_3. Given the RB IGBT, S_4 does not provide i_p the reverse current path, i_p is maintained at zero state during this interval, and a circulating current state occurs for the conventional ZVS PS FB. The zero state also provides the ZCS condition for S_4 to be turned off.

The rectifier diodes D_1 and D_2 still conduct and share the load current in the secondary circuit.

Mode [t_4–t_5] [Fig. 3(e)]: S_4 is turned off at the zero-current condition at t_4. After a short delay of dead time, S_3 can turn on at t_5.

Mode [t_5–t_6] [Fig. 3(f)]: S_3 is turned on by the PWM command at t_5. S_3 is turned on at the zero-current condition because of the leakage inductor L_{lk} that limits the increase in primary current i_p at the negative direction.

$$i_{S3}(t) = -i_p(t) = \frac{V_{in} + v_c(t_2)}{L_{lk}}(t - t_5) \tag{4}$$

The increasing primary current i_p cannot supply the load current during this interval, and both secondary rectifier diodes conduct, which clamps the voltage across the transformer windings at zero.

The primary current i_p reaches the reflected load current to the primary at t_6, and the input voltage source starts to deliver power from the primary to the output such that the second half-cycle starts at t_0.

III. Design Considerations

A. ZVS Range of the Leading Leg

The ZVS transition of the leading- leg is supported by the secondary side filter inductance L_f and the transformer leakage inductance L_{lk}. Thus, the ZVS range of the leading- leg is relatively wide but only limited at light loads, as illustrated below:

$$\frac{1}{2}(L_{lk} + n^2 L_f) I_p^2 > C_r V_{in}^2 \tag{5}$$

B. ZCS Range of the Lagging Leg

The ZCS transition of the lagging- leg is determined as [t_2, t_3] and [t_3, t_4], as shown in Fig. 2, where the primary current must decrease to zero before the PWM signal is applied to the IGBT in the lagging- leg at t_{23}.

Consider the following:

$$v_c(t_2) \approx \frac{I_L}{n}\frac{D_{eff} T_s}{2C_B} \tag{6}$$

where D_{eff} is defined as the effective duty ratio shown in Fig. 2, and T_s is the switching period. Thus, Eq. (3) can be revised as follows:

$$t_{23} = \frac{I_L L_{lk}}{n v_c(t_2)} = \frac{2L_{lk} C_B}{D_{eff} T_s} \tag{7}$$

This condition indicates that t_{23} is independent of the load current and is inversely proportional to D_{eff}. With sufficient D_{eff} that to fulfills the output voltage regulation, the ZCS transition of the lagging- leg can be achieved in the total line input and output load range, including the no -load condition.

C. Circulating Current Elimination

Mode [t_3–t_4] and Fig. 2 show that the primary current reaches zero at t_3 and remains at zero because of the adopted RB IGBTs in the lagging leg, which do not provide i_p to the reverse current path. Therefore, the circulating current does not exit and helps the efficiency improvement.

D. IGBT Selection in the Lagging Leg

Currently, the primary manufacturers of RB IGBTs are Fuji, IXYS, Mitsubishi, and Infineon. These manufacturers all have their own design, so the RB-IGBT architecture depends on the manufacturer. The architecture of an RB-IGBT from IXYS is described in [24]. This company modified an NPT-IGBT by using isolation diffusion and folding up the lower p^+ layer at the chip edge, as shown in Fig. 4. Performing the p^+-n^- junction that blocks the reverse voltage prevents breakthrough at the chip edge. The p^+-n^- junction continues to the isolation layer at the gate connection. These modifications enable the IGBT to block negative collector-emitter voltages as a normal p-n diode

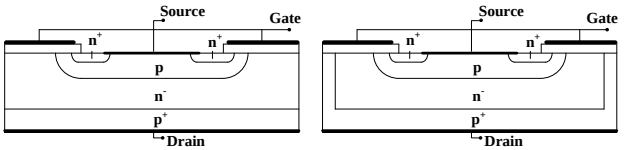

Fig. 4. Architecture of an non-punch-through(NPT) IGBT (left) and IXYS (right). RB-IGBT with an intrinsic diode (right).

and still have the operational behavior of a normal NPT-IGBT. The maximum RB voltage for this device is 1200 V.

Given the limited RB-IGBTs provided in the manufacturers' product category, mass production and cost issues are also concerns for the proposed novel FB converter. The detailed architecture of an IGBT is reexamined at this point. The body-drift region junction in Fig. 5 is the junction that blocks the forward voltage when the device is off, and the junction between the p^+ injection and n^- layers is the junction that blocks the reverse voltage. Thus, the NPT-IGBT can theoretically block a reverse voltage as high as the magnitude of the forward voltage. The NPT-IGBT without a body diode is a possible low-cost solution to replace the RB-IGBT for mass production. The optimization of switching performance of the RB-IGBT is no longer a key issue that makes the RB IGBT still relatively unacceptable in real applications [23]. Common IGBT drivers are sufficient, and the prototype only uses a small driver transformer to drive the NPT-IGBT.

E. Current Sharing Strategy with Multiple Modules

The paralleling of standardized converter modules generally offers several advantages, such as redundancy implementation, expandability of output power, and ease of maintenance. When multi-converter modules operate in parallel, the major issue is load-current sharing among the different modules [25]. Among the different approaches, the democratic current-sharing method is preferred for its autonomous current-sharing feature. A simple, low-cost, and robust democratic current-sharing circuit is introduced at this point with diodes, as shown in Fig. 6. The connecting current bus after the maximum value detection circuit forces the current reference to be the same, which follows the maximum value of the different voltage loop output. The different inner current loop further regulates the module output current independently.

IV. Control Loop Design for Voltage and Current Regulations

The proposed ZVZCS FB converter is used as a downstream main circuit of a marine lead-acid battery charger whose front-end converter is a three-phase passive rectifier. The constant current (CC) and constant voltage (CV) charge modes are preferred for a lead-acid battery [26]. Therefore, the control loops for the voltage and current regulations should be carefully designed [27], [28].

The battery model is complicated because of its

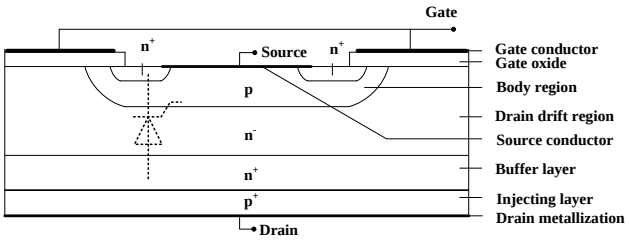

Fig. 5. Detailed architecture of an IGBT.

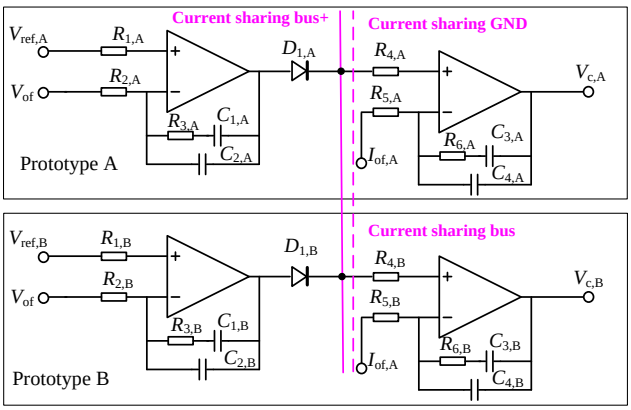

Fig. 6. Current-sharing circuit.

electrochemical feature under charge/discharge management. One approach is to model the battery as an equivalent resistor in charging mode, while another approach models the battery as a DC source with its series resistor. Major loop design differences between these models occur at the low-frequency stage. Key factors such as crossover frequency are unaffected [29]. Consider that an electronic load-based battery emulator is used in this study for convenience. Thus, the lead-acid battery is modeled as an equivalent resistor.

Finally, the real lead-acid battery is further used to reexamine the controller.

Fig. 7 illustrates that several small-signal transfer functions are defined as follows:

Current loop gain before compensation:

$$T_{i\_ol}(s) = K_i(s)F_m(s)G_{iLd}(s) \tag{8}$$

Current loop gain after compensation:

$$T_i(s) = K_i(s)G_i(s)F_m(s)G_{iLd}(s) \tag{9}$$

Modulator can be modeled by a constant gain:

$$F_m(s) = 1/V_{pp} \tag{10}$$

where V_{pp} = 2.35 V is the peak-to-peak voltage of the triangular carrier signal.

$G_{vd}(s)$ is the duty-ratio-to-output-voltage transfer function.

$$G_{vd}(s) = \frac{\hat{v}_0(s)}{\hat{d}(s)}\bigg|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_0(s)=0}} = \frac{nV_{in}R}{(R+R_L)} \frac{SR_CC_0+1}{S^2\frac{LC(R+R_C)}{(R+R_L)}+S(\frac{R_LRC+R_CRC+R_LR_CC+L}{R+R_L})+1} \tag{11}$$

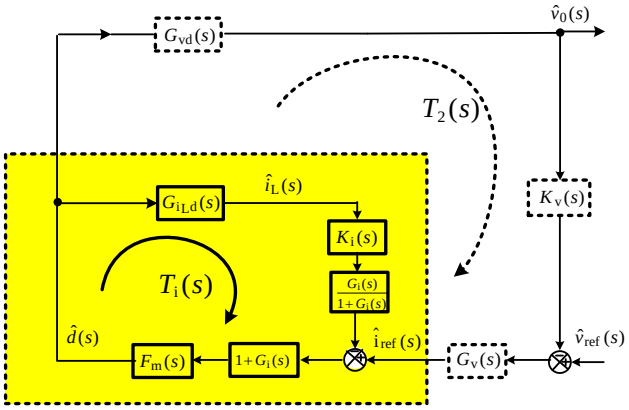

Fig. 7. Control loop block.

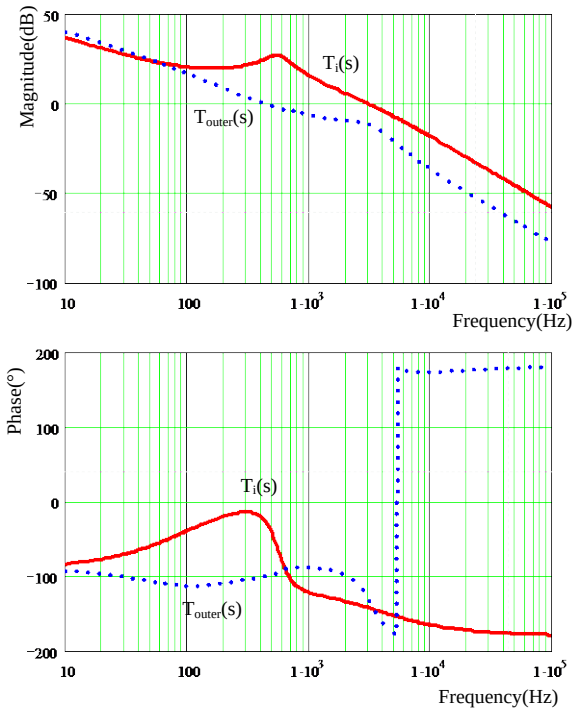

Fig. 8. Loop gains after compensation.

$G_{iLd}(s)$ is the duty-ratio-to-inductor-current transfer function shown in Eq. (12):

$$G_{iLd}(s)=\left.\frac{\hat{i}_L(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_{in}(s)=0\\ \hat{i}_0(s)=0}} =\frac{nV_{in}}{(R+R_L)}\frac{s\cdot(R_0+R_C)C_0+1}{S^2\frac{LC(R+R_C)}{(R+R_L)}+S(\frac{R_LRC+R_CRC+R_LR_CC+L}{R+R_L})+1} \quad (12)$$

$G_i(s)$ is the inner-loop compensation gain:

$$G_i(s)=\frac{(R_6+\frac{1}{C_3\cdot s})//\frac{1}{C_4\cdot s}}{R_5}\quad (R_5=R_4) \quad (13)$$

$G_v(s)$ is the outer-loop compensation gain:

$$G_v(s)=\frac{(R_3+\frac{1}{C_1\cdot s})//\frac{1}{C_2\cdot s}}{R_2}\quad (R_1=R_2) \quad (14)$$

$K_v(s)$ = 0.1 is the output voltage sense gain, $K_i(s)$ = 0.1 is the current sense gain, D is the FB converter duty ratio, L_f is the inductance, C_0 is the output capacitor, R is the load resistance, R_C is the equivalent series resistance of the output capacitor, and R_L is the equivalent series resistance of the inductor in these transfer functions.

We selected the current loop crossover frequency after compensation f_{ci} = 0.1-0.2f_s in these transfer functions. We then placed the zero f_{z1} of $G_i(s)$ at the output resonance frequency f_0 for damping and pole f_{p1} = f_s/10 for switching ripple elimination.

At this point, the current loop gain magnitude at f_{ci} before compensation is $\left|T_{i\_o1}(j\cdot 2\pi f_c)\right| dB$, which indicates that the compensation gain should be as follows:

$$Av=10^{-\left|T_{i\_o1}(j\cdot 2\pi f_C)\right|/20} \quad (15)$$

which ensures that the current loop gain magnitude at f_{ci} after compensation is zero.

Furthermore,

$$R_6=Av\cdot R_5 \quad (16)$$

$$C_3=\frac{1}{2\pi R_6 f_{z1}} \quad (17)$$

$$C_4=\frac{C_3}{2\pi C_3 R_6 f_{p1}-1}\approx\frac{1}{2\pi R_6 f_{p1}} \quad (18)$$

Considering the component tolerances, the resistors and capacitors whose values are near the calculated ones are selected and then reexamined by the Bode plots, as shown in Fig. 8. The current loop crossover frequency is f_{ci} = 2.9 kHz, and the phase margin is 40°, which means that the current loop has a suitable stable and dynamic performance.

After the current loop is closed, the inner loop is used as a power stage as follows:

$$A_p(s)=(1+G_i(s))F_m(s)/(1+T_i(s)) \quad (19)$$

The outer loop gain before compensation is as follows:

$$T_{outer\_ol}(s)=A_p(s)G_{vd}(s)K_v(s) \quad (20)$$

The outer loop controller and outer loop gain can be designed similar to the previously mentioned gains. The outer loop gain after compensation is described as shown in Eq. (21), and more information is provided in Fig. 8.

$$T_{outer}(s)=G_i(s)\,A_p(s)G_{vd}(s)K_v(s) \quad (21)$$

(current loop cross over frequency f_{ci} = 2.9 kHz, PM = 40°, R_4 = R_5 = 10 kΩ, R_6 = 6.2 kΩ, C_3 = 47 nF, C_4 = 13 nF; outerloop crossover frequency f_{cv} = 390 Hz, PM = 80°, R_1 = R_2 = 10 kΩ, R_3 = 30 kΩ, C_1 = 9.1 nF, C_2 = 2.7 nF)

V. Experimental Verification

A. Hardware Description

A 1.2 kW hardware prototype for a marine battery charger was designed, fabricated, and tested to verify the proposed converter and current-sharing strategy. The final charger

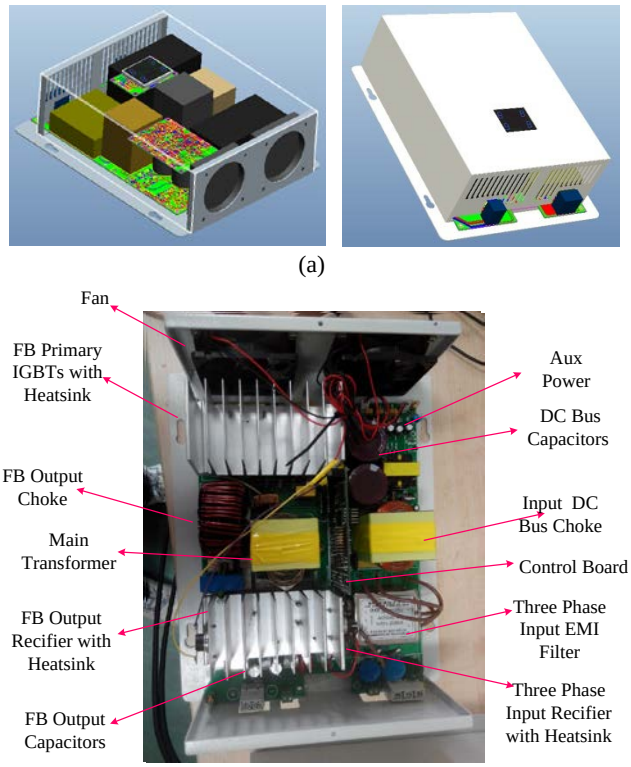

Fig. 9. Prototype photograph. (a) 3D view of the virtual prototype. (b) Interior of the actual prototype.

TABLE I
OPERATION CONDITIONS AND CIRCUIT PARAMETERS

Input voltage v_{ac}	380 V/50 Hz
Dc bus voltage V_{in}	540 V
Input dc bus choke	Ferrite EE55(2 pcs in parallel), 14 mH
Input dc bus capacitor	470 μF/450 V (2 pcs in series)
Output voltage V_0/current I_0	18 –28 V/0–40 A
Switching frequency f_s	25 kHz
IGBT in leading-leg S_1, S_2	SKW15N120 (1 pcs)
IGBT in lagging-leg S_3, S_4	IGW15N120 (1 pcs)
Rectifier diode D_1, D_2	STPS60150C (1 pcs)
Main transformer	Ferrite EE55 (2 pcs in parallel), 28:2:2
Transformer leakage inductance L_{lk}	13 μH
Blocking capacitor C_B	1 μF
Output choke L_f	Kool Mu 77192–A7 33 μH (2 pcs in parallel)
Output capacitor C_0	1200 μF/35 V (2 pcs in parallel)

product started its type test. Detailed specifications and parameters are shown in Fig. 9 and Table I. A single-chip Atmega64 controller provides the voltage and current reference for battery charge management, while a TI UCC3895 IC controls the FB circuit.

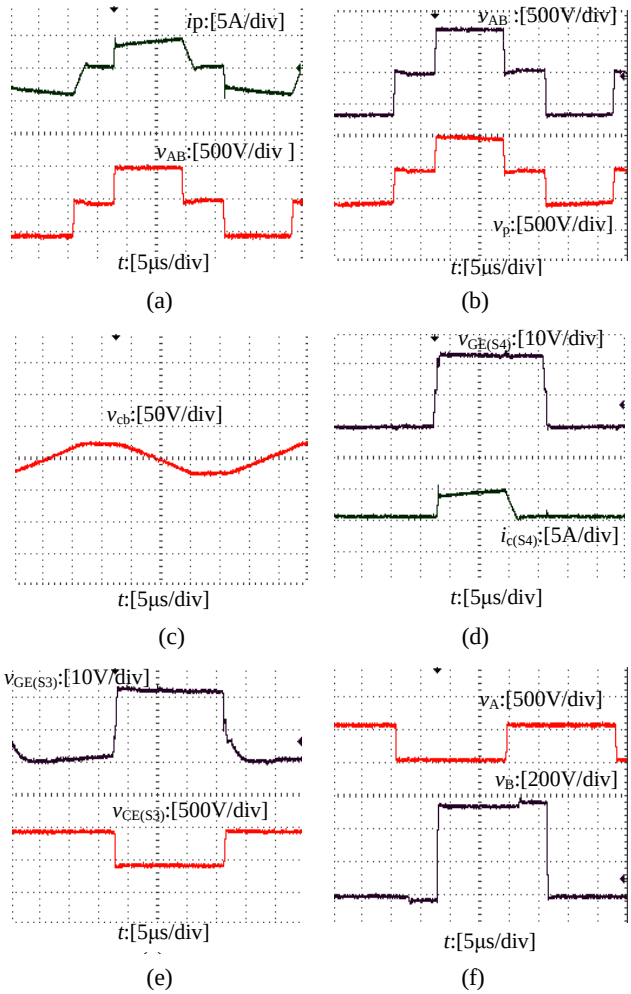

Fig. 10. Experimental results.

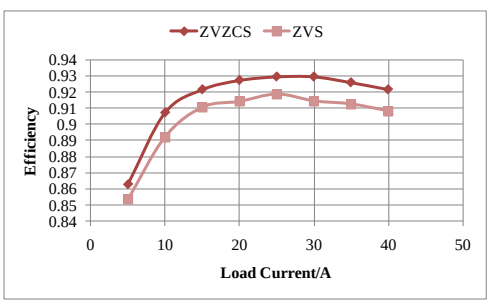

Fig. 11. Efficiency curve.

B. Experimental Key Waveforms

Fig. 10 provides the detailed experimental results of the topology shown in Fig. 2. The fast reset of the primary current is observed in Fig. 10(a), which implies that the circulating current is eliminated, thus helping in efficiency improvement.

Fig. 10(b) illustrates the FB primary middle-point voltage and transformer primary voltage. The difference between the voltage drops in the blocking capacitor C_B is shown in Fig. 10(c).

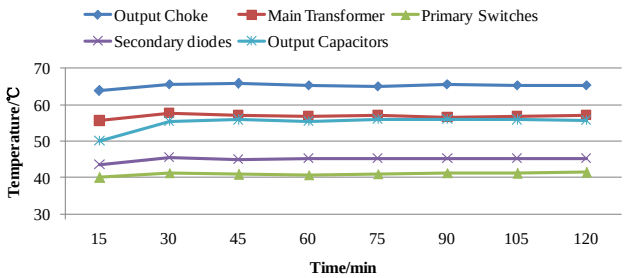

Fig. 12. Prototype devices with hot-spot temperature curves (ambient temperature: 25 ℃).

TABLE II
DATA OF PARALLEL CURRENT SHARING

Output Current-A	Output Current-B	I_{AVG}	I_{ERROR}	Error%
5.71 A	5.46 A	5.585 A	0.25 A	4.4%
7.82 A	7.35 A	7.485 A	0.47 A	6%
12.4 A	11.8 A	12.05 A	0.6 A	4.9%
15.5 A	14.7 A	15.1 A	0.8 A	5%
40.2 A	39.8 A	40 A	0.4 A	1%

TABLE III
EVALUATION CONDITIONS AND RESULTS

Possible Candidates	Primary Main Circuit Features	Auxiliary Circuit Features	Reported test results			Complexity		Cost
			Input voltage	Output voltage	Maximum efficiency	Circuit	Control	
[1]	4 MOSFETs, 2 diodes, 1 inductor	1 transformer	380 Vdc	48 Vdc	93.5%	high	PS PWM	high
[2]	4 MOSFETs	0	400 Vdc	48 Vdc	93.12%	low	PS PWM	lowest
[3]	4 MOSFETs	1 inductor	400 Vdc	48 Vdc–56 Vdc	94.5%	low	resonant	low
[4]	4 IGBTs	1 inductor, 4 capacitors	640 Vdc	27.5 Vdc	94%	low	PS PWM	medium
[5]	2 MOSFETs, 2 IGBTs, 1 extra transformer	1 inductor, 3 capacitors, 3 diodes	390 Vdc	385 Vdc	98%	highest	hybrid resonant and PS PWM	highest
[6]	4 MOSFETs, 1 extra transformer	3 capacitors, 6 diodes	380 Vdc–400 Vdc	420 Vdc	98.6%	highest	hybrid resonant and PS PWM	highest
[7]	4 IGBTs	2 capacitors, 3 diodes	280 Vdc	120 Vdc	96.5%	High	PS PWM	low
[8]	4 IGBTs	2 diodes	537 Vdc	54 Vdc	94.3%	low	PS PWM	low
[9]	4 MOSFETs	1 capacitor, 4 diodes	42 Vdc	–	94.3%	medium	PS PWM	low
[10]	4 IGBTs	1 inductor, 1 capacitor, 3diodes	250 Vdc–350 Vdc	50 Vdc	94.8%	medium	PS PWM	medium
[11]	4 MOSFETs, 2 diodes, 1 inductor	1 transformer, 2 diodes	270 Vdc	54 Vdc	93.4%	medium	PS PWM	high
[12]	4 IGBTs	2 MOSFETs, 4 diodes, 2 inductors, 2 capacitors,	325 Vdc	45 Vdc	94%	highest	an innovative control algorithm [12]	highest
[13]	4 MOSFETs	4 Si diodes, 4 SiC diodes	358.33 Vdc	402.9 Vdc	95%	low	Open loop	highest
[14]	4 IGBTs	0	200 Vdc	14 Vdc	93.7%	low	PS PWM + synchronous rectification	medium
[15]	4 MOSFETs, 2 diodes, 1 capacitor	1 diode with tapped-inductor	540 Vdc	25 Vdc	91.4%	highest	PS PWM	medium
Proposed Topology	4 IGBTs	0	540 Vdc	28 Vdc	93%	lowest	PS PWM	lowest

Fig. 10(d) shows the ZCS operation of the IGBTs in the lagging leg with load current adaptability. Notably, the device current drops to zero at the light-load condition before the gate signal is turned off. Thus, the ZCS is achieved at this point, although the ZVS condition of the lagging leg is still not obtained as shown in Fig. 10(e). Fig. 10(f) shows the test using the simple phase-shift modulation method.

C. Experimental Data and Discussion

Fig. 11 further provides the efficiency curve of the prototype. The expected high efficiency is guaranteed because of the topology with intrinsic soft switching and eliminated circulating current features. The maximum efficiency is approximately 93% under 540 Vdc input and 28 Vdc output condition, where auxiliary power and fan losses are also included.

The decrease in efficiency for currents of 30 A up to 40 A is caused by conduction losses, especially the output rectifying diodes. The impact of conduction losses is highly significant in converters with low output voltage and high output current, such as in our case. In addition, no energy recovery circuits are added in the converter to clamp rectify diode voltage spikes and to achieve forward and reverse recovery current optimization.

Nevertheless, the efficiency is relatively high, unlike the ZVS FB converter in Fig. 11. The only differences between these converters are that the IGBTs without body diodes in the lagging leg use the same devices with body diodes in the leading leg. High-output voltage and low-output current will be higher, especially in the case where the synchronous rectification technique or lossless energy recovery clamp circuits are introduced [30].

Fig. 12 shows the hot-spot temperature curves of the prototype devices. Thermal balance is achieved after 30 min of work. The maximum temperature increase is approximately 20 °C for primary switches and secondary diodes. The hottest component is the output choke, which is insensitive to the heat.

Table II further summarizes the current distribution for a parallel connection of two prototype modules. The current-sharing accuracy is in the 1% to 6% range in the entire load range with the current-sharing bus connected. Even at a light-load condition, the current distribution is insensitive to the noise. The error is mainly caused by the mismatching in circuit power stages because the sharing bus provides the same DC current reference. The implementation of the true $N + 1$ redundant system can then be conducted [25].

Table III further provides a comparative study of the possible prototype candidates. The proposed topology exhibits a suitable balance between performance and cost for industry application with the least components and devices in different possibilities.

VI. CONCLUSIONS

A novel inherent ZVZCS PS FB converter is proposed in this paper. The operation principles, specific design considerations, and experimental results are presented. The distinctive features of the proposed topology are summarized as follows.

1) The ZVS transition of the leading leg is supported by the secondary side filter inductance L_f and the transformer leakage inductance L_{lk}. Thus, the ZVS range of the leading leg is relatively wide.
2) The ZCS transition of the lagging leg and minimized circulating current can be achieved in the total line input and output load range through the use of IGBTs with the RB feature. Therefore, the turn-off and conduction losses of the IGBTs are significantly lowered.
3) The NPT-IGBT without a body diode can be a low-cost solution to replace RB IGBT for mass production. The optimization of switching performance of the RB IGBT is no longer a key issue that makes RB IGBT unacceptable in real applications. Common IGBT drivers are sufficient.
4) The low topology-complexity FB converter without any auxiliary circuit can be easily controlled with a simple PS PWM control strategy. A simple, low-cost, and robust democratic current-sharing circuit is introduced and verified in this study, which offers redundancy implementation, expandability of output power, and ease of maintenance features. This converter is an attractive alternative for compact and cost-effective applications with high-voltage input.

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