JPE 15-3-2

http://dx.doi.org/10.6113/JPE.2015.15.3.587
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

High Step-up Active-Clamp Converter with an Input Current Doubler and a Symmetrical Switched-Capacitor Circuit

Liangzong He*, Tao Zeng†, Tong Li*, Yuxian Liao*, and Wei Zhou*

*†Department of Mechanical and Electrical Engineering, Xiamen University, Xiamen, China

Abstract

A high step-up dc-dc converter is proposed for photovoltaic power systems in this paper. The proposed converter consists of an input current doubler, a symmetrical switched-capacitor doubler and an active-clamp circuit. The input current doubler minimizes the input current ripple. The symmetrical switched-capacitor doubler is composed of two symmetrical quasi-resonant switched-capacitor circuits, which share the leakage inductance of the transformer as a resonant inductor. The rectifier diodes (switched-capacitor circuit) are turned off at the zero current switching (ZCS) condition, so that the reverse-recovery problem of the diodes is removed. In addition, the symmetrical structure results in an output voltage ripple reduction because the voltage ripples of the charge/pump capacitors cancel each other out. Meanwhile, the voltage stress of the rectifier diodes is clamped at half of the output voltage. In addition, the active-clamp circuit clamps the voltage surges of the switches and recycles the energy of the transformer leakage inductance. Furthermore, pulse-width modulation plus phase angle shift (PPAS) is employed to control the output voltage. The operation principle of the converter is analyzed and experimental results obtained from a 400W prototype are presented to validate the performance of the proposed converter.

Key words: Input current doubler, High step-up converter, Switched-capacitor

I. INTRODUCTION

Recently, photovoltaic (PV) power systems has become an attractive candidate due to the increases in energy demand and the concern over environmental pollution around the world. Various kinds of configurations are being developed in grid-connected systems. Generally, a system can be employed as a small-scale distributed generation (DG) system, where the most important design constraint of the PV DG system is to obtain a high voltage gain. For a typical PV module, the open-circuit voltage is about 21~28 V [1], [2]. However, the public DC bus voltage is usually set to 200V or 400V [3], [4]. Therefore, a high step-up dc-dc converter with a high voltage conversion ratio, a low input-current ripple, a low output-voltage ripple and a high efficiency is required to realize the grid-connected function and to achieve a low total harmonic distortion (THD).

Until now, various current-fed step-up conversion topologies have been proposed in photovoltaic (PV) power systems [6]-[10]. These topologies have desirable advantages such as a high voltage conversion ratio, a low input current ripple, a high power capability and galvanic isolation between the input and output sides. However, they have a common serious problem caused by the leakage inductance of the transformer. It is well known that converters with a power transformer suffer high voltage surges across the switches in current-fed topologies such as the current-fed push-pull converter, current-fed full-bridge converter and current-fed half bridge converter. Thus, a snubber circuit is required to absorb the surge energy to protect the switching devices from a permanent breakdown. Moreover, in current-fed power conversion topologies, the snubber circuit has to accommodate the entire boost current until the transformer leakage inductor current is built up to the level of the boost inductor current. Hence, a well-designed snubber circuit is essential for solving these problems. However this greatly increases the circuit design complexity and cost. Most importantly, because the rectifier diodes are

Manuscript received May 30, 2014; accepted Jan. 9, 2015
Recommended for publication by Associate Editor Bor-Ren Lin.
†CorrespondingAuthor: tao.zeng@xmu.edu.cn
Tel: +82-2-554-0185,Fax: +82-2-554-0186, Xiamen University
*Dept. of Mechanical & Electrical Eng., Xiamen University, China

turned off at hard switching, the exiting reverse-recovery problem will shade the efficiency improvement [11]-[14].

Many voltage-fed converters have also been proposed with step-up dc-dc topologies for high gain [15]-[19]. However, these voltage-fed converters may not be optimal due to a large input current ripple, which is not beneficial for MPPT control. Reducing the input current ripple in a voltage-fed converter requires an additional LC filter across the photovoltaic cell stack, which lowers the power efficiency. Additionally, a high frequency transformer with a high turns ratio is required, which increases the voltage stress on the primary elements, and imposes a heavy penalty on the efficiency. As with the current-fed topologies, the reverse-recovery problem is not solved.

Based on those considerations, some resonant converters have been proposed [20]-[22]. However, some disadvantages prevent their popularity. Even the dual resonant circuit applications in [20], [21] produce a double output voltage, and two windings are required for the transformer which results in design complexity and a bottleneck for power density. The authors of [22] provide an ingenious method to achieve a high step-up through a resonant circuit. Unfortunately, the primary inverter bridge fails to realize the soft switching and a transformer with a high turns-ratio is required. Recently, a novel class of resonant converters including the serial resonant converter (SRC), parallel resonant converter (PRC) and series parallel resonant converter (SPRC, also known as an LCC resonant converter) has been developed [23]-[25]. By adjusting the frequency, these resonant circuits can realize ZCS for all of the rectifier diodes, and voltage/current spikes can be suppressed in the primary switches due to a sinusoidal current though the switches instead of a square current. In addition, these circuits enjoy a relative high efficiency. However, some drawbacks limit their wide application:

1) The drifting of component parameters such as the transformer parasitic parameters including the stray inductors in wires and the layout of components can lead to difficulties in resonant loop design.
2) For the SRC, the large frequency change to maintain the output regulation becomes a serious drawback especially in no load or light load conditions. For the PRC, the light load efficiency is very low.
3) The conversion ratio is confined. For the SRC, the maximum is 1. For the SPRC, the design complexity is increased when compared to SRC or PRC. As a result, high turn ratio transformers are required to attain a high gain, which shades their advantages.
4) At the same power factor, the amplitude of the sinusoid current is 3~4 times the square current. This introduces the main switches to a serious radio frequency interface (RFI) problem.

To solve above problems mentioned, a novel isolated converter with an input current doubler, a resonant switched-capacitor circuit and an active-clamp circuit is proposed in this paper. The operation of the proposed converter is analyzed in section II, and the control scheme is described in section III. Then, the performance is discussed in section IV. Finally, some experimental results and waveforms are presented to verify the performance of the proposed converter in section V.

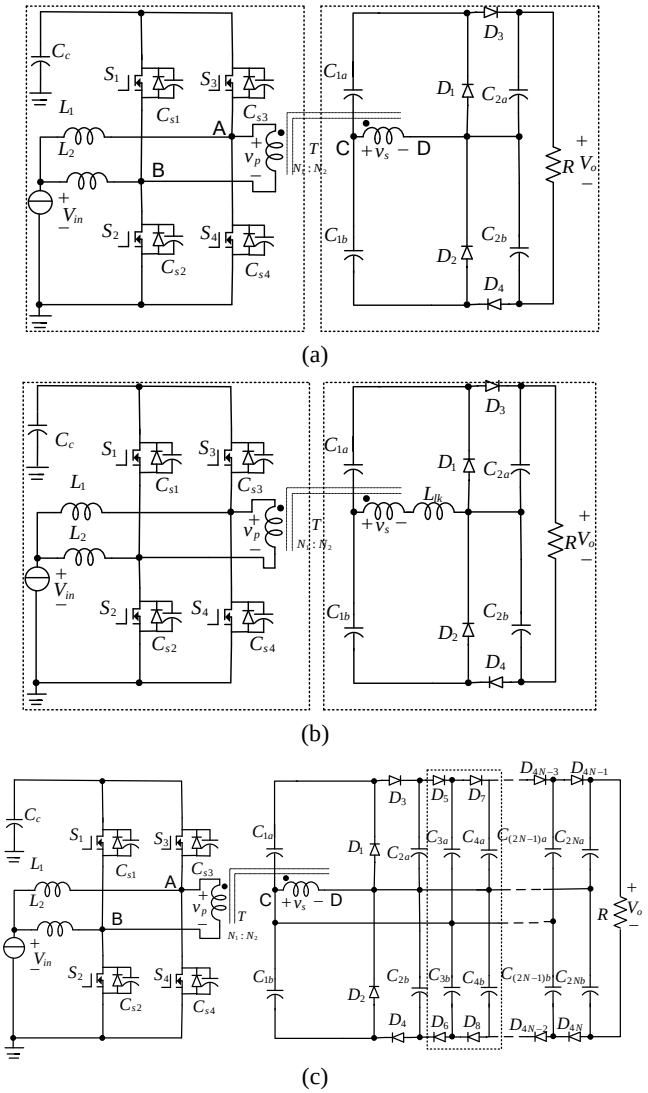


Fig. 1. Proposed converter and its equivalent circuit. (a) Proposed converter. (b) Simplified circuit model. (c) Voltage-level-extension topology with N SC blocks.

II. Proposed Converter and Operation Principle

The proposed converter and its simplified circuit model are shown in Fig. 1. It is composed of a current doubler and a switched-capacitor circuit. The current doubler circuit is plotted in the left dashed block of Fig. 1. Two out-of-phase pulses with an adjustable width are supplied to drive the main switches S_2 and S_4. The auxiliary switches S_1, S_3 are driven

complementarily by the main switches S_2, S_4, respectively. The inductors L_1, L_2 are connected to the main switches S_2, S_4, respectively. The active-clamp circuit is composed of the clamp capacitor C_c and the auxiliary switches S_1, S_3. The switched-capacitor circuit is plotted in the right dashed block of Fig. 1, which is composed of the rectifier diodes D_1, D_2, D_3, D_4 and the capacitors C_{1a}, C_{1b}, C_{2a}, C_{2b}. This circuit provides two complementary series-resonant loops to achieve the ZCS turn-off for all the rectifier diodes. One loop is the transformer leakage inductance L_{lk} resonating with C_{1a}, and the other loop is the transformer leakage inductance L_{lk} resonating with C_{1b}.

By adding a different number of the SC blocks, which functions as a rectifier, as shown in the dotted box in Fig.1(c), the voltage-level-extension topology can be obtained. For every block that is added to the converter, 4 times v_s will be added to the output voltage, where 4 diodes and 4 capacitors are utilized. Assume that the various rectifiers output the same power and the same voltage. The voltage on the primary-winding of the transformer is V_p, the output voltage is V_o and V_o=4V_p, and output current is I_o. A performance comparison between the SC rectifier and conventional rectifiers (a full bridge rectifier and a full wave rectifier) is shown in Table I.

From Table I, it can be concluded that the proposed SC rectifier benefits in terms of the turn ration of the transformer when compared with conventional rectifiers. Meanwhile, lower voltage stress of the diodes, soft switching realization for the diodes and less output voltage ripple make the proposed SC rectifier a better candidate for rectification.

To analyze the stead-state operation of the proposed converter, several assumptions are made during one switching period T_s.

1) The magnetizing current is nearly zero because the magnetizing inductance is relatively large and bi-directionally excited. Therefore, the magnetizing inductance can be neglected and the transformer T is modeled as an ideal transformer with a leakage inductance L_{lk}.
2) The main switches S_2, S_4 and the auxiliary switches S_1, S_3 are operated by the dual asymmetrical pulse-width modulation method with a short dead time. Assume that the duty cycle of the main switches S_2, S_4 is D. The switches S_1, S_3 work complementarily with the switches S_2, S_4. The details are discussed in section III.
3) All of the switches S_1-S_4 are considered to be ideal switches with body diodes Ds1-Ds4 and parallel capacitances C_{s1}-C_{s4}.
4) The ripple component of the clamp-capacitor voltage v_{Cc} is negligible because the clamp capacitor C_c has a relatively large value.
5) The capacitance of the resonant capacitors C_{1a}, C_{1b} are identical (C_{1a}=C_{1b}=C_1). The output capacitors C_{2a}, C_{2b} have the same value (C_{2a}=C_{2b}=C_2). In addition, the capacitance of the output capacitors is larger than that of the resonant capacitors. Furthermore, the equivalent series resistance (ESR) of the capacitors is assumed to be zero.

TABLE I
PERFORMANCE COMPARISON BETWEEN SC RECTIFIER AND CONVENTIONAL RECTIFIERS

Rectifier circuit	SC rectifier	Full-bridge rectifier	Full-wave rectifier
Number of diodes	4	4	2
Turn ration of transformer	1:1	1:4	1:8
Diode current rating	I_o	I_o	I_o
Diode average current	$0.5I_o$	$0.5I_o$	$0.5I_o$
Diode voltage rating	$2V_p$	$4V_p$	$8V_p$
Soft switching	Yes	No	No
Forward voltage overshoot	Small	Large	Large
Reverse recovery current	Small	Large	Large
Output voltage ripple	Low	High	High

The steady-state operation of the proposed converter during one switching period T_s can be divided into ten stages. The equivalent circuits and the key waveforms in each operation stage are described in Fig. 2 and Fig. 3, respectively.

Stage 1 [t_0, t_1]: At t_0, S_4 is turned on. Then, the inductor current i_{L1} flows through S_4, and the inductor current i_{L2} flows through S_2. Since both of the main switches S_2, S_4 are in the on-state, the primary voltage v_p of the transformer is zero. In addition, both the primary current of the transformer i_p and the secondary current of the transformer is are zero. Then, the inductor currents i_{L1}, i_{L2} increase linearly as follows:

$$i_{L1}(t) = i_{L1}(t_0) + \frac{V_{in}}{L_1}(t - t_0) \quad (1)$$

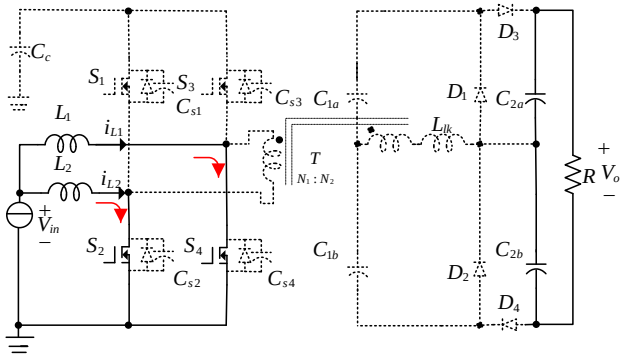
$$i_{L2}(t) = i_{L2}(t_0) + \frac{V_{in}}{L_2}(t - t_0) \quad (2)$$

Where, V_{in} is the output voltage of a photovoltaic battery.

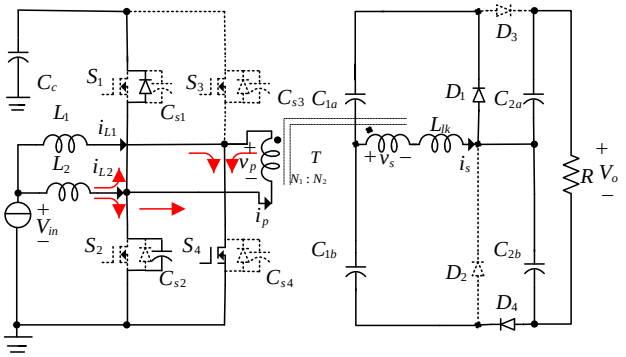
Stage 2 [t_1, t_2]: At t_1, S_2 is turned off. i_{L2} begins to discharge C_{s1} and charge C_{s2} linearly. After i_{L2} fully charges C_{s2} to V_{Cc}, and C_{s1} discharges to 0 V, it flows through the anti-parallel diode of the switch S_1. Therefore, the zero voltage across S_1 is maintained, and the switch S_1 can be turned on at ZVS in the next stage.

During this stage, the input power is transferred to the output side. Since the voltage across the primary winding of the transformer is v_p =-V_{Cc}, the secondary winding voltage is:

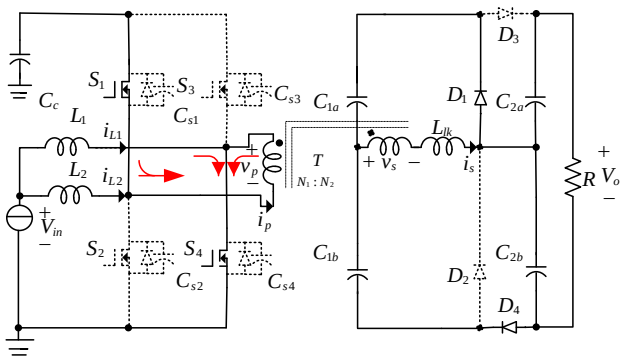
$$v_s = -N \cdot V_{Cc} \quad (3)$$


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
T
$N_1 : N_2$
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

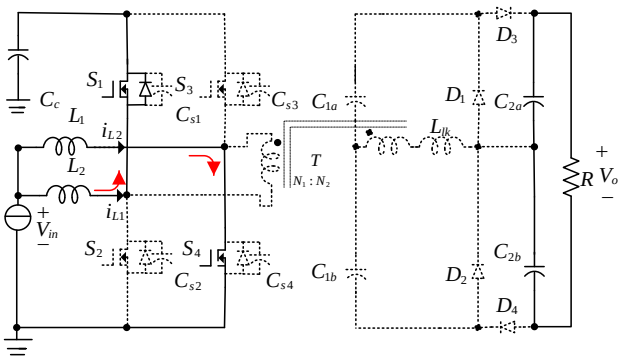
(a)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
v_p
T
$N_1 : N_2$
v_s
i_s
i_p
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

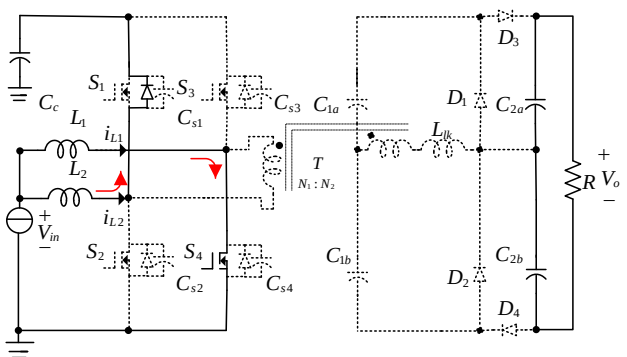
(b)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
v_p
T
$N_1 : N_2$
v_s
i_s
i_p
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

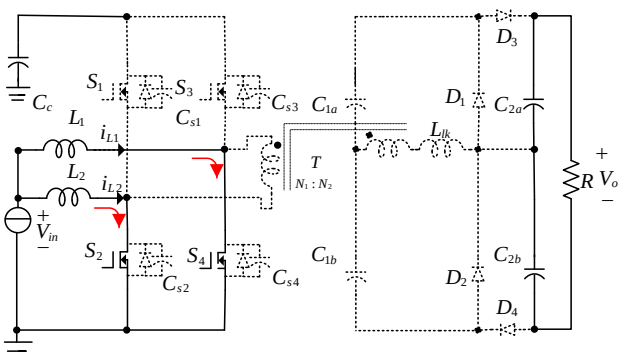
(c)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L2}
L_{lk}
L_2
i_{L1}
T
$N_1 : N_2$
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

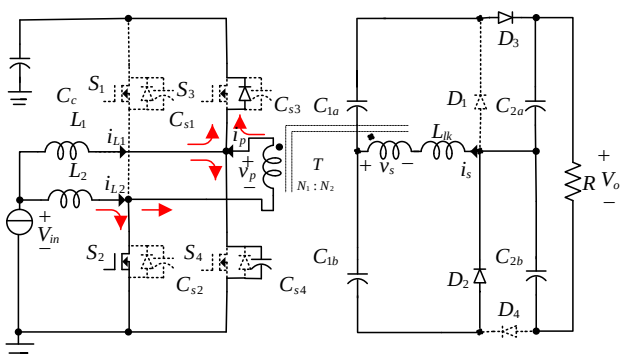
(d)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
T
$N_1 : N_2$
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

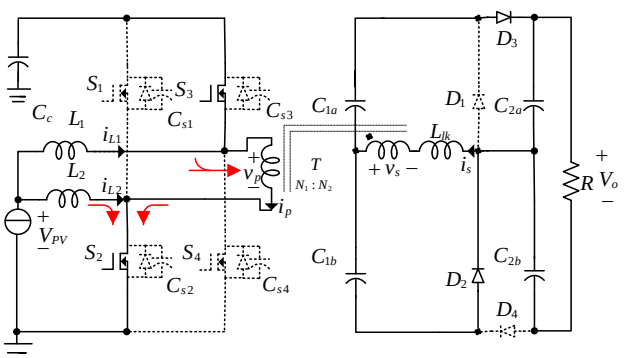
(e)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
T
$N_1 : N_2$
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

(f)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
i_p
L_{lk}
L_2
i_{L2}
v_p
T
$N_1 : N_2$
v_s
i_s
V_{in}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

(g)


C_c
S_1
S_3
C_{s1}
C_{s3}
C_{1a}
D_1
D_3
C_{2a}
L_1
i_{L1}
L_{lk}
L_2
i_{L2}
v_p
T
$N_1 : N_2$
v_s
i_s
i_p
V_{PV}
R
V_o
S_2
S_4
C_{s2}
C_{s4}
C_{1b}
D_2
D_4
C_{2b}

(h)

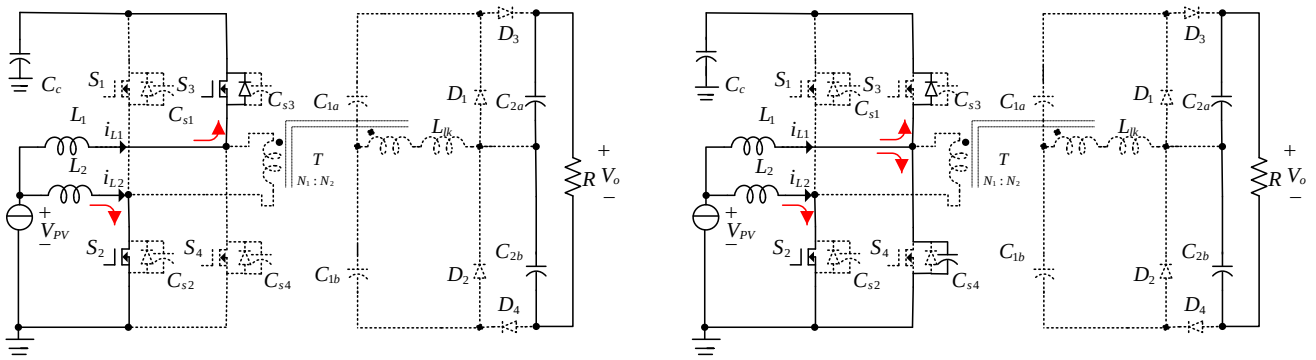


Fig. 2. Operation stages of the proposed converter. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6. (g) Stage 7. (h) Stage 8. (i) Stage 9. (j) Stage 10.

Where, the turns ratio N of the transformer is given by N2/N1. There are two resonant loops. One is the leakage inductor L_{lk}, C_{1a}, D_1 and the other one is L_{lk}, C_{1b}, D_4, C_{2b}. The resonant capacitors C_{1a} is charged by v_s. At the same time, v_s and C_{1b} in series charge C_{2b}. Both D_1, D_4 conduct. The state equations can be written as follows:

$$N \cdot V_{Cc} = v_{C1a}(t) + L_{lk}\frac{di_s(t)}{dt} \tag{4}$$

$$i_s = 2 \cdot C_1 \frac{dv_{C1a}(t)}{dt} \tag{5}$$

Here, i_s, v_{C1a} and v_{C1b} are obtained as follows:

$$v_{C1b}(t) = N \cdot V_{Cc} + [N \cdot V_{Cc} - v_{C1a}(t_1)]\cos\omega_r(t - t_1) \tag{6}$$

$$v_{C1a}(t) = N \cdot V_{Cc} - [N \cdot V_{Cc} - v_{C1a}(t_1)]\cos\omega_r(t - t_1) \tag{7}$$

$$i_s(t) = \frac{V_{Cc} - v_{C1a}(t_1)}{Z_r}\sin\omega_r(t - t_1) = I_{s,peak}\sin\omega_r(t - t_1) \tag{8}$$

Where, $I_{s,peak}$ is the peak current of the secondary transformer. The angular frequency ω_r and the resonant impedance Z_r are given by:

$$\begin{cases} \omega_r = \dfrac{1}{\sqrt{2 \cdot L_{lk} \cdot C_1}} \\ Z_r = \sqrt{\dfrac{L_{lk}}{2 \cdot C_1}} \end{cases} \tag{8}$$

i_{Cc} can be easily obtained as:

$$i_p(t) = N \cdot i_s(t) = N \cdot I_{s,peak}\sin\omega_r(t - t_1) \tag{9}$$

$$i_{Cc}(t) = I_{L2} - N \cdot I_{s,peak}\sin\omega_r(t - t_1) \tag{10}$$

***Stage 3 [t_2, t_3]*:** At t_2, S_1 is turned on while its body diode conducts. Hence, the switch S_1 is turned-on at the ZVS condition. i_{L1} increases continuously as in (1), and i_{L2} decreases linearly as follows:

$$i_{L2}(t) = i_{L2}(t_2) + \frac{V_{Cc} - V_{in}}{L_2}(t - t_2) \tag{11}$$

The two resonance-loops (v_s, L_k, D_1, C_{1a} and v_s, L_k, C_{1b}, D_4, C_{2b}) continue to resonate. In addition, i_p, i_{Cc}, i_s, v_{C1a}, v_{C1b} satisfy (6) (7) (8) (10) (11).

***Stage 4 [t_3, t_4]*:** At t_3, the currents i_{D1}, i_{D4} of the diodes D1, D4 become zero, and i_p decreases to zero. In addition, i_{L1} still increases linearly and i_{L2} still decreases linearly, as shown in Fig. 3. Furthermore, the anti-parallel diode of the switch S_1 conducts again. Since the resonance of the two loops is terminated at t_3, the diodes D_1, D_4 are turned off at ZCS, whose reverse-recovery problem has been removed.

***Stage 5 [t_4, t_5]*:** At t_4, the anti-parallel diode of S_1 begins to conduct. Hence, the switch S_1 is turned off at ZVS.

***Stage 6 [t_5, t_6]*:** At t_5, S_2 is turned on. This stage is analogous to stage 1. Therefore, the analysis of this stage is omitted.

***Stage 7 [t_6, t_7]*:** At t_6, S_4 is turned off. In addition, i_{L1} begins to charge C_{s3} and discharge C_{s4} linearly. After i_{L1} fully charges C_{s4} to V_{Cc} and discharges C_{s3} to 0 V, it flows through the anti-parallel diode of the switch S_3. Therefore, the zero voltage across the switch S_3 is maintained, and the switch S_3 can be turned on at ZVS in the next stage.

Like stage 2, during this stage, the input power is transferred to the output side. Since the voltage across the primary winding of the transformer is $v_p = V_{Cc}$, the secondary winding voltage is:

$$v_s = N \cdot V_{Cc} \tag{12}$$

There are two resonant loops. One loop is formed by C_{1a}, D_3, C_{2a}, L_{lk}. C_{1a} and v_s. It charges C_{2a} in series. The other loop is formed by C_{1b}, D_2, L_{lk} and v_s. C_{1b} is charged by v_s. Since the output capacitors C_{2a}, C_{2b} are sufficiently large when compared to the resonant capacitors C_{1a}, C_{1b}, the capacitors of the two resonant loops can be equivalent as C_{1a}, C_{1b}, respectively. The state equations can be written as follows:

$$-L_{lk}\frac{di_s(t)}{dt} = N \cdot V_{Cc} - v_{C1b}(t) \tag{13}$$

$$i_s(t) = -2 \cdot C_1 \cdot \frac{dv_{C1b}}{dt} \tag{14}$$

Here, C_{1a} is equal to C_1, and C_{1b} is the same as C_{1a}. Consequently, v_{C1a} and v_{C1b} can be derived as:

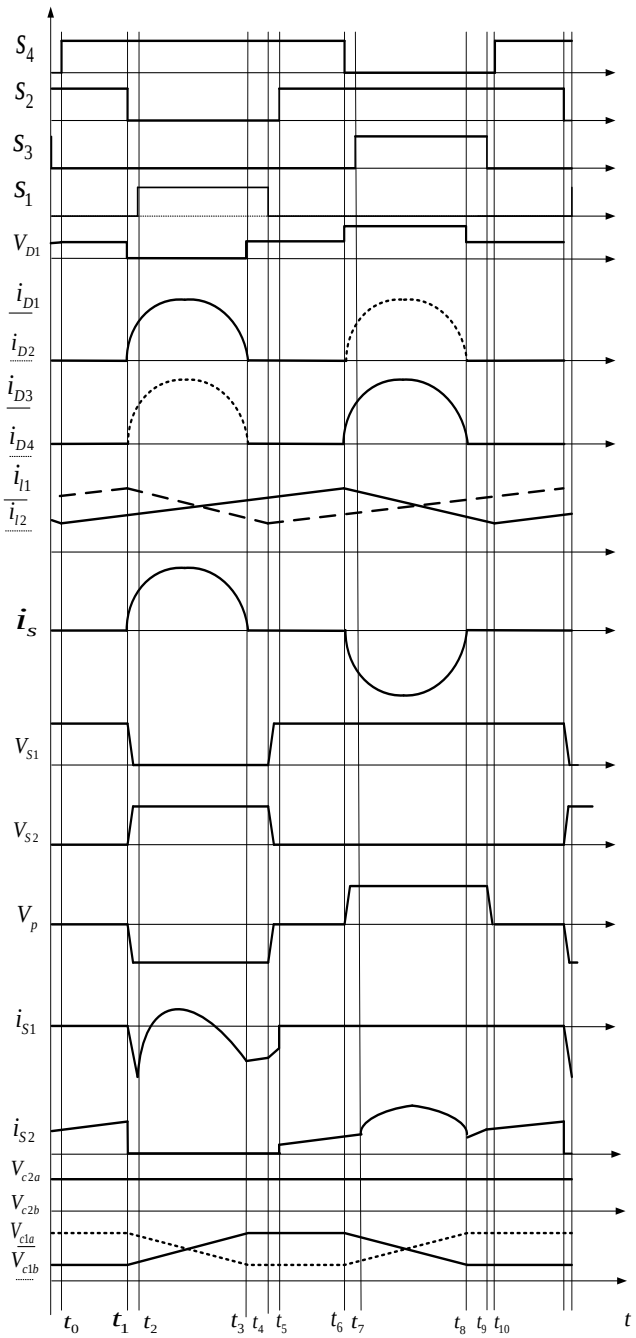


Fig. 3. Key waveforms of the proposed converter.

$$v_{C1a}(t) = N \cdot V_{Cc} + [N \cdot V_{Cc} - v_{C1a}(t_6)]\cos\omega_r(t - t_6) \quad (15)$$

$$v_{C1b}(t) = N \cdot V_{Cc} - [N \cdot V_{Cc} - v_{C1a}(t_6)]\cos\omega_r(t - t_6) \quad (16)$$

$$\begin{aligned} i_s(t) &= -\frac{N \cdot V_{Cc} - v_{C1a}(t_6)}{Z_r}\sin\omega_r(t - t_6) \\ &= I_{s,peak}\sin\omega_r(t - t_6) \end{aligned} \quad (17)$$

***Stage 8 [t_7, t_8]*:** At t_7, S_3 is turned on while its body diode has conducted. Hence, S_3 is turned on at ZVS. i_{L2} increases continuously as (2), and i_{L1} decreases linearly as follows:

TABLE II
SWITCHING SEQUENCE AT DIFFERENT DUTY CYCLE

D<0.5		D>0.5	
S_3 Turn off	S_3 Turn on	S_4 Turn off	S_4 Turn on
S_4 Turn on	S_4 Turn off	S_3 Turn on	S_3 Turn off
S_2 Turn off	S_2 Turn on	S_1 Turn off	S_1 Turn on
S_1 Turn on	S_1 Turn off	S_2 Turn on	S_2 Turn off

$$i_{L1} = i_{L1}(t_7) - \frac{V_{Cc} - V_{in}}{L_1}(t - t_7) \quad (18)$$

***Stage 9 [t_8, t_9]*:** Similar to stage 4, the diodes D_2, D_3 are turned off at ZCS. There is no reverse-recovery problem for the diodes D_2, D_3. The anti-parallel diode of the switch S_3 begins to conduct. The output current I_o is:

$$I_o = \frac{2}{T_s}\int_{t_6}^{t_8} I_{s,peak} \cdot \sin\omega_r(t - t_6) \quad (19)$$

By combining (18) and (20), $I_{s,peak}$ is obtained as:

$$I_{s,peak} = \frac{N \cdot V_{Cc} - V_{C1b}(t_6)}{Z_r} = \omega_r \cdot I_o \cdot T_s \quad (20)$$

***Stage 10 [t_9, t_{10}]*:** At t_9, switch S_3 is turned off at ZVS. Similar operation stages work in the rest of the stages in a switching period.

In the operation analysis discussed above, the duty cycle D is more than 0.5. When D is less than 0.5, the operation analysis is similar but the switching sequence is different. The switching sequences of two cases are summarized in Table II.

It should be pointed out that the bottom switches S_2, S_4 cannot achieve ZVS turn-on in this topology. However, this issue can be solved by adding an auxiliary circuit. The boundary condition will be derived and discussed in future works due to page limitations.

An operation analysis of the switched-capacitor doubler is discussed in Appendix A.

III. THE CONTROL SCHEME OF THE PROPOSED CONVERTER

Pulse-width modulation plus phase angle shift (PPAS) is used as the control scheme in the proposed converter. The current doubler port is plotted in Fig. 4(a). An interleaved boost converter is employed in the current doubler port shown in Fig. 4(a), which is the front part of the proposed converter shown in the left dashed block in Fig. 1(a). Where, V_{bus} is equal to V_{Cc}, v_p is the phase voltage difference between the leg BB_1 and the leg BB_2. Steady-state waveforms of the control scheme are described in Fig. 4(b). Where, D is duty cycle of the switches

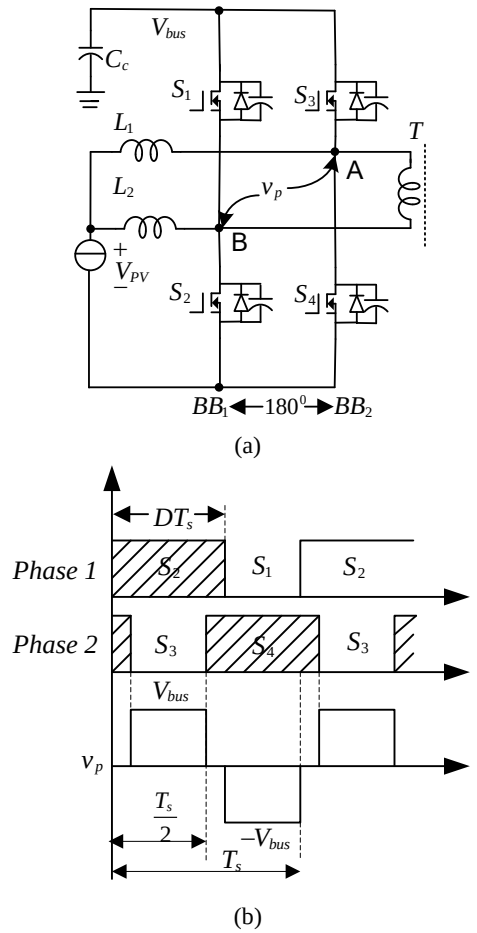


Fig. 4. Control scheme of the proposed converter. (a) Current doubler port. (b) Key steady-state waveforms.

S_2 and S_4, and Ts is the switching period. It is noted that the phase angle between BB_1 and BB_2 is kept at a constant 180° to reduce the current ripple. D is employed as the only control freedom to achieve output voltage regulation. Once D is adjusted during a selected range, the phase voltage difference v_p will vary correspondingly, as shown in Fig. 4(b). Hence, the transformer can be inserted into the primary side (point A and point B) and the switched-capacitor circuit (point C and point D), as shown in Fig. 1, to realize output voltage regulation. The relationship between the duty cycle, the transformer turns ratio N and the voltage conversion is derived in the next section.

IV. Performance Analysis and Design Considerations of the Converter

A. Voltage Gain Ratio

The volt-second balance law of L_1 during one switching period determines the relation between V_{in} and V_{Cc} as follows:

$$V_{in} \cdot D - (V_{Cc} - V_{in}) \cdot (1 - D) = 0 \tag{21}$$

Then, formula (22) can be derived as:

$$\frac{V_{Cc}}{V_{in}} = \frac{1}{1 - D} \tag{22}$$

The volt-second balance law of L_{lk} during one switching period provides the following relationship between the resonant capacitor average voltage V_{c1a} and V_o:

$$(V_{C1a} + N \cdot V_{Cc} - 0.5V_o) \cdot \frac{T_o}{2} + (V_{C1a} - N \cdot V_{Cc}) \cdot \frac{T_o}{2} = 0 \tag{23}$$

Where, T_o is the resonant period. Hence, the average voltage of the resonant capacitor V_{c1a} is obtained as:

$$V_{C1a} = 0.25V_o \tag{24}$$

Due to symmetry, V_{c1b} is equal to V_{c1a}.

The average value V_{c1a} is equal to the amplitude of v_s, and the amplitude of v_p is equal to V_{Cc}. Therefore, the relationship between the clamp capacitor voltage and the output voltage can be written as:

$$V_{Cc} = \frac{1}{4N} \cdot V_o \tag{25}$$

By combining (22) and (26), the relationship between the input voltage V_{in} and the output voltage V_o can be derived as:

$$\frac{V_o}{V_{in}} = N \cdot \frac{4}{1 - D} \tag{26}$$

B. Resonant Capacitor

The existence of stage 3 and stage 8 ensures the ZCS turn-off for the rectifier diodes D_1,D_2,D_3, D_4. The interval of stage 3 and stage 8 changes with variations of resonant frequency and duty ratio. To achieve ZCS turn-off for all of the rectifier diodes D_1, D_4, D_2, and D_3, the following critical conditions must be satisfied:

$$\frac{\pi}{\omega_r} < (1 - D) \cdot T_S \tag{27}$$

Where, ω_r is the critical angular resonant frequency. Therefore, the resonant capacitor C_{1a} must meet the following relationship:

$$C_{1a} < \frac{1}{L_{lk}} \cdot \left(\frac{V_{Cc}}{V_o} \cdot \frac{4N \cdot T_S}{\pi}\right)^2 \tag{28}$$

The leak inductance is an inductive reactance by nature. If the leak inductance is too large, the output capability of the system will be influenced. Of course, this also influences the switching frequency, current and voltage stress of the resonant elements since it participants the resonance process. In practical transformer design, it is difficult for the real value of the leakage inductance to meet the theoretical value well and there is some deviation. Therefore, the switching frequency and the resonant capacitor are determined based on the leak inductance, which means that the switching frequency and resonant capacitor values will be adjusted with deviations of the leak inductance.

C. Input Current Ripple

Assuming that the boost inductors L_1 and L_2 have the same

value L, the input-current ripple ΔI_{in} of the photovoltaic cell is:

$$\begin{aligned}\triangle(i_{L1}+i_{L2}) &= \left|\frac{V_{in}}{L}-\frac{V_{Cc}-V_{in}}{L}\right|\cdot(1-D)\cdot T_S \\ &= \left|\frac{2V_{in}-V_{Cc}}{L}\right|\cdot(1-D)\cdot T_S\end{aligned} \quad (29)$$

The maximum input current ripple $\Delta I_{\text{in,max}}$ occurs at the duty ratio D= 2/3. The maximum input current ripple $\Delta I_{\text{in,max}}$ is:

$$\Delta I_{in,\max} = \Delta(I_{L1}+I_{L2})_{\max} = \frac{V_o\cdot T_S}{36N\cdot L} \quad (30)$$

The current ripple of L_1 and L_2 is:

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{in}}{L}\cdot D\cdot T_S = \frac{(1-D)\cdot D}{L}\cdot V_{Cc}\cdot T_S \quad (31)$$

The maximum current ripple at the duty ratio D=0.5 is:

$$\Delta I_{L1,\max} = \Delta I_{L2,\max} = \frac{V_o\cdot T_S}{8N\cdot L} \quad (32)$$

From (31) and (33), the maximum input current ripple is much less than that of i_{L1} and i_{L2}.

D. Topology Extension of the Proposed Converter

The proposed converter, composed of a current doubler and a quasi-resonant switched-capacitor circuit, can be extended to other converters. The first one is the extension on the primary port as shown in the left dashed block of Fig. 5(a)-5(c), and the second one is the extension on the secondary port as show in the right dashed block of Fig. 5(a)-5(c).

The current doubler is extended into the three types shown in Fig. 5(a)-(c). The primary port of type I is an interleaved buck-boost converter. Unlike the proposed converter, the clamp capacitor is connected to the positive of the power source so that it can endure the lower voltage stresses of the clamp capacitor. However, a larger capacitance is required. Similarly, the primary port of type II is an interleaved buck-boost converter. However, the upper switches S_1, S_3 are employed as main switches and V_{in} is float. On the other hand, the primary port of type III is a current-fed half bridge converter. The current-fed DC-DC isolated converters, use fewer switches without an active clamp circuit.

The switched-capacitor circuit can be extended to attain a different voltage gain by adding or removing switched-capacitor cells as shown in the green block of Fig. 5(a)-(c). In Fig. 5(a)-(c), there are two switched-capacitor cells and 8 times the voltage of the transformer secondary winding can be reached in the output port. A general principle is that M switched-capacitor cells are employed and 4M times the voltage is obtained through the switched-capacitor circuit.

E. Performance Comparison

For conventional current-fed full-bridge converters [28], to provide a current path for the input inductor, the duty cycle of the primary main switches should be greater than 0.5 under any load condition. Consequently, an additional start-up circuit

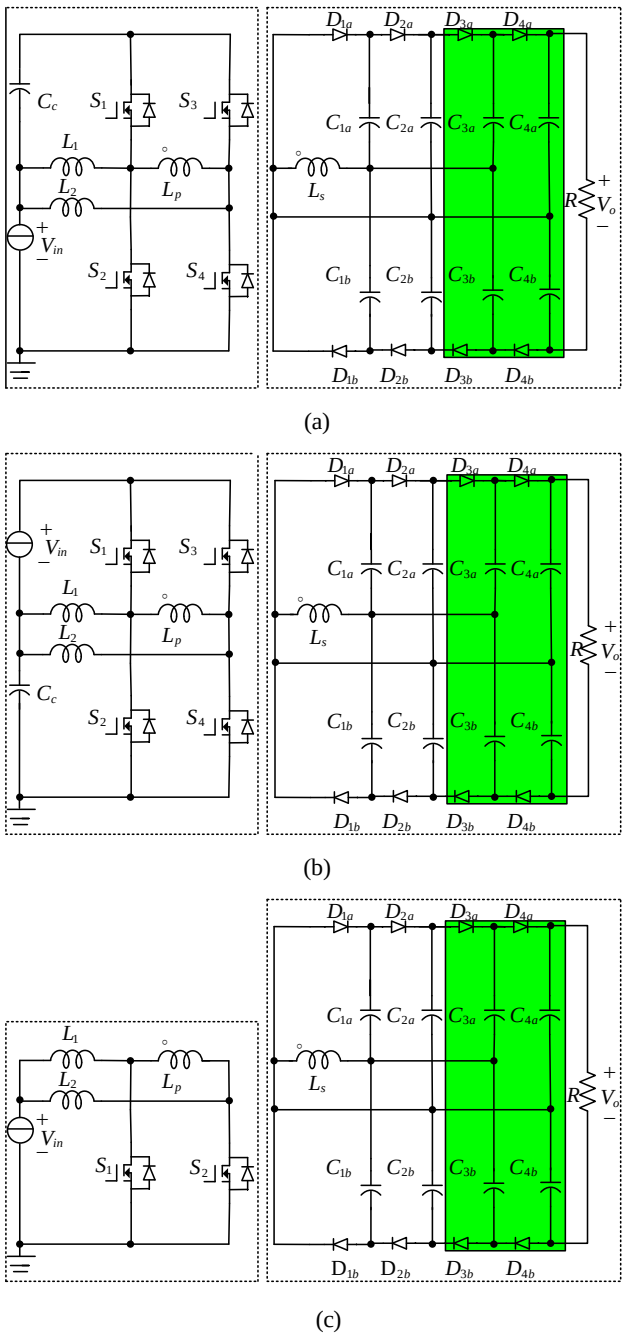


Fig. 5. Extension of the proposed converter (a) Type I(b) Type II(c) Type III

should be designed to minimize the inrush current during the start-up process. Meanwhile, the primary current should flow through two primary switches in most of the operation states, which results in large switch conduction losses. In addition, the current stress of the input inductor is high due to its whole input current maintenance. Last, the magnetizing currents of the two inductors cannot be limited since this leads to a minimum output power level. However, the main-switch duty cycle of the proposed converter can vary from 0 to 1. When the duty cycle is lower than 0.5, the present converter may work in

TABLE III
PERFORMANCE COMPARISON

Converter type	Conventional converter	Converter in [29]	Proposed converter
Duty cycle	More than 0.5	More than 0.5	0~1
Additional start-up circuit	Necessary	Necessary	Unnecessary
Minimum output power level	Limited	Limited	Unlimited
Output voltage ripple	Large	Little	Little
Voltage level extension	No	No	Yes
Soft switching	Yes	No	No
Peak current through switches	Large	Middle	Small
Peak current through diodes	Large	Middle	Small
Soft switching	No	Yes	Yes
Diodes number	4	4	4
Diodes TPDR	$2U_{o*}\ I_o$	$2U_{o*}\ I_o$	$2U_{o*}\ I_o$
Switches number	2	4	4
Switches TPDR	$V_{in}{}^{*}\ I_{in}/(1-D)$	$2V_{in}{}^{*}\ I_{in}/(1-D)$	$2V_{in}{}^{*}\ I_{in}/(1-D)$
Inductor number	3	2	2
Turn ration of transformer at same duty cycle	1:4	1:1	1:1

the discontinuous current mode with a light load. As a result, the ZVS performance is lost because the leakage energy is not sufficient to discharge the energy stored in the parallel capacitor when the corresponding clamp switch turns off. In addition, a wide duty-cycle operation range is achieved in the proposed converter to remove the additional start-up circuit. Moreover, the current stress of the magnetizing inductors is decreased because of the large input current distribution in the two interleaved phases. Finally, the primary switch conduction loss is reduced. This is because the primary current only flows through one switch and the average current stress on the active-clamp switches is relatively low. In other words, the proposed converter is more suitable for high-efficiency, high step-up, and high-power-density dc/dc conversions when compared with the conventional current-fed full-bridge converters.

The authors of [29] presented a topology that is similar to the proposed converter except for the reduced clamped-capacitor utilized in primary-side of the proposed converter. The main difference is the control strategy. This results in different operation principles for the two converters. They have some similar merits, such as soft switching realization for primary-side MOSFET switches and secondary-side diodes, few turn ration of the transformer, and a low output-voltage ripple. Due to the sawtooth-wave current through the switches and diodes for the converter in [29], there is higher peak current when compared with the sine-wave current operation of the proposed converter at the same average output current. This means higher conduction losses in primary-side switches and in the secondary-side diodes for the converter in [29].

A more detailed comparison between the conventional current-fed full bridge converter, the converter in [29] and the proposed converter is summarized in Table III. Assume that the three converters have the same power rating and voltage gain. Define V_{in}, I_{in}, U_o, I_o, and D as the input voltage, input current, output voltage, output current and duty cycle, respectively. Introduce the concept of DPTR (device power total rating, which is equal to the current rating times the voltage rating) to descript the device cost.

F. Design Consideration

The 400-W design procedure of the proposed converter is shown here as an example. Some of the specifications of the prototype converter are set first: V_{in} =25V, V_o= 200 V, P_o= 400 W, N_1/N_2=18:18, L_k=1uH, and f_s=50 kHz.

1) Resonant Frequency: In order to provide ZCS turn-off for the rectifier diodes D_1, D_2, D_3, D_4, in addition to making sure the switching frequency is lower than the resonant frequency, other relations need to be satisfied:

$$\begin{cases}(1-D)T_s - T_{dead} > 0.5T_o \\ DT_s - T_{dead} > 0.5T_o\end{cases} \tag{33}$$

Where, T_o is resonant period. Here, set f_o=80KHz.

2) Resonant Capacitor: The resonant capacitance value should meet (29), and it should be chosen according to the voltage ripple[26][27]. A detailed derivation is discussed in Appendix A:

$$\Delta v_{C1} = \frac{1}{2}\omega_o I_0 z_o T_s = \frac{1}{2}\frac{I_0 T_s}{C_1} \tag{34}$$

Where, C_1 is resonant capacitor value. The value of the voltage ripple is determined by the output current, the resonant capacitance value and the switching frequency. The capacitor voltage ripple should be smaller than the average voltage

TABLE IV
SIMULATION SPECIFICATION OF THE PROPOSED CONVERTER

Input voltage	25V	Boost Inductor	L_1=L_2=60uH
Leakage inductance	1uH	Resonant capacitor	C_{1a}=C_{1b}=2uF
Turn Ratio	1:1	Clamp capacitor	C_c=10uF
Output power	400W	Parallel capacitor	C_{s1}=C_{s2}=C_{s3}=C_{s4}=2.2nF
Switching frequency	50KHz	Output capacitor	C_{2a}=C_{2b}=47uF

TABLE V
PARAMETERS OF THE PROTOTYPE

Input voltage	25V	Output power	400W
Turn ratio of transformer	18:18	Switching frequency	50KHz
Leakage inductance of transformer	1uH	Inductance of boost inductors	60uH
Resonant capacitor	2uF	Output capacitor	47uF
Clamp capacitor	10uF	Parallel capacitor	2.2nF
Main/Auxiliary switches	IRF3710	Rectifier diodes	HER 303

(equal to v_s) to prevent voltage across the resonant capacitor from the positive to negative region and losing ZCS. This means that the resonant capacitor should have a positive dc voltage offset.

3) Output Capacitor: Another consideration is that the maximum voltage ripple should be less than one third of the dc component. Here, a 20% voltage ripple is considered for the resonant capacitor. Then the resonant capacitance value can be derived as:

$$C_1 \geq 1u$$

Here, a 2uF resonant capacitor is selected.

C_2 is large enough to maintain a constant voltage for each stage.

$$\Delta v_{C2} = \frac{I_o}{C_2}[\frac{\cos\theta}{f_s} - \frac{1}{f_o}(1 - \frac{2\theta}{\pi})] \quad (35)$$

Where, $\theta = \sin^{-1}(fs)/(\pi f_o)$ and $I_o = (P_o)/(V_o)$. For a 0.1 V ripple voltage, this gives C_2=59.2uF and 47uF is selected.

4) Duty Cycle: According to (34), the duty cycle range is selected to be 0.3375<D<0.6625. In the experiments, D is selected to be 0.5.

5) Other Considerations: The boost inductor is selected according to formula (33). Here, two 60uH inductors are used.

Since the peak voltage stresses on the diodes D_1, D_2, D_3, D_4 are equal to half of the output voltage V_o, the block voltage of the diodes are chosen to be V_o for twice the voltage stress concern.

V. SIMULATION AND EXPERIMENTAL RESULTS

The specifications for the simulation are shown in Table IV. A prototype of the proposed converter plotted in Fig. 1 is implemented. The prototype is operated with the parameters shown in Table V.

The saber simulation waveforms of the proposed converter are shown in Fig. 6.

The simulation waveforms verify the principle of the proposed converter and the feasibility of the operation is validated.

Fig. 7 shows the ZCS realization of the rectifier diodes. In Fig. 7(a), i_{D1} and i_{D2} decrease to zero before the diodes D_1, D_2 are reverse biased, and D_1, D_2 achieve ZCS turn-off. Analogously, D_3, D_4 achieve ZCS turn-off as shown in Fig. 7(b). From the waveforms, it is noted that the reverse-recovery problem has been removed.

Fig. 8 shows the voltage and current waveforms across the primary/secondary windings of the transformer. The primary/secondary winding currents agree with the theoretical analysis and the primary voltage spike is suppressed partly due to the clamp capacitor. A high frequency resonance occurs as shown in Fig. 8(a) because of the parasitic capacitor of the transformer. This will kill the system efficiency.

Fig. 9 shows the input/output characteristic of the proposed converter. The ripple of the input current is reduced greatly as shown in Fig. 9(a). Due to the symmetrical duty cycle of the switches S_2, S_4, the two boost inductors work in an interleaved way to be charged or discharged, and the input current is almost ripple free. Fig. 9(b) shows the input/output voltage and the current waveforms together. The output voltage drops to 188V from the theoretical 200V under the open loop control due to the output impedance. The voltage drop includes the device (MOSFETs and rectifier diodes) drop voltage and the transformer voltage drop. It is noted that the output voltage is almost ripple free due to the alternate charging and discharging of the output capacitors.

Fig. 10 shows the voltage of the switched-capacitors. V_{c1a} and V_{c1b} are the dc voltages with a sinusoidal ripple determined by the resonant parameters and load as calculated in (34)(35), V_{c2a} and V_{c2b} have relatively large capacitances. As a result, the voltage is basically constant. In theoretical calculation, V_{c2a} = V_{c2b}=100V.

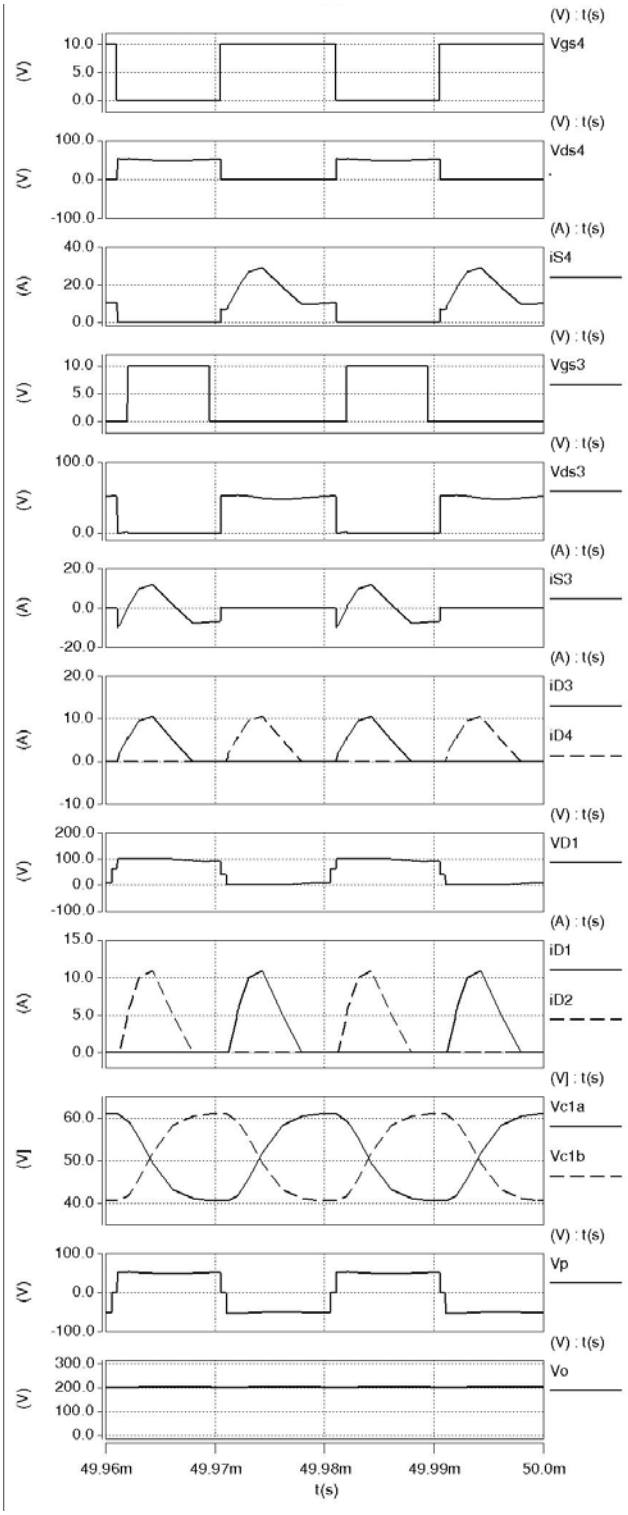


Fig. 6. Simulation waveforms.

In Fig.11, the voltage spike of the main switches is reduced by the active-clamp circuit. The clamp-capacitor voltage calculated from (22) is 25V for a duty cycle that is close to 0.5. Hence, S_3 (the drain-source voltage of the auxiliary switch) along with V_{ds3} and V_{ds4} (the drain-source voltage of the main switch S_4) are clamped to be about 50V, which agrees with the

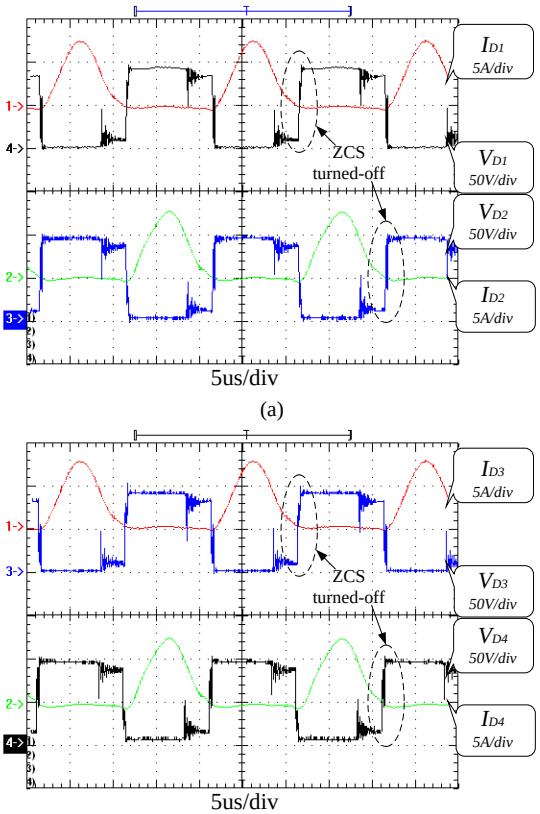


Fig. 7. Voltage/current waveforms of the rectifier diodes. (a) Waveforms of D_1, D_2. (b) Waveforms of D_3, D_4.

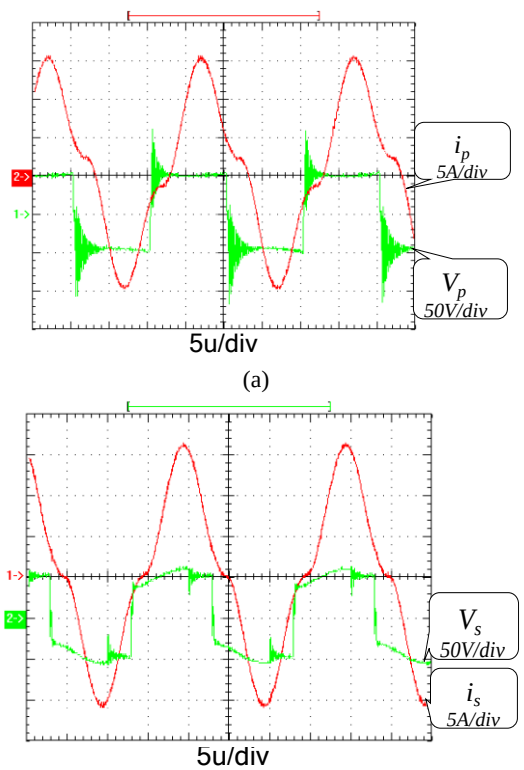
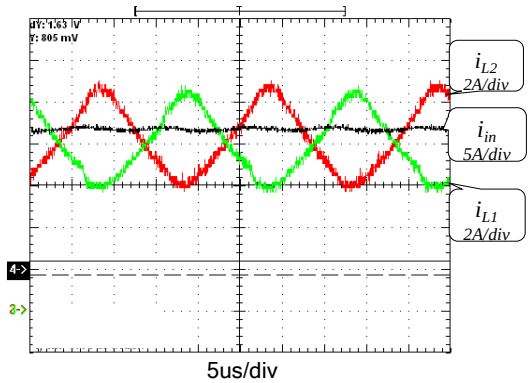
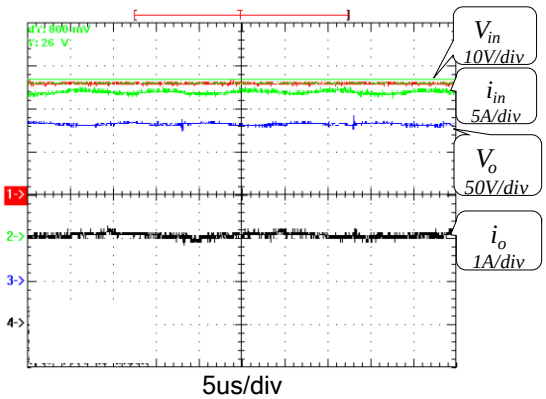


Fig. 8. Voltage/current of transformer windings. (a) Primary winding. (b) Secondary winding.



(a)



(b)

Fig. 9. Input/output characteristic of the proposed converter. (a) Current waveforms of i_{L1},i_{L2}, $I_{in.}$ (b)Input/output voltage and current.

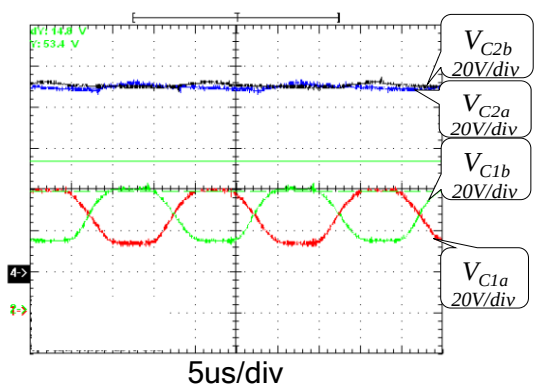


Fig. 10. Switched-capacitors voltage.

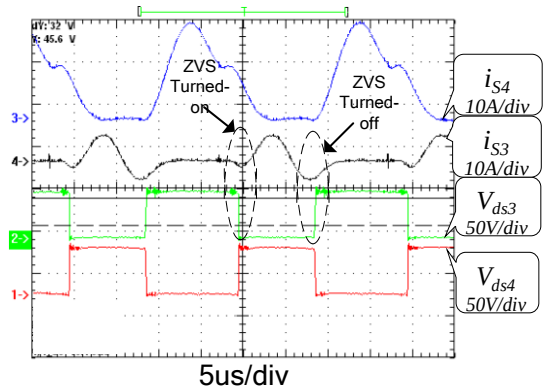


Fig.11. Drain-source voltage waveforms of switches S_3&S_4 and current waveforms of switches S_3&S_4.

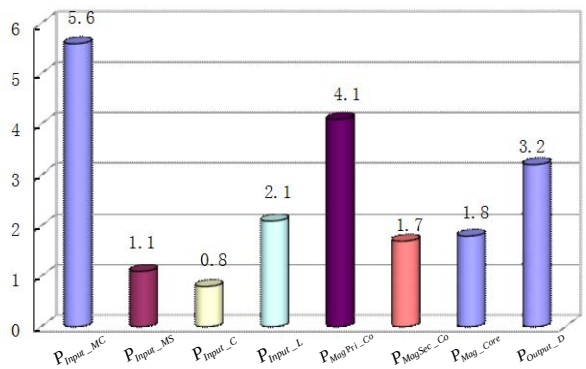


Fig. 12. Loss breakdown distribution at 400-W load.

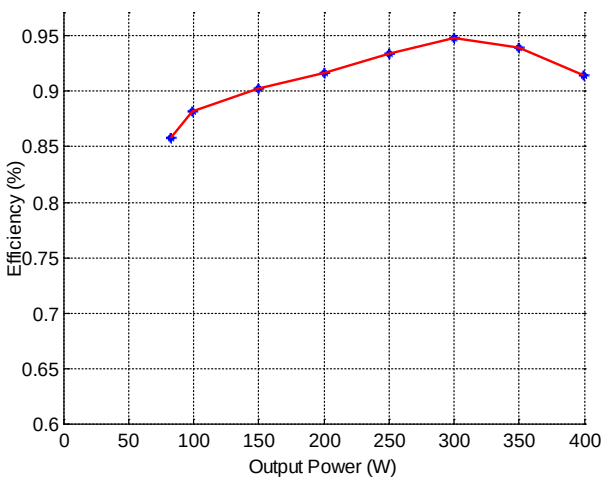


Fig.13. Measured efficiency.

theoretical waveforms. It should be mentioned that ZVS turn-on/off is realized for the switch S_3.

With the selected parameters, the estimated power loss distribution is calculated and summarized in Fig.12. The loss includes the main switches conduction loss P_{Input_MC}, the main switches switching loss P_{Input_MS}, the clamp switches conduction loss P_{Input_C}, the input-side boost inductors conduction loss P_{Input_L}, the output-side diodes conduction loss P_{Output_D}, the magnetic core loss of the transformer P_{Mag_Core}, the primary copper loss of the transformer P_{MagPri_Co}, and the secondary copper loss of the transformer P_{MagSec_Co}. It can be found that the main switches loss and the primary copper loss are dominant for the loss distribution. The estimated efficiency at a 400w load with a 25V input and a 200V output is about 94.86%.

The main switches conduction loss and the primary copper loss of the transformer are dominant due to a high primary current. In addition, the output diodes conduction loss covers a relative breakdown because of the relative high forward voltage of the diodes. Since the diodes are turned off at ZCS, it

is better to utilize diodes with a lower forward voltage to promote system efficiency.

The measured efficiency of the proposed converter under all load conditions is presented in Fig.13. The maximum efficiency is over 94.79% at a 300-W load. Due to ZCS realization for all of the rectifier diodes and ZVS turn-off/turn-on realization for the auxiliary switches S_1, S_3. The efficiency of the proposed converter is high but relatively low at a light load since the basic loss weight increases in the whole power range.

VI. CONCLUSION

This paper presents a high step-up DC-DC converter for photovoltaic power systems. The characteristic of the proposed converter can be summarized as follows:

1) The diodes are turned off at ZCS to solve the reverse-recovery problem and the maximum voltage stress of the rectifier diodes is reduced to one half of the output voltage.
2) The symmetrical structure of the switched-capacitor circuit results in an output voltage ripple reduction because the ripples on the charging capacitor and discharging capacitor cancelled each other out.
3) The double boost inductors are operated in an interleaved way to minimize the input current ripple.
4) The voltage spike of the MOSFETs is suppressed by an active clamp circuit.
5) The leakage of the two-winding transformer is shared by two resonant loops to reduce the complexity of the transformer.
6) The PPAS control strategy is employed in the proposed converter to control the output voltage.

APPENDIX

Without a loss of generality, the following assumptions are made: all of the switches are desirable and no conduction resistance is considered. The input voltage source is desirable, constant and has no internal impedance. The capacitor ESR is zero. Assuming that C_{1a}=C_{1b}=C_1 and C_{2a}=C_{2b}=C_2, the state equations of the simplified equivalent circuit shown in Fig. 1 are derived:

***State I [t_1, t_3]*:** From the waveforms shown in Fig. 14, the resonance starts at t_1, and stops at t_3.

$$\begin{cases} V_s = L_{lk}\dfrac{di_{Lr}}{dt} + v_{C1a} \\ i_{Llk} = 2C_1\dfrac{dv_{C1a}}{dt} \end{cases} \tag{A1}$$

By using input and output power balancing in the whole period, for state I in half of a period:

$$V_{in}\int_{t_1}^{t_3} i_{Llk}\,dt = \frac{1}{2}V_o I_o T_s \tag{A2}$$

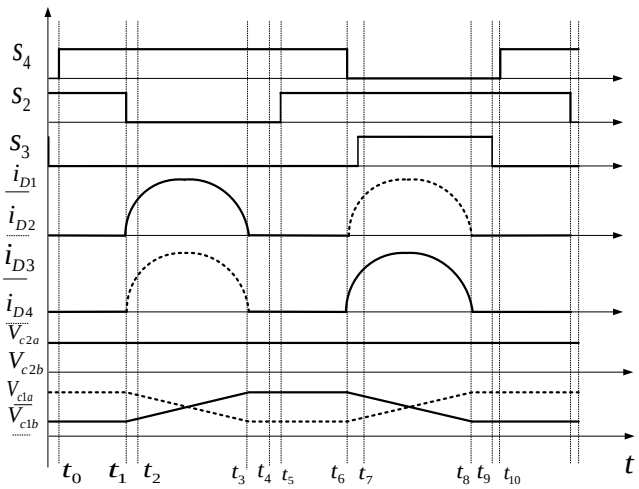


Fig. 14. Key waveforms of switched-capacitor circuit.

By solving (A2), assume that the voltage conversion ratio is 4, then:

$$\begin{cases} i_{Llk} = \dfrac{1}{2}\omega_o I_0 T_s \sin\omega(t-t_1) \\ v_{C1a} = V_{in} - \dfrac{1}{2}\omega_o I_0 z_o T_s \cos\omega(t-t_1) \\ v_{C1b} = V_{in} + \dfrac{1}{2}\omega_o I_0 z_o T_s \cos\omega(t-t_1) \\ \Delta v_C = \dfrac{1}{2}\omega_o I_0 z_o T \end{cases} \tag{A3}$$

Where:

$$\begin{cases} \omega_o = \sqrt{\dfrac{1}{2L_{lk}C_1}} \\ z_o = \sqrt{\dfrac{L_{lk}}{2C_1}} \end{cases} \tag{A4}$$

***State II [t_3, t_6]*:** In this stage, the voltages of C_{1a} and C_{1b} are unchanged. C_{2a} and C_{2b} in series are discharged to the load. The equations of this state are:

$$\begin{cases} v_{C1a} = V_{in} - \dfrac{1}{2}\omega_o I_0 z_o T_s \\ v_{C1b} = V_{in} + \dfrac{1}{2}\omega_o I_0 z_o T \\ i_{Llk} = 0 \end{cases} \tag{A5}$$

***State III [t_6, t_{10}]*:** This process is similar to state I. The state equations are as follows:

$$\begin{cases} V_s = -L_{lk}\dfrac{di_{Llk}}{dt} + v_{C1b} \\ i_{Llk} = -2C_1\dfrac{dv_{C1b}}{dt} \end{cases} \tag{A6}$$

By using input and output power balancing, for state III:

$$\begin{cases} V_s \int_{t_6}^{t_8} i_{Llk} dt = \frac{1}{2} V_o I_o T_s \\ i_{Llk} = -\frac{1}{2} \omega_o I_0 T_s \sin \omega (t - t_6) \\ v_{C1a} = V_s + \frac{1}{2} \omega_o I_0 z_o T_s \cos \omega (t - t_6) \\ v_{C1b} = V_s - \frac{1}{2} \omega_o I_0 z_o T_s \cos \omega (t - t_6) \end{cases} \quad \text{(A7)}$$

***State IV [t_3, t_4]*:** This process is similar to state II. The operation analysis is neglected but the state equations are listed here:

$$\begin{cases} v_{C1a} = V_{in} + \frac{1}{2} \omega_o I_0 z_o T_s \\ v_{C1b} = V_{in} - \frac{1}{2} \omega_o I_0 z_o T_s \\ i_{Llk} = 0 \end{cases} \quad \text{(A8)}$$

ACKNOWLEDGMENT

The research work was supported by the National Nature Science Foundations of China (No.61403320), the Natural Science Foundation of Fujian Province (No. 2015J201274) and the Fundamental Research Funds For Central University (No.2013121017, No. 20720150088). The support from Collaborative Innovation Center of High-End Equipment Manufacturing in FuJian is also acknowledged.

REFERENCES

[1] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind.Appl.*, Vol. 41, No. 5, pp. 1292-1306, Sep./Oct. 2005.

[2] B. Yang, W. Li, Y. Zhao, and X. He," Design and analysis of a grid-connected photovoltaic power system," *IEEE Trans. Power Electron.*, Vol. 25, No. 4, pp. 992-1000, Apr. 2010.

[3] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM converters with high step-up conversion ratio," *IEEE Trans. Circuit and System*, Vol. 55, No. 4, pp. 1159-1175, Mar. 2008.

[4] B. Liu, S. Duan, and T. Cai, "Photovoltaic DC-building-module-based BIPV system-concept and design considerations," *IEEE Trans. Power Electron.*, Vol. 26, No. 5, pp. 1418-1429, May 2011.

[5] J. I. Kang, C. W. Roh, G. W. Moon, and M. J. Youn "Phase-shifted parallel-input/series-output dual converter for high-power step-up applications," *IEEE Trans. Ind. Electron.*, Vol. 49, No. 3, pp. 649-652, Jun. 2002.

[6] Y. Jang and M. M. Jovanovic, "New two-inductor boost converter with auxiliary transformer," *IEEE Trans. Power Electron.*, Vol. 19, No. 1, pp. 169-175, Jan. 2004

[7] S.-K. Han, H.-K. Yoon, G.-W. Moon, M.-J. Youn, Y.-H. Kim, and K.- H. Lee, "A new active clamping zero-voltage switching PWM current-fed half-bridge converter," *IEEE Trans. Power Electron.*, Vol. 20, No. 6, pp. 1271-1279, Nov. 2005.

[8] S.-J. Jang, C.-Y.Won, B.-K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEETrans. Energy Convers.*, Vol. 22, No. 2, pp. 332-340, Jun. 2007.

[9] N. P. Papanikolaou and E. C. Tatakis, "An integrated magnetic isolated two-inductor boost converter: analysis, design and experimentation ," *IEEE Trans Power Electron.*, Vol. 20, No. 2, pp. 332-342, Jun. 2005.

[10] M. Prudente, L. L. Pfitscher, G. Emmendoerfer, E. F. Romaneli, and R. Gules, "A new active clamping zero-voltage switching PWM current-fed half-bridge converter". *IEEE Trans. Power Electron.*, Vol. 20, No. 6, pp. 1271-1279,Nov. 2005.

[11] T. F. Wu, Y. S. Lai, J. C. Hung, and Y. M. Chen, "Boost converter with coupled inductors and buck–boost type of active clamp," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 1, pp. 154-162, Jan. 2008.

[12] Q. Li and P. Wolfs, "A current fed two-inductor boost converter with an integrated magnetic structure and passive lossless snubbers for photovoltaic module integrated converter applications," *IEEE Trans. Power Electron.*, Vol. 22, No. 1, pp. 309-321, Jan. 2007.

[13] S.-J. Jang, C.-Y. Won, B.-K. Lee, and J. Hur, "Fuel cell generation system with a new active clamping current-fed half-bridge converter," *IEEE Trans. Energy Convers.*, Vol. 22, No. 2, pp.332-340, Jun. 2007.

[14] Y. Jang and M. M. Jovanovic, "Interleaved boost converter with intrinsic voltage-doubler characteristic for universal-line PFC front end," *IEEE Trans. Power Electron.*, Vol. 22, No. 4, pp. 1394-1401, Jul. 2007.

[15] J. Wang, F. Z. Peng, J. Anderson, A. Joseph, and R. Buffenbarger, "Low cost fuel cell converter system for residential power generation," *IEEE Trans. Power Electron.*, Vol. 19, No. 5, pp. 1315–1322, Sep. 2004.

[16] S. Jalbrzykowski, A. Bogdan, and T. Citko, "A dual full-bridge resonant class-E bidirectional DC–DC converter," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 9, pp.3879-3883, Sep. 2011.

[17] L. He, "A novel quasi-resonant bridge modular switched-capacitor converter with enhanced efficiency and reduced output voltage ripple," *IEEE Trans. Power Electron.*, Vol. 29, No. 4, pp. 1881-1893, Mar. 2013.

[18] W.-J. Lee, C.-E. Kim, G.-W. Moon, and S.-K. Han, "A new phase-shifted full-bridge converter with voltage-doubler-type rectifier for high-efficiency PDP sustaining power module," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 6, pp. 2450-2458, Jun. 2008.

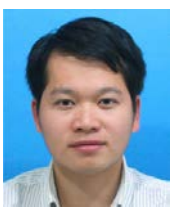
[19] L. He, "High-performance bridge modular switched-capacitor converter with small component requirement based on output impedance analysis for low loss," *IEEE Trans. Power Electron.*, Vol. 28, No. 10, pp. 4668-4680, Oct. 2014.

[20] J. J. Lee, J. M. Kwon, E. H. Kim, and B. H. Kwon, "Dual series-resonant active-clamp converter," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 2, pp. 699-709, Feb. 2008.

[21] B. R. Lin, Y. S. Huang, and J. J. Chen, "Soft switching active-clamped dual-series resonant converter," *IEEE Trans. IET Power Electron.*, Vol. 3, No. 5, pp. 764-773, Feb. 2010.

[22] J.-M. Kwon and B.-H. Kwon, "High step-up active-clamp converter with input-current doubler and output-voltage doubler for fuel cell power systems," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 108-115, Jan. 2009.

[23] K.-H. Yi and G.-W. Moon, "Novel two-phase interleaved LLC series-resonant converter using a phase of the resonant capacitor," *IEEE Trans. Ind. Electron.*, Vol. 56, No. 5, pp. 1815-1819, May 2009.
[24] G. Ivensky, S. Bronshtein, and A. Abramovitz, "Approximate analysis of resonant LLC DC-DC converter," *IEEE Trans. Power Electron*, Vol. 26, No. 11, pp. 3274-3284, Nov. 2011.
[25] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp.1746-1756, May 2011.
[26] C. Y.-F. Ho, B. W.-K. Ling, Y.-Q. Liu, P. K.-S. Tam, and K.-L. Teo, "Optimal PWM Control of Switched-Capacitor DC–DC Power Converters via Model Transformationand Enhancing Control Techniques," *IEEE Trans. Circuits Syst. I, Reg. Papers*, Vol. 55, No. 5, pp. 1382-1391, Jun. 2008.
[27] Y. P. B. Yeung, K. W. E. Cheng, S. L. Ho, K. K. Law, and D. Sutanto, "Unified analysis of switched-capacitor resonant converters," *IEEE Trans. Ind. Electron.*, Vol. 51, No. 4, pp. 864-873, Aug. 2004.
[28] G. I. Vensky, I. Elkin, and S. Ben-Yaakov, "An isolated dc/dc converter using two zero current sitched IGBT's in a symmetrical topology," in *Proc. IEEE PESC'94 Conf.*, pp. 1218-1225, 1994.
[29] Y. Zhao, X. Xiang, W. Li, X. He, and C. Xia, "Advanced symmetrical voltage quadrupler rectifiers for high step-up and high output-voltage converters," *IEEE Trans. Power Electron*, Vol. 28, No. 4, pp.1622-1631, Apr. 2013.



Liangzong He was born in Hunan, China, in 1984. In September 2012, he joined Xiamen University, Xiamen, China, as an Assistant Professor. His current research interests include DC-DC converters, switched-capacitor converters, Z-source converters, and renewable energy generation.

Tao Zeng was born in Hunan, China, in 1983. He is presently an Assistant Professor in Department of Mechanical and Electrical Engineering, Xiamen University, Xiamen, China. His current research interests include the design of switching power supplies, and the design of haptic devices for shape and texture rendering.

Tong Li was born in Hubei, China, in 1989. He is presently working toward the master degree in Department of Mechanical and Electrical Engineering, Xiamen University, Xiamen, China. His current research interests include ac-ac switched-capacitor converters, and renewable energy generation.

Yuxian Liao was born in Fujian, China, in 1989. He is presently working toward the master degree in Department of Mechanical and Electrical Engineering, Xiamen University, Xiamen, China. His current research interests include renewable energy generation and wireless power transmission.

Wei Zhou received his Ph.D. degree in Mechanical Engineering from the South China University of Technology, Guangzhou, China. From 2010 to 2012, he was a Postdoctoral Researcher at Sun Yat-sen University, Guangdong, China. He is presently an Associate Professor at Xiamen University Xiamen, China. His current research interests include the design, fabrication and performance evaluation of energy and biomedical devices.