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Design of a 12b SAR ADC for DMPPT Control in a Photovoltaic System

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***Abstract*:** This paper provides the design techniques of a successive approximation register (SAR) type 12b analog-to-digital converter (ADC) for distributed maximum power point tracking (DMPPT) control in a photovoltaic system. Both a top-plate sampling technique and a V_{CM}-based switching technique are applied to the 12b capacitor digital-to-analog converter (CDAC). With these techniques, we can implement a 12b SAR ADC with a 10b capacitor array digital-to-analog converter (DAC). To enhance the accuracy of the ADC, a single-to-differential converted DAC is exploited with the dual sampling technique during top-plate sampling. Simulation results show that the proposed ADC can achieve a signal-to-noise plus distortion ratio (SNDR) of 70.8dB, a spurious free dynamic range (SFDR) of 83.3dB and an effective number of bits (ENOB) of 11.5b with bipolar CMOS LDMOD (BCDMOS) 0.35μm technology. Total power consumption is 115uW under a supply voltage of 3.3V at a sampling frequency of 1.25MHz. And the figure of merit (FoM) is 32.68fJ/conversion-step.

***Keywords*:** SAR ADC, Low switching energy, Photovoltaic system, Distributed MPPT

1. Introduction

Solar electricity is one of today's prospective renewable energy sources. However, the power-generating efficiency is reduced by weather conditions and the surrounding environment, such as shadow. To improve efficiency of the photovoltaic (PV) module, a maximum power point tracking (MPPT) control system is usually applied.

Fig. 1 shows the structure of a photovoltaic system to which a distributed MPPT (DMPPT) is applied [1]. To apply MPPT control, an analog-to-digital converter (ADC) and a DMPPT control block are designed inside the system on chip (SoC). And a PV cell module, a boost DC-DC converter and loads are outside the SoC [1]. The 12b ADC receives single-ended analog voltage from the PV cell and provides the corresponding digital information to the DMPPT control circuits of the photovoltaic system.

In this paper, we focus on the design of this 12b successive approximation register (SAR) ADC for DMPPT control in a photovoltaic system, while conventional MPPT uses an 8b ADC [1]. The proposed ADC is optimized for performance in terms of power, accuracy, and small area.

2. Proposed 12b SAR ADC Architecture

Fig. 2 shows a block diagram of the proposed 12b SAR ADC. It has a synchronous main control block, a comparator, a digital output buffer and a single-to-differential 10-bit DAC. To enhance the accuracy of the ADC, a single-to-differential converted DAC is exploited with a dual-sampling technique [2].

Both the top-plate sampling technique and V_{CM}-based switching technique are also applied to the 12b capacitor digital-to-analog converter (CDAC). With these techniques, we can implement a 12b SAR ADC with a 10b capacitor array DAC. More details are described in Section 3.

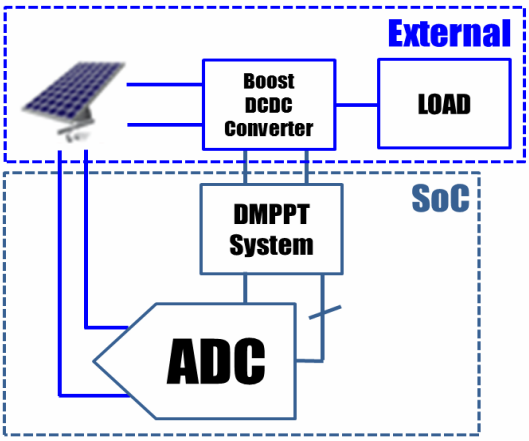

Fig. 1. Block diagram of a PV system.

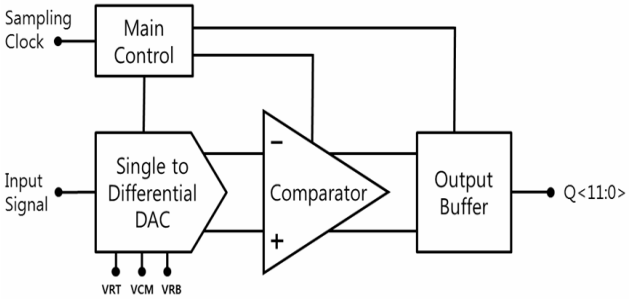

Fig. 2. Block diagram of the proposed 12b SAR ADC.

3. Design of Proposed 12b DAC

Fig. 3(a) shows the conventional 12b DAC with attenuation capacitor under bottom-plate sampling techniques. This attenuation capacitor reduces the total capacitor array, and hence, reduces the chip area remarkably [7]. During the sampling periods, VIN is sampled at all the bottom plates of capacitor arrays. In the very first step during the holding and conversion periods, for the most significant bit (MSB) decision, the 32C capacitor is switched to VRT (or VRB), then the difference of the VIN and one half of VRT (VRT/2) is compared. As a result, the MSB is determined. After the MSB is determined, the next (second) MSB is resolved by switching the 16C capacitor to VRT (VRT/4). These operations continue for 12 steps until the least significant bit (LSB) is resolved. The total number in the conventional capacitor array is 256Cs for differential operation.

Fig. 3(b) shows the proposed single-to-differential 12b DAC by adopting a dual sampling technique that is basically the same as a top-plate input sampling technique in differential operation. To improve accuracy, the single-ended input signal (PV voltage) is converted to a differential signal by selectively sampling the single-ended input signal of VIN. That is, for the upper capacitor array, the analog single-ended input signal VIN is sampled at the top plate of the capacitor array, and for the lower capacitor array, the analog single-ended input signal VIN is sampled at the bottom plate. This means that the plus (+) VIN signal is sampled at the non-inverting input of the comparator, and the minus (-) VIN signal is also sampled at the inverting input of the comparator. With this dual sampling technique, differential signal processing is possible with the single input signal in this photovoltaic system application. Since the differential VIN is applied to the comparator, the MSB can be directly determined with this differential sampled input signal. In this case, we do not need to switch 32C to VRT (or VBT). This means that the MSB can be determined without the 32C capacitor array for the MSB in holding mode as with the conventional design. The remaining bits can be resolved from the second MSB by using the half of the capacitor array in holding and conversion periods. This dual sampling technique reduces the MSB capacitor array by half. Total number in the capacitor array with this sampling technique is 192Cs for differential operation.

Fig. 3(c) shows the proposed 12b DAC with 10b capacitor array by adopting both the dual sampling technique and the V_{CM}-based switching technique [3]. By switching the reference voltage on the last unit capacitor between (VRT, V_{CM}) instead of (VRT, VRB), additional LSB comparison is allowed. The comparator can be directly combined with this DAC output signal, and the final digital code is generated. In this case, we do not need additional lower capacitors for LSB as in the conventional design. With this V_{CM}-based switching technique in the LSB decision, we can reduce the lower sub-capacitor array by half. As mentioned earlier, we can reduce the MSB 32C capacitors in the main array with the dual sampling technique. And with this V_{CM}-based LSB switching technique, we can also reduce another 32C in the sub-array. As a result, this V_{CM}-based LSB switching technique, together with aforementioned dual sampling technique, allowed us to implement a 12-bit ADC with a 10-bit capacitor array DAC as shown in Fig. 3(c). Total number of the capacitor array with this V_{CM}-based LSB switching technique, together with the dual sampling technique, is 128Cs for differential operation. Compared to the conventional design of Fig. 3(a), this technique reduces the total DAC capacitor array by half.

Since the dual sampling technique and V_{CM}-based LSB switching technique reduces the capacitor array by two times, these reduced capacitors in a DAC inherently reduce the switching energy by two times. Moreover, we can save more switching energy by applying top plate sampling and also by adopting a proposed low switching energy technique. Fig. 4(a) shows the conventional switching process of a three-bit DAC as an example.

In the sampling periods, VIN is sampled at the bottom plate of the capacitor arrays. During the first conversion process in the holding periods, the MSB capacitors are switched to VRT and other capacitors are connected to VRB in the upper array of the DACP. And reverse reference voltages are also connected in the lower array of the DACN. In this case, all the capacitors are switched to the reference voltage, and hence, consume the switching power of $4CV^2$. Also, during the second and third conversion processes in the holding period, this conventional switching technique consumes more switching energy, as shown Fig. 4(a).

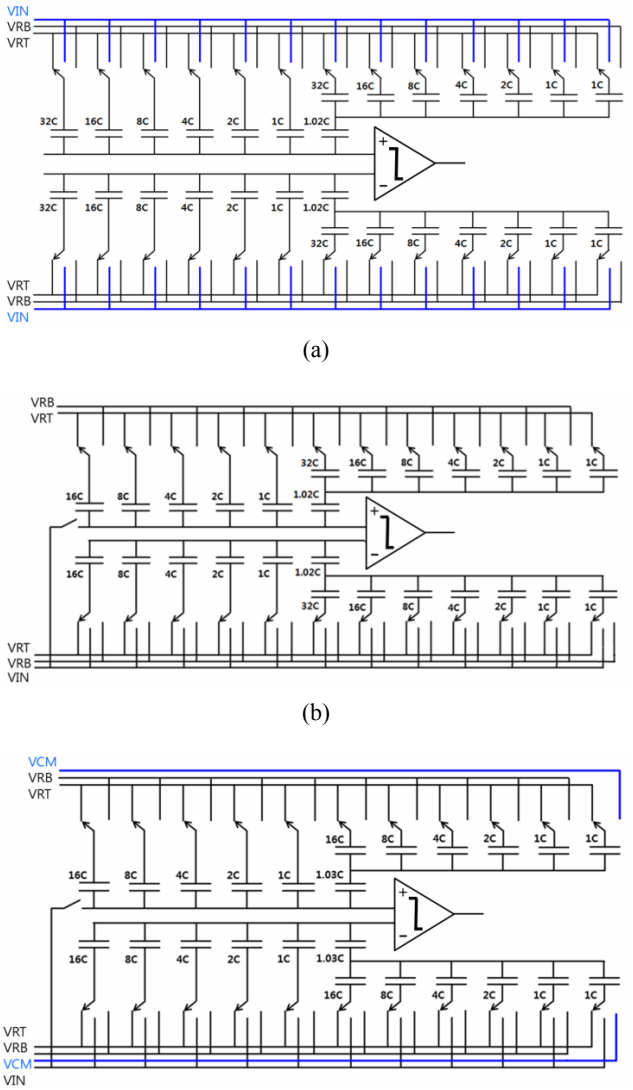

Fig. 3. (a) Conventional 12b differential DAC, (b) 12b DAC with a dual sampling technique, (c) the proposed 12b DAC with 10b capacitor array by using a V_{CM}-based switching technique together with a dual sampling technique.

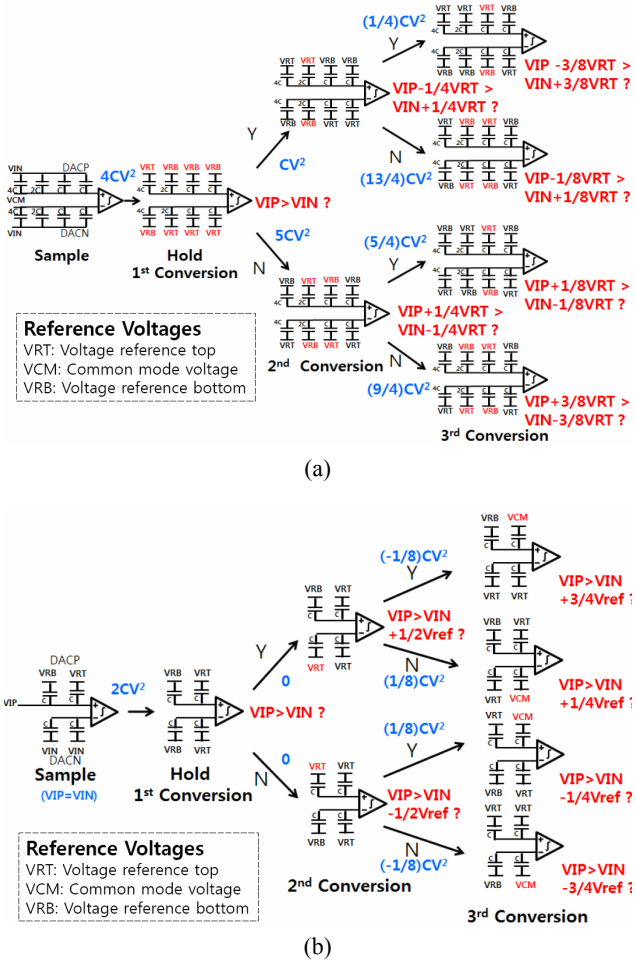

Fig. 4. (a) Conventional switching process with 3b DAC example, (b) proposed low switching energy process with 3b DAC example.

Fig. 4(b) shows the process of the proposed low switching energy technique with a three-bit DAC as a conceptual example. If both VIP and VIN are sampled at the top plate of each capacitor array, there we have zero switching energy during the first conversion. But, due to the single-to-differential operation in the sampling period in this application, the VIN in DACN is not sampled at the top-plate. This first conversion needs the switching energy of 2 CV^2 for the MSB decision in the first cycle. But for the remaining LSB decisions, we need zero switching energy in the second conversion cycle and $1/8CV^2$ in the third conversion cycle, as shown Fig. 4(b).

Fig. 5 shows a circuit diagram of the dynamic comparator that we used. It has a preamp followed by a dynamic latch. The comparator was optimized to have low noise and also to have high accuracy.

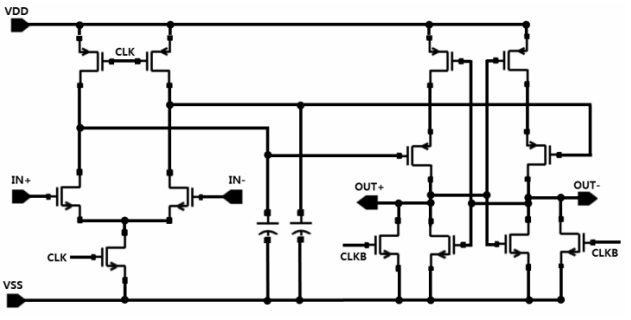

Fig. 5. Circuits of dynamic comparator.

4. Simulation Results and Performance Summary

The proposed 12b SAR ADC was designed with 0.35μm bipolar CMOS LDMOD (BCDMOS) technology. The fast Fourier transform (FFT) simulation results are shown in Fig. 6 with an input signal of 14.3KHz and a sampling frequency of 1.25MHz. The proposed ADC achieves an SNDR of 70.75dB, an SFDR of 83.28dB, and an ENOB of 11.46 bits. The core area, as shown in Fig. 7

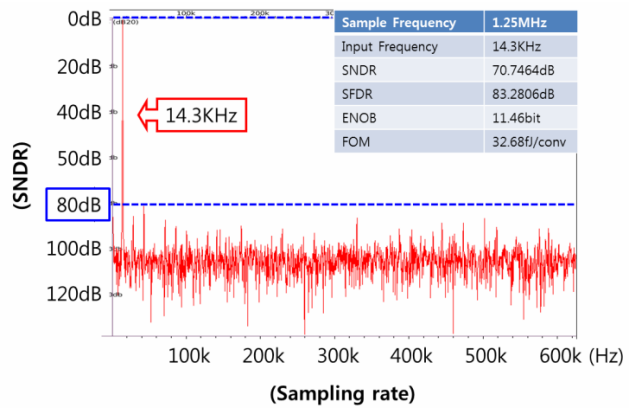

Fig. 6. FFT simulation results (4096 point).

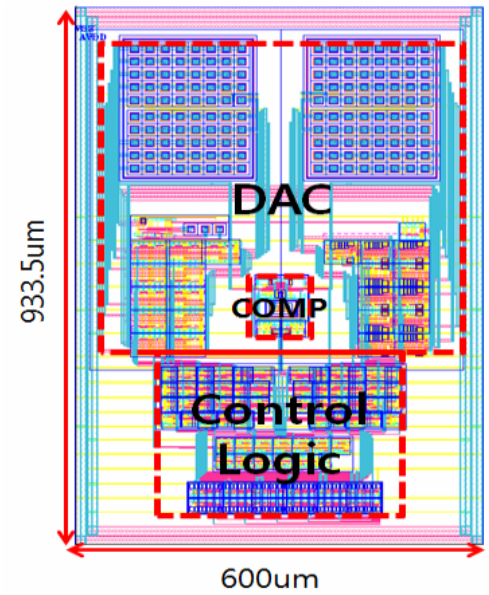

Fig. 7. Chip layout (w/o pad).

Table 1. Performance Summary.

Parameters	Values
Process	BCDMOS 0.35μm
Resolution	12 bits
Power Supply	3.3V
Sampling Rate	1.25MHz
Input Signal Voltage Range	0 ~ 3.3V
Power Consumption	34.8μA (at 3.3V)
SNDR/SFDR	70.75dB / 83.28dB
ENOB	11.46 bits
FoM	32.68 fJ/conv
Layout Area	664μm * 933.5μm

is 600μm x 935.5μm, excluding pads. The power consumes 115μW at a sampling frequency of 1.25MHz under the supply voltage of 3.3V. And the figure of merit (FoM) is 32.68fJ/conversion-step. We can further reduce power consumption if we adopt asynchronous control. The performance is summarized in Table 1.

5. Conclusion

The 12-bit SAR ADC was designed for DMPPT control in a photovoltaic system. Both a top-plate sampling technique and a V_{CM}-based switching technique are applied to the 12b capacitor digital-to-analog converter. With these techniques, we can implement a 12b SAR ADC with a 10b capacitor array DAC. To enhance the accuracy of the ADC, a single-to-differential converted DAC is exploited with a dual sampling technique during top-plate sampling. A low switching energy technique is also applied to the capacitor DAC.

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