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A 10-bit 10MS/s differential straightforward SAR ADC

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** Regular Paper*

***Abstract*:** A 10-bit 10MS/s low power consumption successive approximation register (SAR) analog-to-digital converter (ADC) using a straightforward capacitive digital-to-analog converter (DAC) is presented in this paper. In the proposed capacitive DAC, switching is always straightforward, and its value is half of the peak-to-peak voltage in each step. Also the most significant bit (MSB) is decided without any switching power consumption. The application of the straightforward switching causes lower power consumption in the structure. The input is sampled at the bottom plate of the capacitor digital-to-analog converter (CDAC) as it provides better linearity and a higher effective number of bits. The comparator applies adaptive power control, which reduces the overall power consumption. The differential prototype SAR ADC was implemented with 0.18µm complementary metal-oxide semiconductor (CMOS) technology and achieves an effective number of bits (ENOB) of 9.49 at a sampling frequency of 10MS/s. The structure consumes 0.522mW from a 1.8V supply. Signal to noise-plus-distortion ratio (SNDR) and spurious free dynamic range (SFDR) are 59.5 dB and 67.1 dB and the figure of merit (FOM) is 95 fJ/conversion-step.

***Keywords*:** SAR ADC, Straightforward, Comparator, CDAC

1. Introduction

High performance analog-to-digital conversion on a nanometer scale is performed according to high-speed switching rather than amplifying. The nature of a successive approximation register (SAR) analog-to-digital converter (ADC) is based on high-speed switching. While low-power characteristics of a SAR ADC have increased the application of this structure, it suffers from low speed because, for each conversion, a large number of decision cycles is required. The necessity for, and interest in, higher speed and lower power consumption for SAR ADCs has given rise to many efforts to increase the speed of these blocks and surpass this drawback. Besides, a lot of techniques are used to decrease the power consumption of these blocks [1-4].

In this paper, we will present straightforward DAC switching for SAR ADCs. Here, the most significant bit (MSB) is decided without any switching energy. The input voltage is sampled at the bottom plate and, in each cycle, the capacitor will switch from common mode voltage (VCM) to source voltage (VDD) or ground (VSS). Unlike the conventional structures, in each cycle, only the next capacitor in the DAC will switch up or down, and the capacitor that has been switched to VDD or VSS in the previous step will remain intact without any switching. So, the switching is always straightforward. This sequence of switching eliminates wasted switching steps and causes lower power consumption. Besides, because in each step, we switch only from VCM to VDD or from VCM to VSS, the speed of charging and discharging the capacitors will increase.

The organization of this paper is as follows. Section 2 proposes a straightforward algorithm for SAR ADCs. A 10-bit prototype SAR ADC using a straightforward switching sequence is implemented in Section 3. Section 4 reports the simulation results, and Section 5 concludes the paper.

2. Straightforward SAR ADC switching sequence

The DAC switching sequence for a three-bit differential straightforward SAR ADC is shown in Fig. 1. This switching algorithm is slightly different than

previously reported Vcm-based structures [1, 2]. In the first step (A), VIP and VIN (differential input voltages) are connected to the bottom plates of the capacitors in CDACY and CDACX, respectively. Besides, the top plates of the CDACs are connected to the VCM. In this step, VX=VCM-VIN and VY=VCM-VIP are sampled in CDACX and CDACY. After sampling (B), the bottom plates of the two CDACs are switched to the VCM. In this step, we will have VX=2VCM-VIN and VY=2VCM-VIP, and the MSB will be decided. If VX>VY (VIP>VIN), then the output of the comparator will be high, and the MSB will be 1; otherwise, it will be 0. For the next cycle, if the MSB is 1, the 2c capacitors in CDACX and CDACY will switch to GND and VREF, respectively (C). In this way, VX will decrease to 2VCM-VIN-VCM/2, and VY will increase to 2VCM-VIP+VCM/2. On the other hand, if MSB is 0, the 2c capacitor in CDACX will connect to VREF, and the one in CDACY will switch to GND and VX=2VCM-VIN+VCM/2, VY=2VCM-VIP-VCM/2 voltages will be available at the input terminals of the comparator (D). After this redistribution is finished, the comparator will decide MSB-1. The sequence for deciding the next bit is similar.

In this structure, the largest capacitor in each CDAC is 2c, which is half of the conventional structures. If we assume a single-ended structure, the number of unit capacitors in a straightforward structure is half of that in a conventional structure. Besides, in each cycle the switching is from VCM to VREF or GND (which, in other recent structures, is from VREF to GND, or vice versa).

The proposed structure for the SAR ADC is called straightforward because, unlike other structures, in each cycle, only the next capacitor in the CDAC will switch to VREF or GND, and the capacitor that was switched in the previous step will remain intact without any switching. It reduces wasted power and increases the speed of the switching. The bottom-plate, sampling-based, straightforward structure can be used for higher resolutions because it provides better linearity in principle [5].

Note that the MSB is decided without any extra switching. The reference voltages for comparison are implemented inside the CDACs.

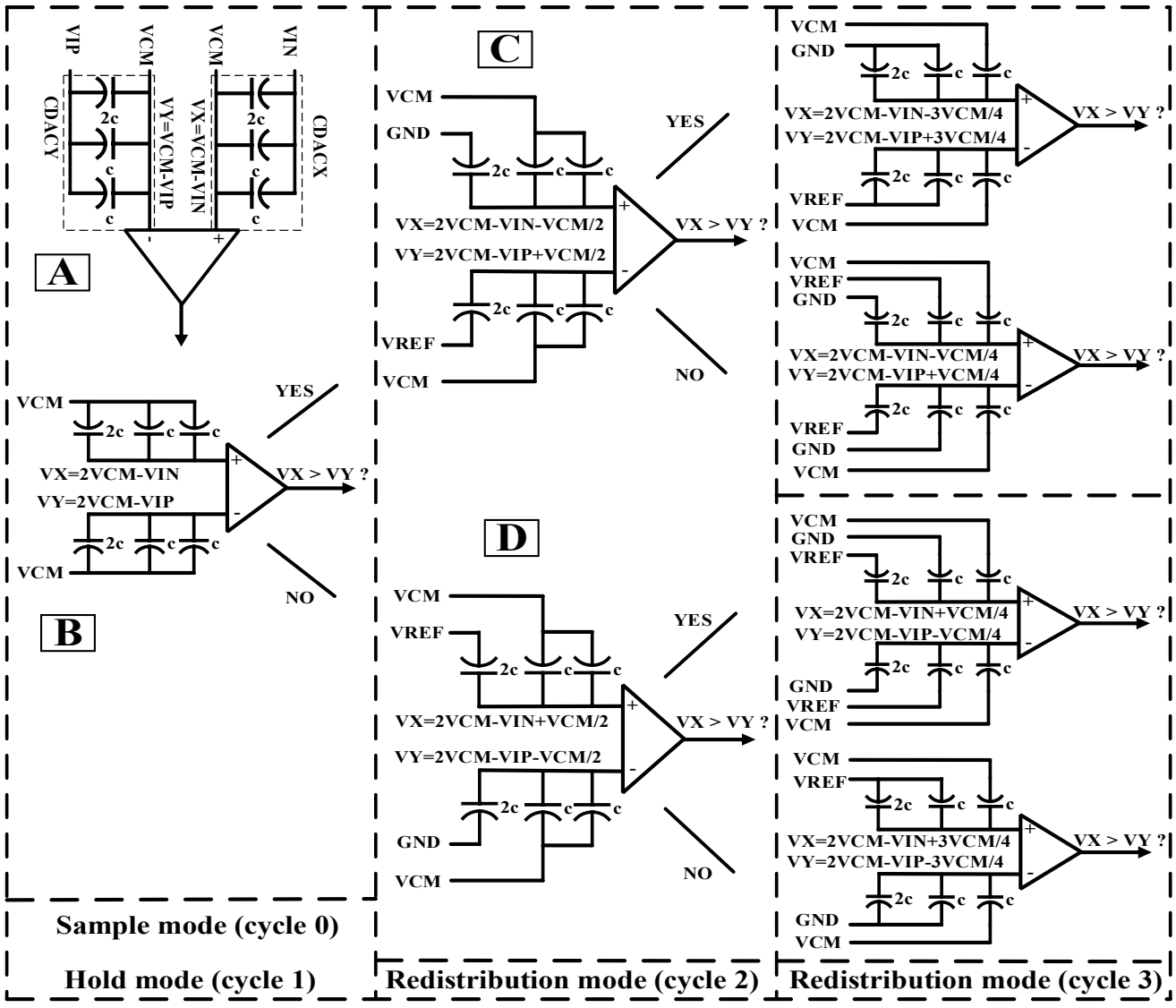

Fig. 1. 3 bit differential straightforward switching sequence.

3. Prototype 10-bit SAR ADC structure

The top block diagram of the proposed SAR ADC is shown in Fig. 2. This is a differential SAR ADC with a straightforward switching sequence. VIN is sampled in CDACX, and VIP is sampled in CDACY. In this structure the inputs are sampled in bottom plates of the capacitors.

In the CDAC structures, unit capacitor values are 29fF, which is limited with the process. The maximum capacitor value in each CDAC is 256c, which is half of the conventional ones. To decide each bit (except MSB), in each CDAC, one of the capacitors switches from VCM to VREFT or VREFB, which is the half their previously reported counterparts. This causes higher speed and lower power consumption. Besides, the decision as to the MSB without charging or discharging an extra capacitor is another reason for the lower power consumption of this structure.

Moreover, in Fig. 2 we can see the timing diagram of the ADC. At the rising edge of the clock, if the reset signal is high, and we have high in the start signal, sampling of the input will start. After sampling is finished, the structure starts to decide the output bits from MSB to the least significant bit (LSB). At each positive edge of the clock, one bit is decided, and after the decision is finished, until the next sampling and bit decision, output of the ADC remains intact unless the reset signal becomes low. A somewhat similar switching structure has been applied [6], but the difference is that the DAC structure is based on a C-R hybrid DAC, which employs a two-step split-capacitor array. The DAC structure we applied does not have the complexity of the above-mentioned structure, and the overall structure has comparable results. Also, according to our simulations, applying a split capacitor array to a DAC structure degrades the linearity of the system.

Fig. 3 presents a block diagram of the comparator [7, 8]. During the reset phase (CLK=0 and CLKD=0), the intermediate nodes (m+, m-) and output nodes (O+, O-) are charged to VREF through M1, M2 and M6, M7, which are turned on by the inputs at around common-mode voltage. In phase 1 during comparison (CLK=1 and CLKD=0), M5 is turned on, and a current path from supply to ground through the dynamic inverter (M1-M4) is created. Furthermore, the intermediate nodes (m+ and m-) are discharged with a time difference (Δt) depending on the comparator's inputs and the skew rate of the dynamic inverters. Also, adaptive power control (APC) has been applied in this comparator. The APC signal reduces the active time of the comparator, which causes total power consumption to be reduced.

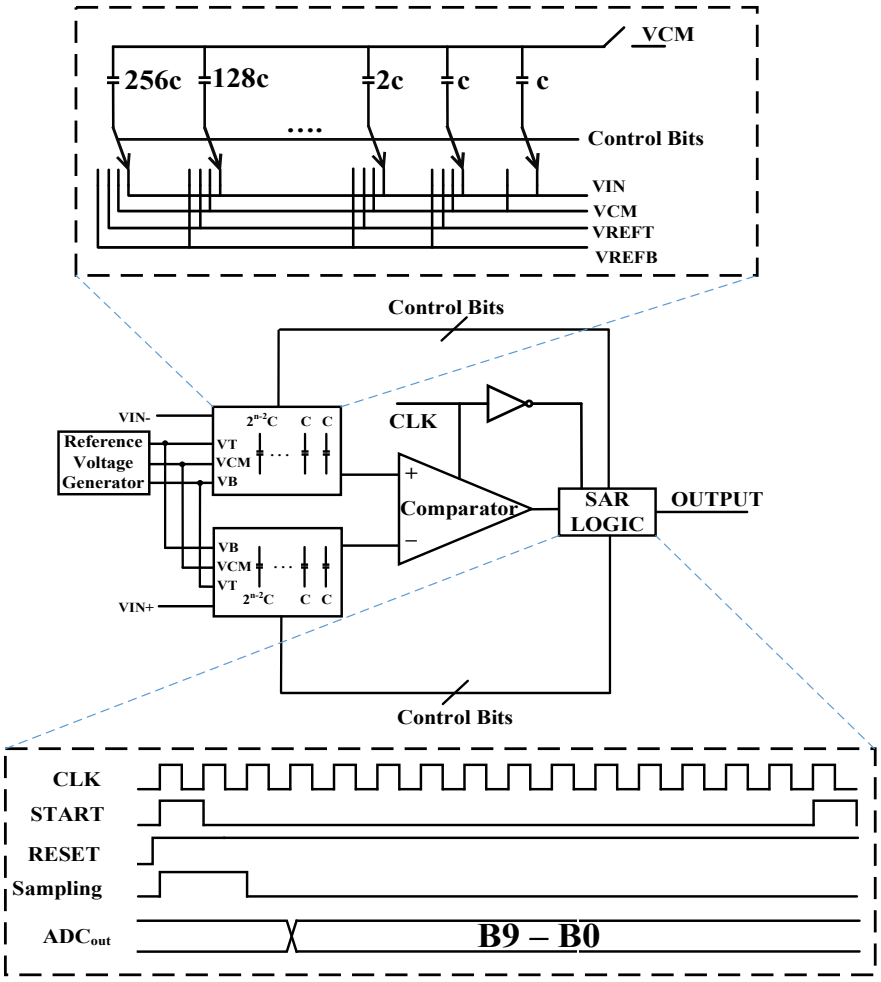

Fig. 2. (a) Top block, (b) Timing diagram of the proposed ADC.

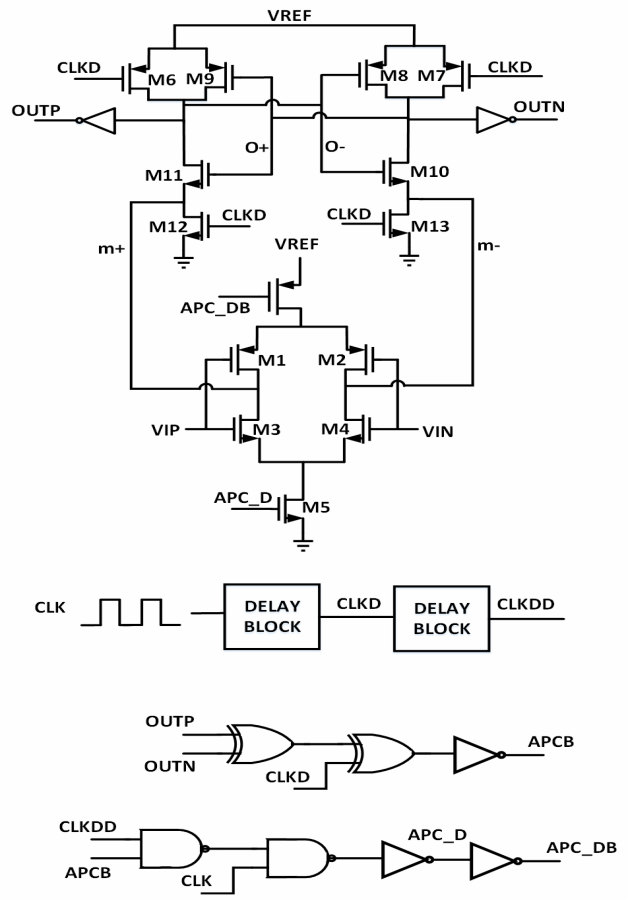

Fig. 3. Comparator structure and APC control.

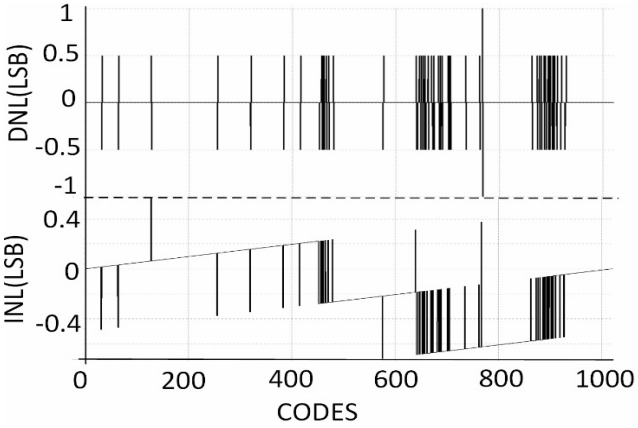

Fig. 4. DC Analysis Results.

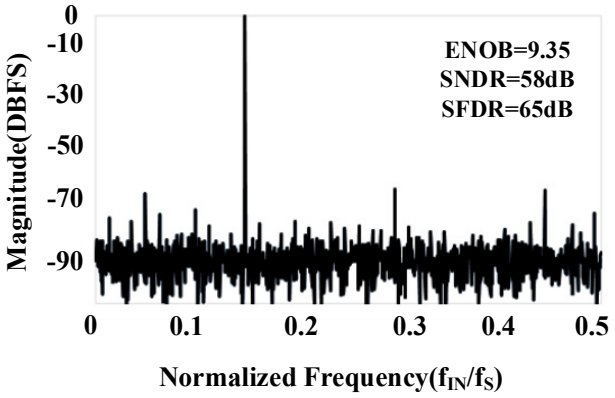

Fig. 5. Spectrum of the output samples for the input 1.5 MHz at 10MS/s.

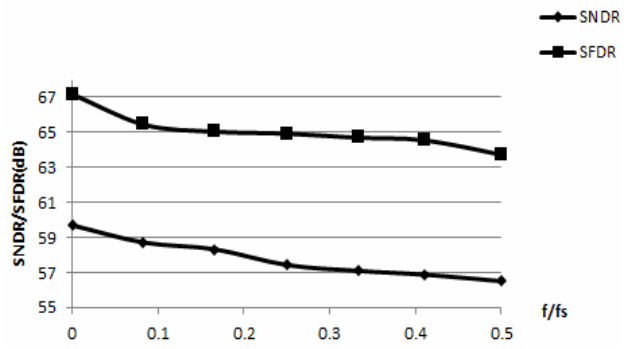

Fig. 6. SNDR and SFDR for the different input ranges from DC to Nyquist rate.

4. Simulation Results

Simulation results for the proposed ADC have been implemented with 0.18-µm CMOS technology. Fig. 4 shows the DC analysis results for this ADC. The DC analysis results that are extracted from ramp simulation are as follows.

DNL max and DNL min are 1.0 and -1.0 LSB, respectively. INL max and INL min are 0.55 and -0.69 LSB, and Sigma DNL and Sigma INL for this structure are 0.152 and 0.287 LSB.

Fig. 5 implements a fast Fourier transform (FFT) of the output. In this simulation, the input is a 1.5MHz sine wave sampled at 10MS/s. The effective number of bits (ENOB) for this simulation is 9.35. SNDR and SNR are 58.02 and 59.98dB, respectively, and SFDR is 64.94dB. This ADC consumes around 290µA from a 1.8V source, so the current consumption of this structure is 522µW. In Fig. 6, SNDR and SFDR for different input frequencies from DC to Nyquist rates have been illustrated. The FOM was calculated to be 95fJ/Conv-step according to the following equation:

$$FOM = \frac{Power}{2^{ENOB} \times \min\{2 \times ERBW, f_s\}} \quad (1)$$

Finally, the summary of the simulation results and comparison is presented in Table 1.

6. Conclusion

In this paper, we have proposed a 10-bit SAR ADC. We applied a straightforward structure for the CDAC and adaptive power control for the comparator, which reduces power consumption. This ADC was implemented with CMOS 0.18-µm technology. The power consumption for this structure is 522µW under a 1.8 V supply. It has 59.5

Table 1. Summary and comparison results.

Parameters	[9]	[10]	This work
Process (nm)	**180**	**180**	**180**
Resolution (bits)	**10**	**10**	**10**
Sampling Rate (MS/S)	**14**	**5**	**10**
Supply Voltage (V)	1.8	1.2	1.8
$ENOB_{Peak}$	9.76	9.12	9.59
$SNDR_{peak}$ (dB)	60.5	56.7	59.5
$SFDR_{peak}$ (dB)	72	67.8	67.1
Sigma DNL (LSB)	0.51	0.32	0.152
Sigma INL (LSB)	0.98	0.42	0.287
Power (mW)	4	3.6	0.52
FOM (fJ/Conv-step)	343	-	95

dB SNDR and 67.1 SFDR under a 10MS/s conversion speed. In this conversion speed for all frequencies from DC to Nyquist rate, the ENOB is above 9.1 bits. The figure of merit is 95fJ/conversion-step.

Acknowledgement

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