

Low Phase Noise CMOS VCO with Hybrid Inductor

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Abstract: A low phase noise CMOS voltage controlled oscillator(VCO) for multi-band/multi-standard RF Transceivers is presented. For both wide tunability and low phase noise characteristics, Hybrid inductor which uses both bondwire inductor and planar spiral inductor in the same area, is proposed. This approach reduces inductance variation and presents high quality factor without custom-designed single-turn inductor occupying large area, which improves phase noise and tuning range characteristics without additional area loss. An LC VCO is designed in a 0.13 μ m CMOS technology to demonstrate the hybrid inductor concept. The measured phase noise is -121dBc/Hz at 400KHz offset and -142dBc/Hz at 3MHz offset from a 900MHz carrier frequency after divider. The tuning range of about 28%(3.15 to 4.18GHz) is measured. The VCO consumes 7.5mA from 1.3V supply and meets the requirements for GSM/EDGE and WCDMA standard.

Keywords: Low phase noise, CMOS VCO, Hybrid inductor, Wide tuning range

1. Introduction

Recently, miniaturized and cost-effective RF transceivers are highly demanded by the worldwide wireless communication market for global mobility and wide coverage of the proposed communication service. Therefore, designing an integrated VCO for multi-standard/multi-band system-on chip(SOC) has attracted considerable interest. 3G/4G communication service requires miniaturized and cost-effective device solution, which can cover different frequency bands. CMOS has become the most favored technology meeting demands such as high data rates, global mobility and wide communication service coverage, because structural complexity and operating speed of silicon integrated circuits are continuously increased by scaling down of CMOS technology. Among the efforts for highly integrated wireless CMOS transceivers, the implementation of building blocks with both wide frequency operability and signal purity is crucial. And single low phase noise multi-band/multi-mode CMOS VCO design is still remain as challenging work [1, 2]. The multiband VCO with wide frequency tunability needs large capacitor banks and varactor diodes, large capacitor banks result in area occupation issue and high VCO gain of varactor results in phase noise degradation issue. Though these problems can be solved by allowing higher power consumption, this is not desirable for total performance of

the SOC. In addition, the larger the value of capacitance, the lower the inductance value, which normally results in low quality factor inductor. Though the custom-designed single turn inductor could have higher quality factor, it should have wide metal strip and occupies larger area than a conventional inductor which is provided by the process design kit(PDK). The silicon area issue has become severer these days since MIMO is basically required for much better uplink/downlink capability. For the MIMO communication system, multi RF transceiver architecture should be integrated in one SOC. Therefore, the size of wideband and low phase noise VCO is the most crucial issue for feasible wireless communication SOC. The bondwire inductor occupies far less area than custom-designed inductor and could be a proper alternative for good quality factor, however it suffers from inductance variation issues which is generated during bonding process and package fabrication.

This paper describes the design of a low phase noise CMOS VCO with wide tunability using hybrid inductor which is composed of bondwire inductor and planar spiral inductor in the same area and is less vulnerable to variation. With a 1.3V power supply, this VCO consumes a 7.5 mA bias current at VCO core and shows frequency tunability from 3.15 to 4.18GHz with low phase noise characteristics. GSM/EDGE and WCDMA bands can be covered by the proposed VCO.

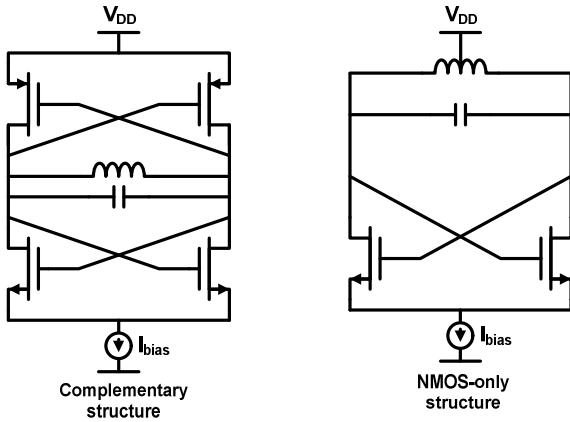


Fig. 1. Two types of CMOS VCO Structures.

2. Hybrid Inductor Structure

A complementary type and an NMOS-only type are mostly favored structure for differential CMOS VCO. Two types of VCO structures are depicted in Fig. 1.

The well-known phase noise model for an oscillator is Leeson’s proportionality [3].

$$L\{\Delta\omega\} \propto \frac{1}{V_o^2} \cdot \frac{kT}{C} \cdot \left(\frac{\omega_o}{Q}\right)^2 \cdot \frac{1}{\omega_m^2} \quad (1)$$

where the phase noise is given by kT/C noise that is shaped in frequency domain by LC tank and normalized to the power in the tank. This expression reveals the dependency of the phase noise upon the signal amplitude V_o . For the complementary type VCO, as the bias current increases, signal amplitude is limited by V_{DD} in the voltage limited regime, while the NMOS-only type VCO enables higher voltage swing above V_{DD} limit. Therefore, the phase noise of the complementary type at each offset frequency may become worse than that of the NMOS-only type as the bias current increases [4]. The complementary type could maintain better phase noise performance for relatively small bias current, but this bias current is not enough to satisfy the requirements for multi-band/multi-standard operation. In addition, considering various lossy components of the real Si circuits, enough phase noise margin is necessary. Accordingly, the NMOS-only type is adopted. This topology has just two MOSFETs for active gm-switching cell, which minimizes parasitics and is really helpful for maximizing frequency tuning range. After selecting optimum FET size considering power consumption and phase noise, the LC tank which is composed of a switched capacitor bank and inductor decide the performance of the multi-band VCO. On the whole, the inductor has lower quality factor than the capacitor bank.

Therefore, a high Q factor inductor is cardinal for low phase noise CMOS VCO design. However, the planar spiral inductor model which is provided by PDK has low Q factor value of around 10. Though thick metal option could help for enhancement of Q factor, it is not enough

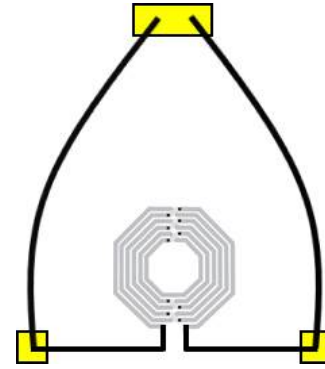


Fig. 2. Hybrid Inductor Structure.

and is normally not provided for the wireless communication SOCs due to the cost issues. A custom-designed planar spiral inductor which has higher Q factor than PDK model is another alternative. A relatively large size single-turn inductor shows Q of around 15 ~ 20. However, very wide metal strip width and out-diameter of around 400 ~ 500 μm is required for high Q inductor. The inductor occupies large area, which is not desirable from the point of view of high density integration.

The bondwire inductor occupies far less area than custom-designed inductor and has a quite good quality factor of above 25, therefore it could be a proper alternative. However it suffers from inductance value variation which is generated during bonding process and package fabrication.

To address these issues, Hybrid inductor which is composed of both bondwire inductor and planar spiral inductor is proposed for both wide tunability and low phase noise characteristics. Two types of inductors are designed to be placed in the same area and are connected in parallel as depicted in Fig. 2. This approach reduces inductance variation and presents high quality factor without custom-designed single-turn inductor occupying large area, which improves phase noise and tuning range characteristics without additional area loss.

Considering the tuning range and Q factor, inductance value of about 1nH is often selected for 2 ~ 6GHz operation. In this research, 1nH Hybrid inductor is composed of a 2nH bondwire inductor and a 2nH conventional spiral inductor. The quality factor of each 2nH inductor is depicted in Fig. 3. The bondwire inductor shows good quality factor above 30 in the frequency range of interest, however conventional spiral inductor which is provided in PDK has low Q of around 12 at 4GHz.

The spiral inductor has peak Q at high frequency above 7GHz and peak Q of the bondwire inductor is at around 3GHz. With parallel connection of these two types of inductors, the hybrid inductor has Q factor value of around 20 and inductance value of about 1nH at 4GHz as shown in Fig. 4. The shunted bondwire inductor and conventional planar spiral inductor are simulated using EM simulator.

The inductance of bondwire is linearly increased with the bondwire length and can be modified with changing the distance between two bondpads and bondwire height. In general, bondwire inductor has 3-D structure and other

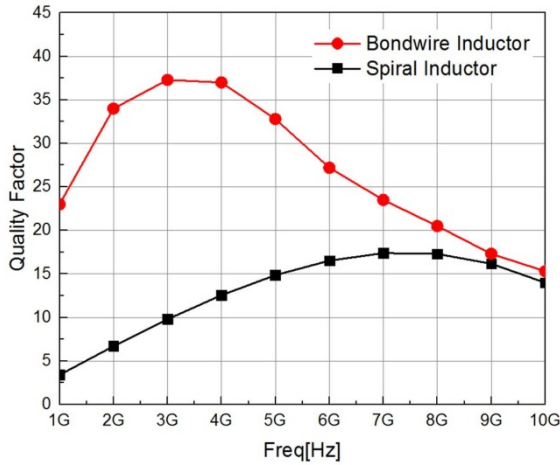


Fig. 3. Quality factor of each inductor structure.

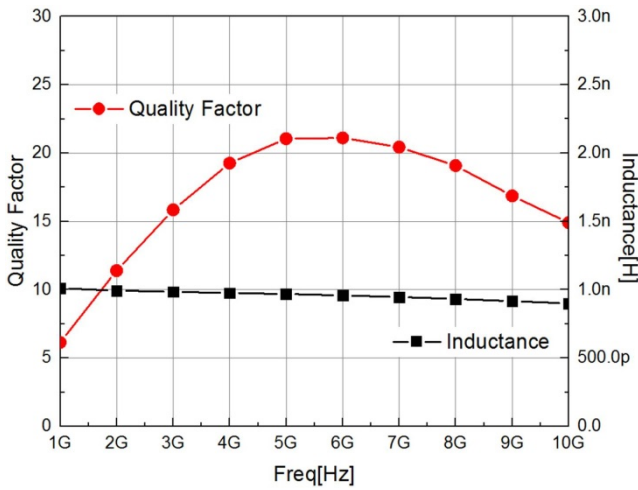


Fig. 4. Quality factor and Inductance for Hybrid Inductor.

circuit blocks such as dividers, buffers and bias blocks could be placed under bondwire inductor. In this research, a conventional planar spiral inductor and periphery circuitry are placed under bondwire inductor.

3. The VCO Circuit Design

The mobile integrated system for quad-band GSM/EDGE and WCDMA requires the VCO having a very wide tuning range and very low phase noise at both close in offset and higher offset from the carrier frequency. Since complex carrier generation structures using a harmonic mixer have various non-ideal effects including harmonics coupling, a simple frequency planning based on only divide-by-two prescaler is favored these days. This simple LO chain structure is the optimum solution to minimize the cost in terms of system complexity, power consumption and area in comparison with other solutions such as quadrature VCO (QVCO) and a polyphase filter. QVCO requires doubling both area and power consumption. The polyphase filter has similar defects to lose dependency on the process variation and mismatches [5].

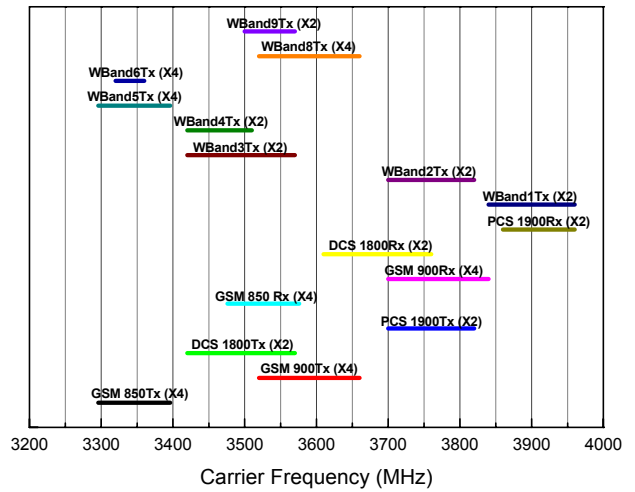


Fig. 5. Frequency planning for the carrier generation of quad-band GSM/EDGE and WCDMA standards.

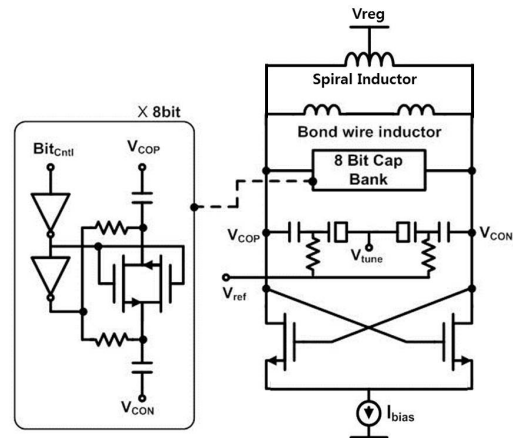


Fig. 6. Proposed VCO structure.

In the simple prescaler only LO chain, even though carrier frequency doubling is needed to generate quadrature I/Q signal, side effects of other structures such as self-mixing, DC-offset and frequency pushing/pulling can be minimized. Fig. 5 depicts a frequency planning for the carrier generation of quad-band GSM/EDGE and WCDMA standards. WCDMA Rx band is included in this frequency planning since WCDMA Tx and Rx are simultaneously active for operation. The VCO with a frequency tuning range of 684MHz, which is from 3296MHz ($GSM850Tx \times 4$) to 3980MHz ($PCS1900Rx \times 2$), is needed for prescaler-only scheme.

In the design of a VCO for wide frequency range standard, it is very difficult to satisfy both wide tunability and phase noise requirement with same LC tank. Proper design of a switched capacitor bank and varactor is required to avoid phase noise degradation and to acquire reasonable K_{VCO} , the vco gain, for stable PLL operation. The proposed VCO structure is shown in Fig. 6. Accumulation-type MOS varactor is used for fine tuning. A binary-weighted 8-bit switched capacitor bank with enough frequency margin is used for coarse tuning to overcome frequency shift due to PVT variations.

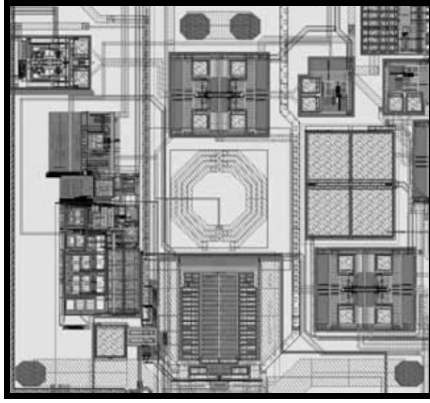


Fig. 7. Complete layout of the proposed CMOS VCO.

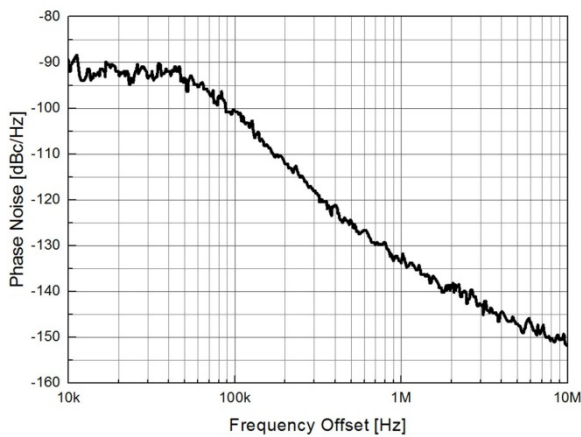


Fig. 8. Measured phase noise of the proposed VCO at 900MHz carrier frequency.

As for the size issue, this VCO structure can save large silicon area by placing two inductors and periphery circuitry in the same position. In the layout of LC VCOs, inductor commonly occupies almost total silicon area. And for minimizing power consumption, the VCO bias current is varied between each frequency band by controlling the 3-bit binary weighted bias resistors. This programmability allows the trade-off between power consumption and phase noise, which is necessary for multi-band/multi-standard VCOs.

4. Measurement Results

Considering these multi-band low phase noise VCO design issues, the VCO is designed with the proposed hybrid inductor in 0.13 um CMOS technology, Fig. 7 shows the complete layout of the VCO. The chip size is $0.7 \times 0.6 \text{ mm}^2$.

The VCO is tunable between 3.15GHz and 4.18GHz. The resulting range is 28% of the mid frequency. The VCO operates from 1.3V supply and biases at 7.5 mA. Fig. 8 plots the measured phase noise for the test VCO with the carrier frequency of 900MHz after 1/4 divider.

The VCO achieves -121dBc/Hz and -142dBc/Hz at 400KHz and 3MHz offset frequencies from the 900MHz

Table 1. VCO performance summary and comparison.

VCO	Tech.	Freq. [GHz]	Power [mW]	P/N [dBc/Hz]	FOM
[6]	0.35um Bi-CMOS	1.91	10	-121 @600KHz	-181.1
[7]	0.35um Bi-CMOS	5.6	13.5	-117 @1MHz	-180.7
[8]	0.13um CMOS	3.0-5.6	2	-114.5 @1MHz	-186.5
[9]	0.35um CMOS	2.19	12.6	-139 @3 MHz	-185.3
This Work	0.13um CMOS	3.15-4.18	9.75	-142 @3 MHz	-181.7

carrier, respectively. The measured frequency tuning range and phase noise performances satisfy Quad-band GSM/EDGE and WCDMA standard requirements. Table 1. shows the summary of the measurement results compared to those of other low phase noise VCOs.

A normalized figure of merit (FOM) has been defined [10] to compare the VCO performance with other VCOs as

$$FOM = L(\Delta\omega) \left[\frac{dBc}{Hz} \right] + 10\log\left(\frac{P_{DC}}{1mW}\right) - 20\log\left(\frac{\omega_0}{\Delta\omega}\right) \quad (2)$$

where $L(\Delta\omega)$ is the total single-sideband phase-noise spectral density at an offset frequency $\Delta\omega$, P_{DC} is total VCO power consumption, and ω_0 is the frequency of oscillation. The calculated FOM of this VCO is about -181.7 dBc/Hz at 3MHz offset. Considering the wide tuning range of 28%, this FOM is quite comparable to the previously published results.

5. Conclusion

In this paper, a low phase noise CMOS VCO with Hybrid inductor for multi-band/multi-standard RF Transceivers is presented. The proposed VCO has wide frequency tunability through hybrid inductor structure, which is composed of bondwire inductor and spiral inductor. These two inductors are placed in the same position, which saves large silicon area. This approach reduces total inductance variation and presents high quality factor without custom-designed single-turn inductor occupying large area.

The design has been achieved with 0.13um CMOS process. An NMOS-only structure, high Q bond wire inductor and conventional planar spiral inductor are adopted for enough frequency tuning range, good phase noise characteristics, and chip area efficiency. In addition, programmable 3-bit bias resistors are used for a trade-off between phase noise and power consumption. Proposed hybrid inductor structure enables wide frequency tunability and low phase noise characteristics. The measured results show the tuning range of about 28%(3.15 to 4.18GHz) and the phase noise of -121dBc/Hz at 400KHz offset and -

142dBc/Hz at 3MHz offset from a 900MHz carrier after 1/4 divider. The VCO consumes 7.5mA from 1.3V supply and meets the requirements for GSM/EDGE and WCDMA standard. These values confirm that a good tradeoff among phase noise, wide tunability and silicon area efficiency is achieved by the proposed CMOS VCO with hybrid inductor.

Acknowledgement

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