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A Capacitor-less Low Dropout Regulator for Enhanced Power Supply Rejection

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** Regular Paper*

Abstract: Various power supply noise sources in a system integrated circuit degrade the performance of a low dropout (LDO) regulator. In this paper, a capacitor-less low dropout regulator for enhanced power supply rejection is proposed to provide good power supply rejection (PSR) performance. The proposed scheme is implemented by an additional capacitor at a gate node of a pass transistor. Simulation results show that the PSR performance of the proposed LDO regulator depends on the capacitance value at the gate node of the pass transistor, that it can be maximized, and that it outperforms a conventional LDO regulator.

Keywords: Low dropout, Regulator, Power supply rejection, Capacitor-less

1. Introduction

Low dropout (LDO) regulators are essential for analog circuits in mobile devices that require a clean power supply. The power supply of a system integrated circuit (IC) is usually stepped down by using buck converters in a switched mode power supply (SMPS). Then, an LDO regulator cascaded with the SMPS provides clean power to analog circuits. With the growing trend of external capacitor-less design of an LDO regulator, it is essential to have a regulator integrated into a single system IC and to maintain low cost by minimizing the chip size as well. However, a system IC is affected by several power supply noise sources. The output voltage ripple of the SMPS directly affects the performance of the LDO regulator. In addition, the transition of logic levels in high-speed digital circuits causes supply voltage bouncing. These power supply noises appear from a few hundred kilohertz to a few megahertz [1].

To minimize power supply noise from these sources, an LDO regulator needs superior power supply rejection (PSR) performance for frequencies up to a few megahertz. There are several techniques to achieve high PSR performance without using an off-chip capacitor. A supply noise shielding technique using a negative metal oxide semiconductor (NMOS) cascode transistor was used [2]. Since the NMOS cascode transistor with its gate biased separately acts like a source follower, it shields the entire regulator from fluctuations in the power supply. But this technique is not suitable for most applications because of high dropout voltage and bad transient response. A feed-forward supply-noise cancellation (FFNC) technique was used [3]. However, as a widely used solution, this technique is no longer available, because it is very sensitive to input voltage and load current variation. Moreover, supply noise is partially cancelled according to the control voltage that determines the gain of the feed-forward amplifier. Ho and Mok [4] proposed an LDO regulator composed of a band-pass filter and summing amplifier to enhance power supply rejection. But, its ripple rejection accuracy is limited due to passive elements of the filter. Moreover, the PSR enhancement in high frequency regions was trivial. The feed-forward current injection technique was introduced [5], which achieves significant PSR enhancement in the 0.4-4 MHz range at the expense of an additional complex circuit block to minimize mismatch between the scaled transistor and the current amplifier ratio for direct dependency of PSR performance to the ratio.

We analyzed a new PSR enhancing scheme that consists of an additional capacitor at the gate node of a pass transistor. Since the additional capacitor is related to parasitic capacitance at the gate node of the pass transistor, frequency response of the gate-source voltage of the pass

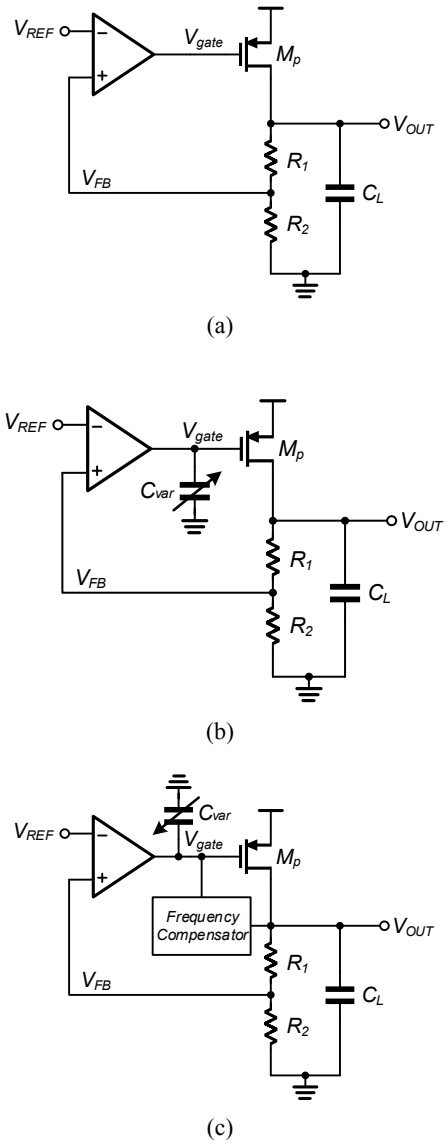


Fig. 1. Fundamental blocks of (a) the conventional LDO regulator, (b) an LDO regulator with an additional capacitor, (c) the proposed LDO regulator.

transistor is changed. Therefore, the PSR performance of the LDO is changed by its additional capacitance value.

This paper is organized as follows. The design considerations for fundamental circuit blocks are reviewed in Section 2, and the proposed PSR enhancing scheme is reviewed in Section 3. Simulation results and discussion of the effect of the proposed scheme are presented in Section 4. Finally, comparisons of the proposed LDO regulator with others follow with our conclusion in Section 5.

2. Design Considerations

Fig. 1(a) shows fundamental blocks of a conventional LDO regulator composed of an error amplifier, a pass transistor, and passive elements. Fig. 1(b) shows an additional capacitor added at the gate node of the pass transistor in order to enhance PSR performance. But the stability of this circuit can be degraded. Therefore, the

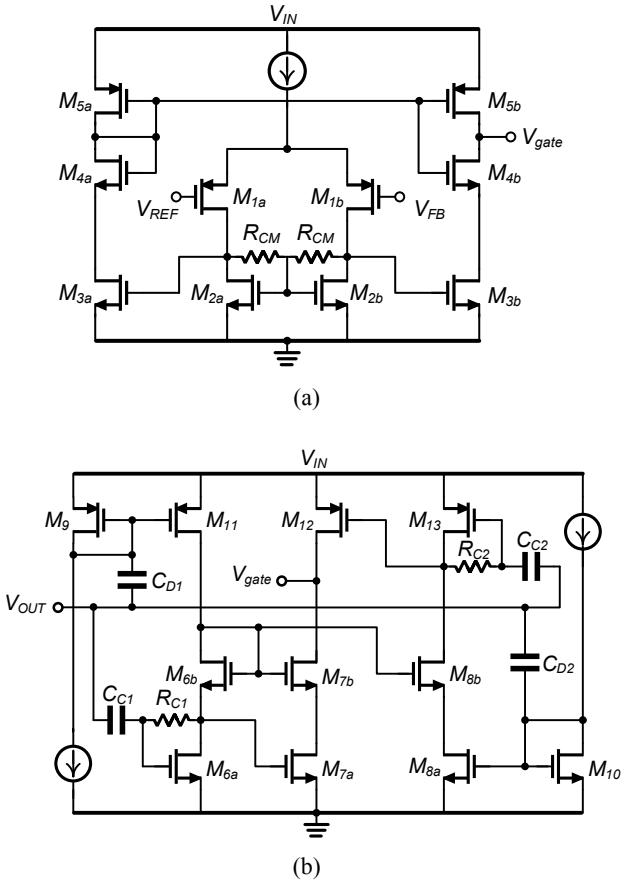


Fig. 2. Circuit implementation of (a) error amplifier, (b) frequency compensator [5, 6].

proposed LDO regulator includes a frequency compensator to enhance the frequency response, as shown in Fig. 1(c).

A circuit implementation of the error amplifier is depicted in Fig. 2(a). Differential gain of the single-ended two-stage error amplifier with a fully differential input stage is tuned by the common-mode resistor R_{CM}. High-frequency PSR affected by the error amplifier is minimized by using a symmetrical structure. To improve the matching between M_{3a} and M_{3b} and to increase the output impedance, cascade transistors M_{4a} and M_{4b} are added to the second stage of the error amplifier. The conventional structure of a frequency compensator as shown in Fig. 2(b) is adapted to the proposed LDO regulator for a phase margin higher than 60°, which compensates loop stability with a differentiator and a gain stage that generate a frequency compensating zero [5, 6].

3. The Proposed Scheme

3.1 Conventional PSR Enhancing Scheme

Fig. 3 shows a small signal model of the conventional LDO regulator [5]. The main factor for PSR limitation at high frequencies of the conventional LDO regulator is the supply voltage coupled through the gate-source and the gate-ground parasitic capacitances of the pass transistor.

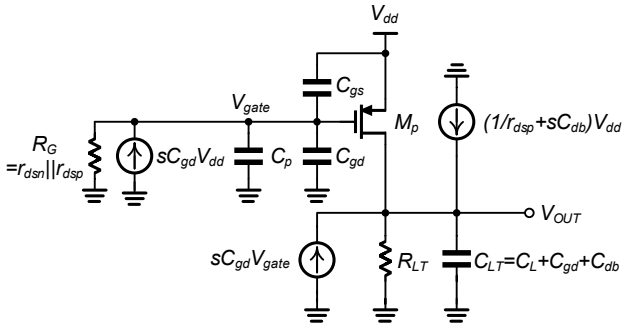


Fig. 3. Small-signal equivalent circuit of the conventional LDO regulator [5].

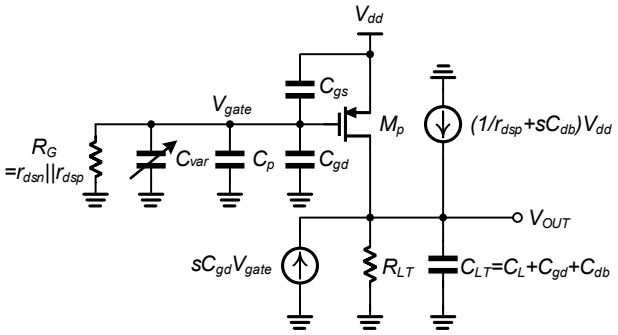


Fig. 4. Small-signal equivalent circuit of the proposed LDO regulator.

The coupled gate-source voltage from the supply is converted into current through the pass transistor. Then, the output voltage of the LDO regulator is affected by the supply noise, resulting in degradation of PSR performance at high frequencies. The gate voltage as a function of supply voltage V_{dd} can be approximated as

$$V_{gate} = \frac{s(C_{gs}+C_{gd})}{\frac{1}{R_G}+s(C_p+C_{gs}+C_{gd})}V_{dd} \cong \frac{C_{gs}+C_{gd}}{C_p+C_{gs}+_{gd}} \cong V_{dd} \quad (1)$$

where C_p, C_{gs}, and C_{gd} represent the parasitic capacitances of the error amplifier, of the gate-source, and the gate-drain, respectively. R_G indicates output resistance of the error amplifier. $1/R_G$ and C_p can be ignored since R_G is large enough, and the sum of C_{gs} and C_{gd} are much bigger than C_p. Note that the gate-source voltage $V_{gs}(= V_{dd} - V_{gate})$ is small enough to be neglected. Thus, the fluctuation of the supply voltage does not affect the output node. But complex circuits are needed to implement the voltage controlled current source, $sC_{gd}V_{dd}$, and a mismatch problem also exists.

3.2 Proposed PSR Enhancing Scheme

The proposed PSR enhancing scheme is described as follows. The aforementioned noise modulation of the gate voltage can easily be removed by an additional capacitor at the gate node of the pass transistor. Fig. 4 shows the small-signal equivalent circuit with additional capacitor C_{var} connected between the gate node of the pass transistor and the ground. The gate-source voltage of the pass transistor can be neglected by choosing the optimum value of C_{var}, which leads to enhanced PSR at high frequencies.

The gate voltage as a function of supply voltage V_{dd} of the proposed LDO regulator can be approximated as

$$V_{gate} = \frac{sC_{gs}}{\frac{1}{R_G}+s(C_p+C_{gs}+C_{gd})+sC_{\text{var}}}V_{dd}$$

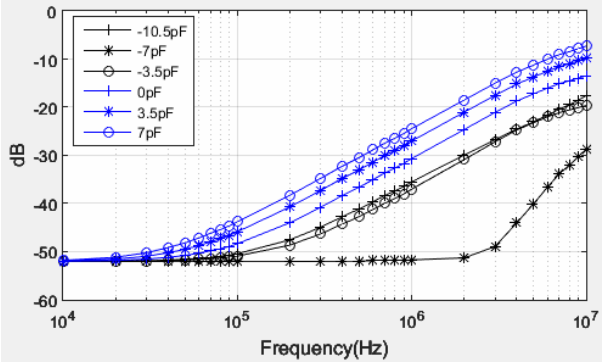
$$\cong \frac{sC_{gs}}{s(C_p+C_{gs}+C_{gd}+C_{\text{var}})}V_{dd} = V_{dd} \quad (2)$$

If the capacitance value of C_{var} is adjusted to $-(C_p+C_{gd})$, C_p and C_{gd} in the denominator cancel out.

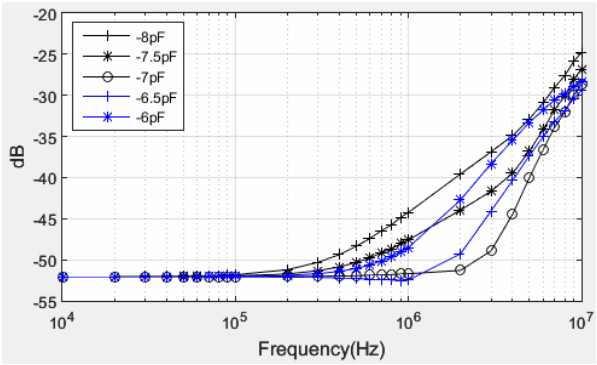
4. Simulation Result

The proposed LDO regulator is simulated with 0.18 μm complementary metal-oxide semiconductor (CMOS) technology. Regulated output voltage of the LDO regulator is 1.6 V for an input voltage ranging from 1.8 V to 2.6 V, and its minimum dropout voltage is 200 mV. The capacitance of the load is 20 pF, and maximum load current is 50 mA. Four 1.3 pF on-chip capacitors are used for both frequency compensation and fast slew. The sum of on-chip capacitor values is 25.2 pF, which includes the 20 pF load capacitor. Fig. 5(a) depicts the simulated PSR with different values of C_{var} at a load current of 50 mA. The PSR performance of the proposed LDO regulator with fine values of C_{var} is shown in Fig. 5(b), which indicates the best performance of PSR at a C_{var} of -7 pF. As a result, in Fig. 5(c), the proposed LDO regulator achieves higher PSR than the LDO regulator without C_{var} by over 20 dB in a 0.9 MHz to 6 MHz range. In particular, it is 25 dB higher at a 2 MHz to 5 MHz range. There is remarkable PSR improvement in the tens of megahertz region that equals the switching frequency of the DC-DC converter and digital circuits. Fig. 6 shows the simulated load step transient response from 0 to 50 mA regulated under 100 ns for the rising and the falling time. The maximum overshoot and undershoot are 88 mV and 164 mV, respectively. The settling time is obtained in less than 1.5 μs. The simulated load regulation is 0.14 mV/mA. The simulated line regulation for an input variation from 1.8 V to 2.6 V is regulated under 500 ns for rising and falling times, as shown in Fig. 7. The maximum variation of output voltage is 3 mV for a load current of 50 mA, and the simulated line regulation is 1.45 mV/V.

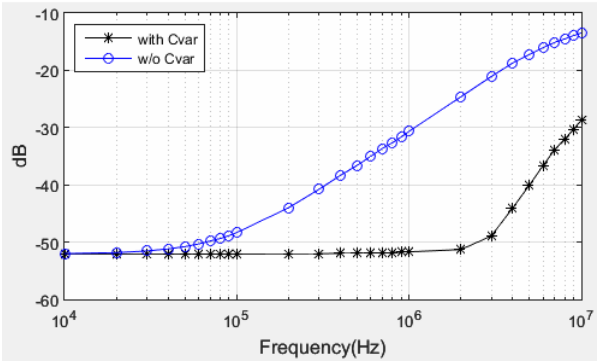
Performance comparisons between the proposed LDO regulator and other capacitor-less LDO regulators is listed in Table 1. Park et al. [5] achieved the best PSR performance. However, a large total on-chip capacitor, 128 pF, is needed, which occupies 45% of its active area. The proposed LDO regulator exhibits the second-best PSR performance among the others. Since the least total capacitance, 32.2 pF, is used, a smaller area can be achieved, compared to the Park et al. scheme [5].



(a)



(b)



(c)

Fig. 5. Simulated PSR (a) with coarse values of C_{var}, (b) with fine values of C_{var}, (c) with and without C_{var}.

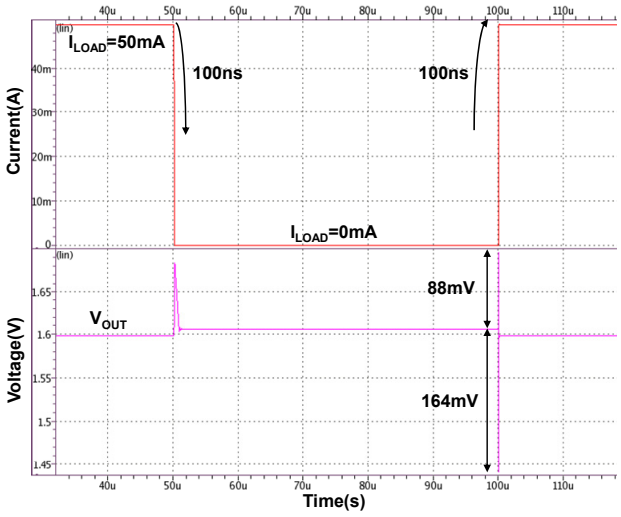


Fig. 6. Simulated load transient response for a load current step of 50Ma.

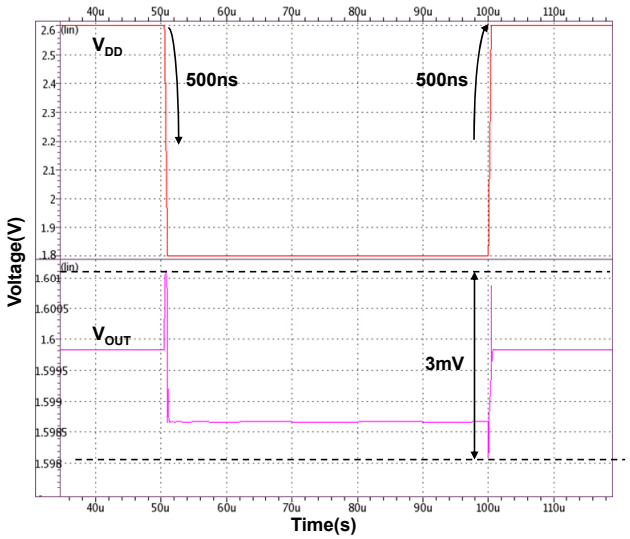


Fig. 7. Simulated line transient response for an input variation of 1.8 to 2.6V.

Table 1. Performance Comparison.

		[2], 2007	[3], 2011	[4], 2012	[5], 2014	[6], 2007	this work
Technology (μm)		CMOS 0.6	CMOS 0.18	CMOS 0.13	CMOS 0.18	CMOS 0.35	CMOS 0.18
Max. load (mA)		5	25	50	50	50	50
V_{OUT} (V)		1.2	1.5	1	1.6	2.8	1.6
V_{DROP} (mV)		600	300	200	200	200	200
I_Q (μA)		80	300	37.32	80	65	80
Load capacitor (pF)		10	25	20	100	100	20
Total on-chip capacitor (pF)		58	125	41	128	123	32.2
PSR (dB)	**@1MHz**	-40	-40	-40	-70	-36	-52
	@10MHz	-30	-22	-15	-36	-5	-29
ΔV_{OUT} (mV)		192	N/A	56	75	90	103
FOM* (ns)		0.006144	N/A	0.000017	0.000264	0.000234	0.000066

*FOM=(C_{OUT} x ΔV_{OUT} x I_Q)/($I_{MAX.LOAD}$)^2

5. Conclusion

A capacitor-less LDO regulator for enhanced PSR is proposed at the expense of an additional capacitor at the gate node of a pass transistor. The proposed LDO regulator is simulated with 0.18 μm CMOS technology, and simulation results show the optimum value of the capacitor gives a PSR better than -40 dB up to 5 MHz with a 50 mA load current. Compared to a conventional LDO regulator, regulator is 25.2 pF, including the load capacitor of 20 pF.

the proposed LDO regulator improves PSR by more than 20 dB in a frequency range of 0.9 MHz to 6 MHz. The total on-chip capacitor required for the proposed LDO Because of both the high PSR performance at higher frequencies and the smaller on-chip capacitor, the proposed LDO regulator can be widely used for low-cost applications requiring high power supply rejection.

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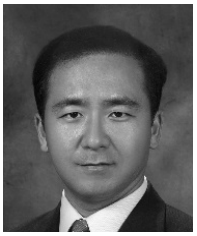

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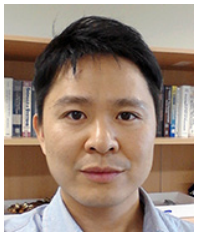

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