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A Stability-Secured Loop Bandwidth Controllable Frequency Synthesizer for Multi-Band Mobile DTV Tuners

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** Short Paper*

Abstract: A broadband radio frequency synthesizer for multi-band, multi-standard mobile DTV tuners is proposed, it's loop bandwidth can be calibrated to optimize integrated phase noise performance without the problem of phase noise peaking. For this purpose, we proposed a new third-order scalable loop filter and a scalable charge pump circuit to minimize the variation in phase margin during calibration. The prototype phase-lock loop is fabricated in 180nm complementary metal-oxide semiconductor shows that it effectively prevents phase noise peaking from growing while the loop bandwidth increases by up to three times.

Keywords: Frequency synthesizer, Phase-lock loop (PLL), Loop filter (LF), Loop bandwidth (LBW), Charge-pump circuit (CPC), Phase noise peaking

1. Introduction

Broadband radio frequency synthesizers for multi-band, multi-standard mobile DTV tuners require stringent integrated phase noise (IPN) or phase jitter specifications to support complex baseband demodulation [1, 2]. Also, it is more important that the uniform performance of IPN must be retained against the voltage-to-frequency gain of the voltage-controlled oscillator (VCO) and the phase-lock loop (PLL) multiplication factor, as both experience a wide range of variation over broadband.

Typically for this purpose, calibration of loop bandwidth (LBW) is applied to each band to suppress phase noise particularly close-in phase noise and spurs to get the optimal IPN. In many cases, such calibration is achieved by controlling charge-pump circuit (CPC) current, since it affects only the LBW, unlike resistors in a loop filter. However, calibrating LBW while confined within poles and zero fixed by passive filters causes an issue of excessive jitter peaking around the LBW, because open-loop phase margin is degraded more as LBW approaches to the poles or zero more closely.

The effect of jitter peaking, intense as marginal stability is reached, is one of the main factors that degrade IPN performance. So, the LBW should be controlled within a range where stability must not be degraded.

To avoid the issue of stability, we propose a stability-secured LBW-controllable PLL with a pole-zero scalable loop filter and a current-scalable CPC. When these two circuits are combined with a common bias source, the proposed PLL provides LBW calibration while keeping a constant phase margin. In this paper, we present a second-order scalable loop filter, including third-order filter conversion and its application for the fractional-N frequency synthesizer with a MASH 1-1-1 sigma-delta modulator (SDM).

2. Circuit implementation

Fig. 1 shows a frequency synthesizer designed with a fractional-N PLL to support the multi-band receiver including Frequency Modulation (FM), Terrestrial Digital Multimedia Broadcasting (T-DMB), Digital Video Broadcasting-Handheld (DVB-H), and Integrated Services Digital Broadcasting-terrestrial (ISDB-T), where VCO needs to cover 2.4GHz to 3.6GHz if we use a Local Oscillator (LO) planning based on the divider-by-2 circuit only.

The designed frequency synthesizer is composed of a Phase Frequency Detector (PFD), the second-order scalable loop filter, a scalable CPC, a first-order passive

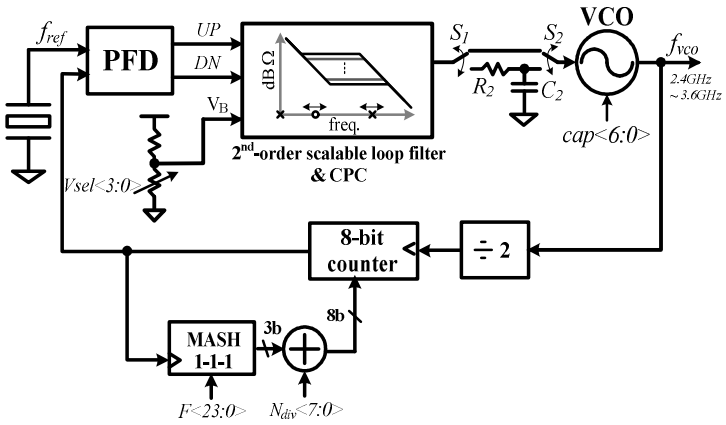


Fig. 1. A block diagram of the proposed frequency synthesizer.

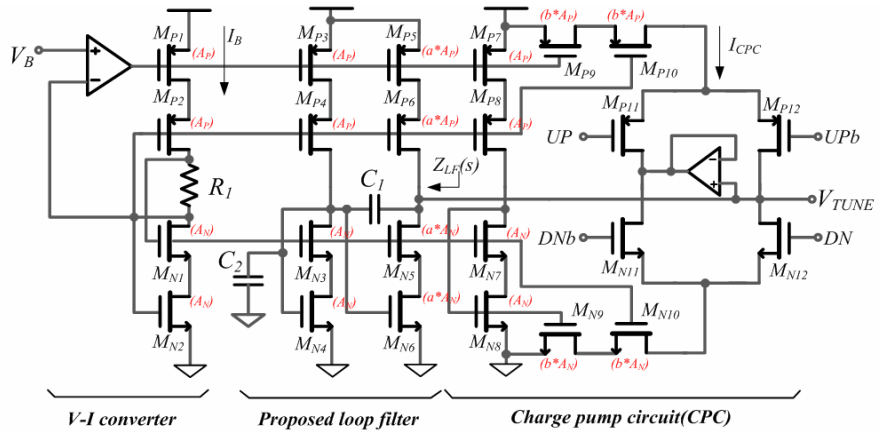


Fig. 2. The proposed second-order scalable loop filter and scalable CPC.

filter, a VCO, dividers, and a MASH 1-1-1 sigma-delta modulator. The VCO is designed with a complementary g_m cell and a seven-bit binary-weighted capacitor bank to minimize the variation in VCO gain. To avoid a gap between frequency segments, the overlap between adjacent center frequencies of a segment is designed to be 50% or more. Switches S1 and S2 are used to connect the first RC filter for third-order filter conversion, which is required to reject the third-order SDM noise from the MASH 1-1-1.

Fig. 2 shows a circuit diagram of the proposed second-order scalable loop filter and scalable CPC. The original concept was presented by Hwang [3], but this design is enhanced to include a differential CPC so that it solves the problems of voltage headroom and glitch-induced spur by charge sharing.

The proposed circuit is composed of a V-to-I converter, loop filter core, and CPC. In the V-to-I converter, the input voltage (V_B) is converted to the basic current (I_B) and M_{N2} is a replica transistor of M_{N4}, so we can change g_m as well as I_D of the M_{N4} through M_{N2} indirectly. The variables, a and b, represent the size multiplication factor of the corresponding branches in terms of the basic aspect ratios: $A_P=W_p/L_p$ in a positive-channel metal oxide semiconductor and $A_N=W_n/L_n$ in a negative metal oxide semiconductor. The loop filter core provides the given second-order characteristics as follows, where the output resistance seen in M_{N5} and M_{P6} is assumed to be large enough for simplicity of calculation.

$$Z_{LF}(s)=\frac{v_{LF}(s)}{i_{LF}(s)}=\frac{(C_1+C_2)/C_1}{1+a}\cdot\frac{1}{g_{m,M_{N4}}}\cdot\frac{1+s/\omega_z}{(s/\omega_z)(1+s/\omega_p)} \quad (1)$$

$$\omega_z=\frac{g_{m,M_{N4}}}{C_1+C_2}=\frac{\mu_n C_{ox}A_N(V_B-V_T)}{C_1+C_2} \quad (2)$$

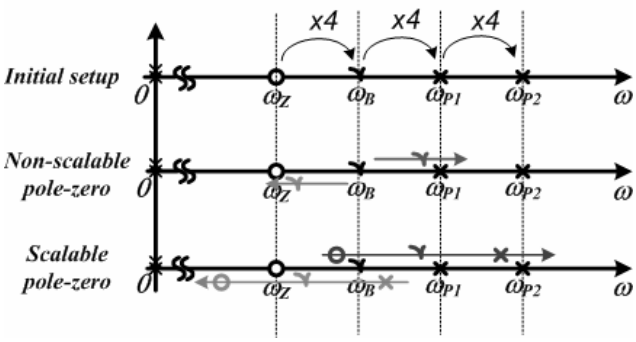
$$\omega_p=\frac{(1+a)g_{m,M_{N4}}}{C_2}=\frac{\mu_n C_{ox}(1+a)A_N(V_B-V_T)}{C_2} \quad (3)$$

where ω_z and ω_p are the zero and the non-zero poles in radian frequency, respectively.

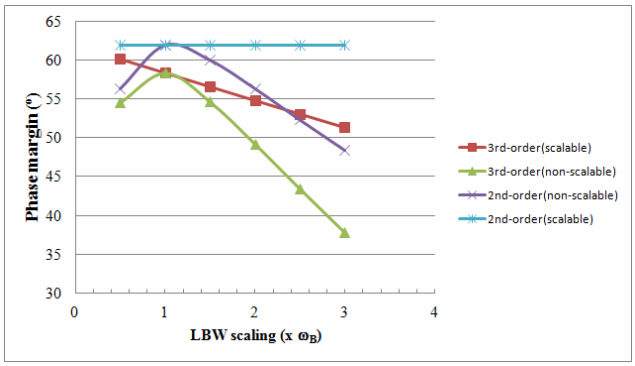
The whole transfer function ($H_T(s)$) including CPC current can be calculated as

$$H_T(s)=I_{CPC}\cdot Z_{LF}(s)=\left[\frac{(C_1+C_2)}{C_1}\cdot\frac{b}{1+a}\cdot\frac{(V_B-V_T)}{2}\right]\cdot\frac{1+s/\omega_z}{(s/\omega_z)(1+s/\omega_p)}$$

This equation results in the loop bandwidth (ω_B) in radians as follows:



(a)



(b)

Fig. 3. The effect of the scalable loop filter on phase margin (a) conceptual diagram for LBW location within pole and zero, (b) phase margin vs. LBW scaling.

$$\omega_B = (1+\frac{C_2}{C_1})\cdot\frac{K_0}{N_{div}}\cdot\frac{b}{1+a}\cdot\frac{V_B - V_T}{2} \quad (4)$$

where VCO gain and the frequency multiplication factor are K_O and N_{div}, respectively.

With this set of equations, we can say that the fractional ratios between ω_z, ω_{p1}, and ω_B are kept constant, independent of scaling ω_B, and therefore, phase margin can be constant. Also, the proposed circuit saves silicon area because it reuses capacitor C_2 with its value rescaled by $1/(1+a)$ for the pole composition, while the sum of C_1 and C_2 builds up the zero.

As another remarkable advantage, the proposed second-order scalable loop filter can be easily converted into a third-order one by adding a series RC filter as shown in Fig. 1, which provides an additional fixed pole at ω_{p2} ($\sim 1/R_2C_2$).

We can analyze the effect of the second-order scalable filter on phase margin in the third-order filter by a comparison with a passive filter having fixed poles and zero.

Fig. 3(a) shows a conceptual diagram that represents locations of poles and zero in the open-loop transfer function of the PLL with the third-order loop filter having two poles at DC(0 Hz) frequency , one zero at ω_z, and two non-zero poles at ω_{p1} and ω_{p2}. For this analysis, we assume that the LBW (ω_B) is placed equally four times apart from the boundary set by ω_z and ω_{p1}, respectively, as a rule of thumb.

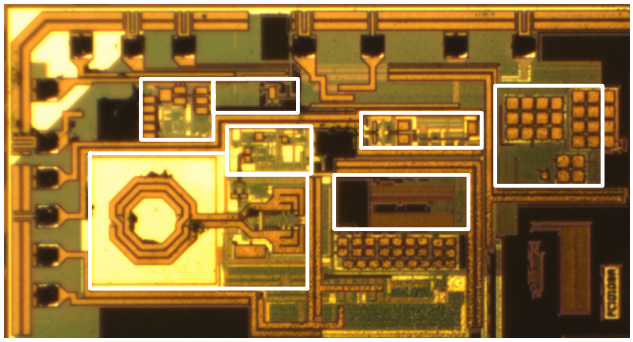


Fig. 4. Microphotograph of the fabricated chip.

In passive filters having non-scalable poles and zero, movement of ω_B in any direction degrades phase margin, because it approaches ω_z or ω_{p1}. But the scalable loop filter blocks the degradation of phase margin because ω_B is moved, accompanied by ω_z and ω_{p1}, as shown in Fig. 3(a), even though ω_{p2} is fixed in position.

To quantify the effect, Fig. 3(b) plots the variation of phase margin caused by the LBW scaling. For comparison purposes, the upper two curves represent the phase margin with a second-order filter when ω_{p2} is assumed to be infinity. As expected, the phase margin is kept constant at the scalable filter, but drops at the passive filter. Also in the third-order filter, we observe that the scalable loop filter blocks the abrupt degradation of phase margin, and even the worst phase margin is better than that of the second-order non-scalable filter.

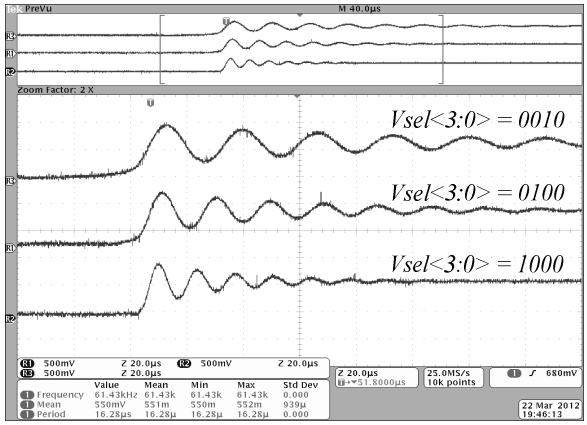
3. Measurement results

Fig. 4 shows a microphotograph of the proposed fractional-N PLL, fabricated with a TSMC 180nm complementary metal-oxide semiconductor (CMOS) process.

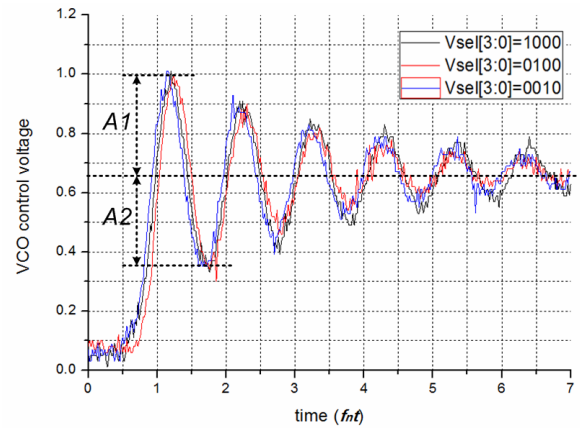
Fig. 5(a) shows the transient response monitored via V_{TUNE} with a test mode (the second-order filter) where the RC filter is bypassed and the SDM is turned off while the PLL is in transition mode under three different conditions of V_B. Voltage V_B is provided by an on-chip programmable four-level voltage divider controlled by *Vsel*[3:0], which can have the values of "1000", "0100", "0010", and "0001", measured to provide 750mV, 665mV, 582mV, and 507mV, respectively. With $V_T \approx 500$mV, therefore, the three conditions of "0010", "0100", and "1000" can provide 1x, 2x, and 3x the loop bandwidth, respectively. This variation of the LBW causes the corresponding difference in lock time in Fig. 5(a).

Phase margin (Φ_M) is difficult to measure directly, because it is an open-loop small-signal parameter. But, we can calculate it using the damping ratio (ζ) that can be measured at the transient response of the PLL, as given in Eq. (5).

$$\Phi_M = \tan^{-1}\frac{2\zeta}{\sqrt{-2\zeta^2+\sqrt{1+4\zeta^2}}} \quad (5)$$



(a)



(b)

Fig. 5. PLL acquisition with a second-order scalable filter over three different conditions of the LBW (a) Measured oscilloscope waveform, (b) Waveforms normalized with respect to natural frequency(f_n).

For this purpose, Fig. 5(b) plots the transient response using the time axis normalized with a damped natural frequency (f_n), where we can show that the three curves have the same damping ratio (ζ), thus the same phase margin when it is estimated with the first peak (A1) and the second peak (A2).

$$\zeta = \frac{\ln(A1/A2)}{\sqrt{\pi^2 + [\ln(A1/A2)]^2}} \tag{6}$$

Fig. 6 shows a plot of the single sideband phase noise from the designed frequency synthesizer, with the normal mode where the third-order filter is connected and the SDM is turned on. With the same conditions on V_B as given above, the phase noise is measured when the LBW is 1x, 2x, and 3x. In this figure, we can see that phase noise peaking is blocked within a tolerable range. The overall performance of phase noise meets the requirement for multi-band, multi-standard mobile DTV tuners when divided into the required bands.

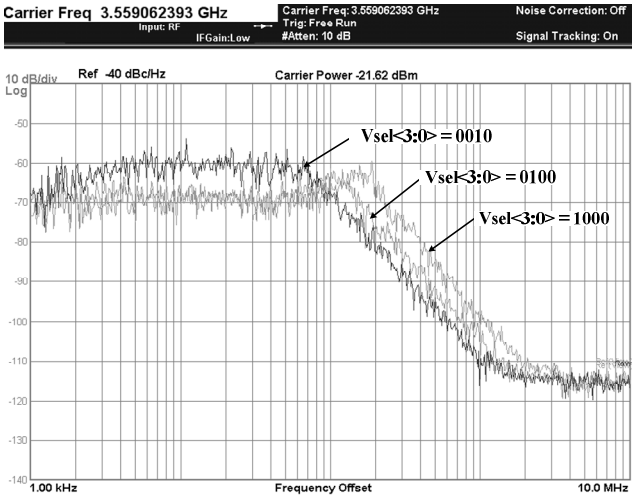


Fig. 6. Plot of SSB phase noise with the third-order scalable filter and MASH 1-1-1.

4. Conclusion

The proposed scalable filter and scalable CPC enables the design of a stability-secured LBW-controllable PLL, which prevents the degradation of phase margin and thus phase noise peaking while its loop bandwidth is tuned targeting the best IPN in each band.

The fractional-N PLL for multi-band and multi-standard mobile DTV tuners, fabricated with a TSMC 180nm CMOS process, has shown that the third-order filter, based on a second-order scalable filter, with the property of constant damping effectively rejects the SDM noise from the MASH 1-1-1, adds little noise to close-in phase noise, and prevents phase noise peaking from growing while its LBW increases by up to three times.

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