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Design of Super-junction TMOSFET with Embedded Temperature Sensor

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Abstract

Super-junction trench MOSFET (SJ TMOSFET) devices are well known for lower specific on-resistance and high breakdown voltage (BV). For a conventional power MOSFET (metal-oxide semiconductor field-effect transistor) such as trench double-diffused MOSFET (TDMOSFET), there is a tradeoff relationship between specific on-state resistance and breakdown voltage. In order to overcome the tradeoff relationship, a SJ TMOSFET structure is suggested, but sensing the temperature distribution of TMOSFET is very important in the application since heat is generated in the junction area affecting TMOSFET. In this paper, analyzing the temperature characteristics for different number bonding for SJ TMOSFET with an embedded temperature sensor is carried out after designing the diode temperature sensor at the surface of SJ TMOSFET for the class of 100 V and 100 A for a BLDC motor.

Key words: *SJ TMOSFET, Trench MOSFET, Embedded Temperature Sensor, TMOSFET, Bipolar Sensor Structure*

I. Introduction

Super-junction (SJ) MOSFET [1,2] power devices are well known for lower on-state resistance and gate charge. However, it is difficult to fabricate the exact balanced doping profile, and the impact of imbalance results in varying breakdown voltages (BV). TMOSFET is exposed to overload power dissipation during overload operating conditions, such as inductive switching events or short circuit; its junction temperature and react need to be measured. There are two types of bipolar and resistive temperature sensors in self-isolated, common drain, smart power TMOSFETs.

In this paper, the bipolar temperture sensor is used as temperature one because of its diode voltage linear temperature dependence [3,4]. ANSYS simulation is used to analyze the sensor sensitivity. The structure of SJ TMOSFET with embedded diode temperature sensor, as shown in Fig. 1, is composed of alternate P and N pillars of the same widths of W_p and W_N, respectively, based on SJ TMOSFET [1,2]. The doping profile concentration of P and N pillar in SJ TMOSFET are assumed as N_A and N_D, respectively. The relationship between P and N pillar in doping concentrations and widths is

$$N_D W_N = N_A W_P \tag{1}$$

The diode is formed at the well region. The drift

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current flows from the drain at the bottom N+ substrate to the source at the top. The doping profile required in the drift region to achieve a uniform electric field along the y-direction is determined by two dimensional charge coupling for the non-uniform SJ TMOSFET structure.

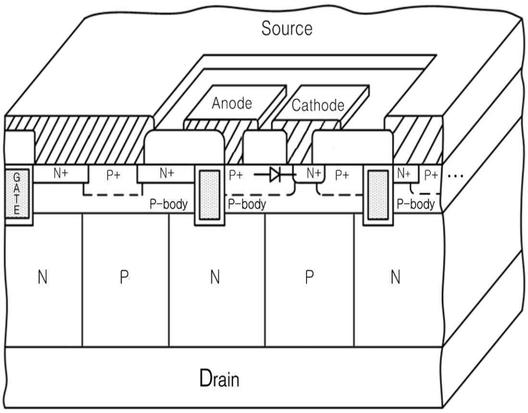


Fig. 1 Fundamental structure of SJ TMOSFET with embedded diode temperature sensor

II. Bipolar Sensor Structure

For temperature sensing, the temperature change of base-emitter voltage (V_{BE}) under constant emitter current is measured. The forward voltage is a well known electrical parameter for measuring the temperature of a semiconductor device. The relationship [3] between the current, the voltage, and the temperature of an ideal PN-junction is given by eq. (2).

$$I_{PN} = I_s\left(e^{\frac{qV_{PN}}{kT}} - 1\right) \quad (2)$$

where I_S is the saturation current of the diode, I_{PN} is the current flowing through the PN-junction, V_{PN} is the voltage across the junction, q is the electron charge, k is Boltzmann's constant and T is the temperature. The saturation current [3] is described in eq. (3).

$$I_S = I_O T^{\gamma} e^{\frac{-Eg}{kT}} \quad (3)$$

where ɣ is a constant equal to about 3, I_O is a constant, and E_g is the bandgap of Si (1.12 eV at T =275 K). From eq. (2), the voltage of V_{PN} can be represented by the function of temperature of T for a current [4] after substituting eq. (3) into eq. (2).

The bipolar transistor is formed by the emitter (N+source), base (P-body) and collector (N-epi) regions shown in Fig. 1. The base-emitter voltage [5] depends on the temperature under the biased constant current, and the change of V_{BE} under constant current can be calculated as eq. (4).

$$V_{BE}(T) = V_{BE}(T_R) + \beta_{V_{BE}}(T - T_R) \quad (4)$$

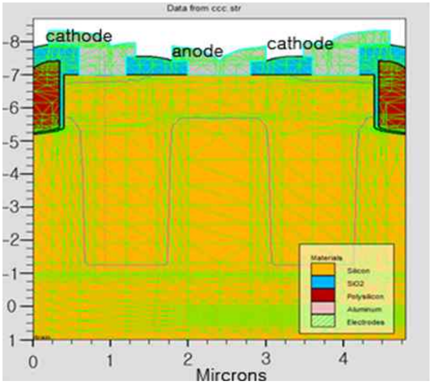
where V_{BE}(T) is the temperature dependent base-emitter voltage, T_R[K] is the reference temperature and $\beta_{V_{BE}}$ [V/K] is the temperature coefficient. The temperature coefficient of $\beta_{V_{BE}}$ is shown as -2 mV/K [5], which is also checked by Silvaco TCAD Device simulation as shown in Fig. 2 (b). The measurement temperature range is -60 ℃ to 180℃. The structure of SJ TMOSFET is composed of P and N pillars alternately. The doping concentration and pillar width are determined to make the charge distribution of the structure be balanced. The main characteristics of SJ TMOSFET with bipolar sensor are shown in Table 1.

Table 1. Main characteristics of SJ TMOSFET with bipolar transistor

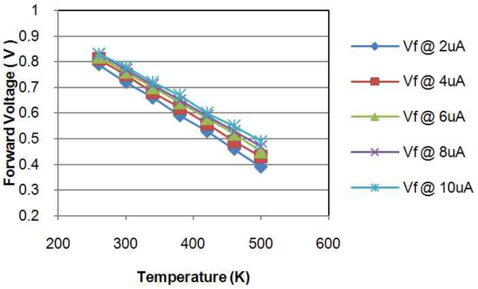
Device Parameter	Value	Device Parameter	Value
Cell pitch	2.4 μm	Trench depth	1.75 μm
N, P pillar doping concentration	$1 \times 10^{16}/\text{cm}^3$	Trench width	0.28 μm
Gate oxide thickness (t_{OX})	500 Å	N_+ source width	0.25 μm
P well depth(X_j)	1.2 μm	P_+ body contact width	1.5 μm

In the SJ TMOSFET structure designed in Fig. 2 (a), the diode sensor is implemented on the top area for measuring V_{BE}.

In this temperature range, a linear fit is applied, and the forward voltages vs. temperature (K) are obtained for five kinds of different emitter currents as shown in Fig. 2 (b). It linearly decreases as temperature increases under the biased current for 2 μA to 10 μA. The characteristics are analyzed after simulation by SILVACO TCAD Atlas [6].



(a) SJ TMOSFET structure with the implemented bipolar sensor



(b) forward voltage vs. temperature (K)

Fig. 2 Design of SJ TMOSFET and Temperature characteristics

III. Simulations and Analyses

The simulation results for the forward voltages (V_{BE}) between base and emitter are satisfied with the theoretical equation of eq. (3), showing linearly decreasing function of temperature (T_R). The equivalent resistance model for the SJ TMOSFET array shown in Fig. 3 for an example is sketched. The vertical resistance of R_{FET} is caused by the drift region in TMOSFET. R_{metal} includes the source contact resistance and the source metal one between grids and grids. R_{bonds} indicates the contact resistance caused by the bonding pad and the wire itself. As the number of arrays increases, model and temperature distribution [7,8] can be precisely achieved.

The sheet resistance of aluminum, which is used for the source metal at the top layer, is 15 mΩ for 2 μm thickness. The area of a unit chip is 1 mm^2 (1mm × 1mm), and the structure is composed of 5×5 array meshes. The drift resistance between grid points is approximately simulated as 4 mΩ when the voltage between gate and source is 10 V, and the resistance of bonding wire is 0.1mΩ. In the SJ TMOSFET equivalent circuit model [9] with the mesh resistance caused by the source metal at the top area, the drift resistance at the SJ TMOSFET and the resistance at the bonding is modeled as the array.

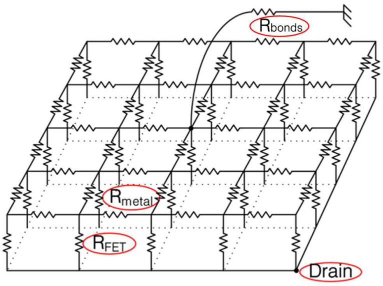


Fig. 3 The equivalent resistance model for a SJ TMOSFET 5 × 5 array meshes

For analyzing the power dissipation, the simulation was carried out by SPICE [10] and the temperature characteristics are accomplished by using ANSYS software [11]. It is shown that the power dissipation when $V_{drain} = 0.5\,V$ is concentrated at the center, showing the peak point for one, two and four bondings in Fig. 4, Fig. 5 and Fig. 6, respectively.

The power dissipation gets to be widely and uniformly distributed as the number of bonding wires increases. The change in the maximum power dissipation vs. the number of bonding wires is depicted in Fig. 7.

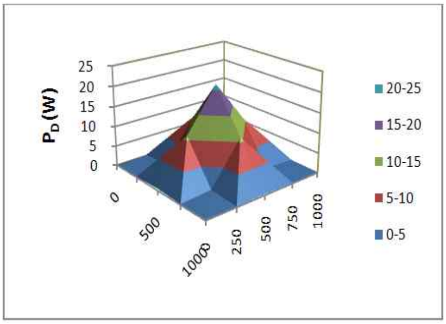


Fig. 4 Power distribution of total 29 W for One bonding 5 × 5 array meshes

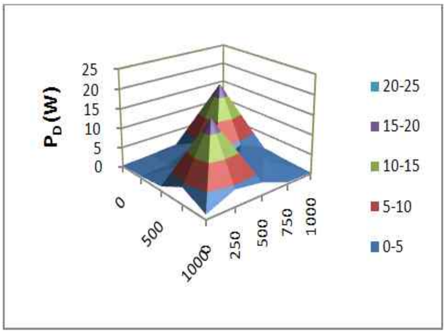


Fig. 5 Power distribution of total 47 W for Two bonding 5 × 5 array meshes

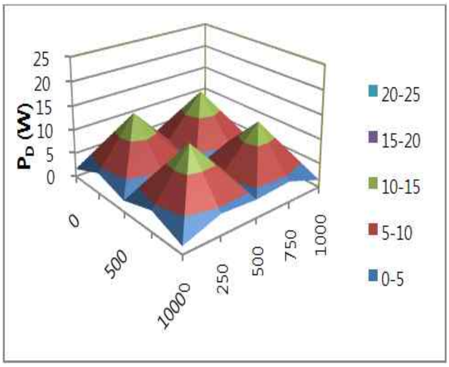


Fig. 6 Power distribution of total 129 W for Four bonding 5 × 5 array meshes

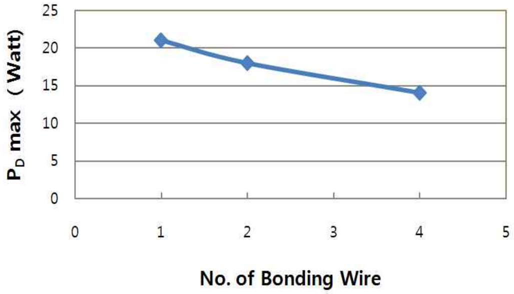


Fig. 7 The maximum power distribution vs. no. of bonding wires

In order to measure the temperature of the chip, the test circuit is shown in Fig. 8. The constant current source is connected to the cathode of the embedded diode temperature sensor shown in Fig. 1. The square wave is applied to the gate of SJ TMOSFET and the embedded diode temperature sensor is internally mounted to the source. When the constant current is flowing, the negative voltage of V_1 is made. The voltage shift circuit for adding 0.7 V of V_{BE} is added to the output terminal of the embedded diode. The voltage vs. time, which can be converted to the corresponding transient variation of temperature, is measured. The self-heating is produced when SJ TMOSFET is operated, and it is possible to check the sensing temperature of SJ TMOSFET by using the test circuit in Fig. 8. Here, an arbitrary constant current is applied to the input to measure the variance of voltage.

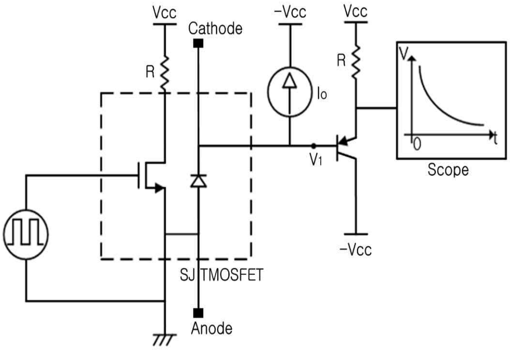


Fig. 8 A temperature application circuit

Ⅳ. Conclusions

The structure of SJ TMOSFET with an embedded temperature sensor was completely designed and the simulation for analyzing the diode temperature characteristics were also throughly examined. It is found that the forward voltage linearly decreases as the temperature increases. To achieve uniformly distributed power dissipation, the distributed wire bonding with multiple wires should be used to accommodate heat at the bonding point where the current is concentrated. The SJ TMOSFET should be designed, making the temperature be dispersed and the power be widely distributed. The appropriate number of bonding and the size of the package are determined for thermal allowable temperature, considering the manufacturing cost.

When assembling the power device, the number and the position of bonding wires for packaging the SJ TMOSFET with low resistance should be carefully considered.

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