JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.3, JUNE, 2015
http://dx.doi.org/10.5573/JSTS.2015.15.3.417
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A 6.5 – 8.5 GHz CMOS UWB Transmitter Using Switched LC VCO

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***Abstract*—A 6.5 – 8.5 GHz CMOS UWB transmitter is implemented using 0.18 μm CMOS technology. The transmitter is mainly composed of switched LC VCO and digital pulse generator (DPG). Using RF switch and DPG, the uniform power and sidelobe rejection are achieved irrespective of the carrier frequency. The measured UWB carrier frequency range is 7 ~ 8 GHz and the pulse width is tunable from 1 to 2 ns. The measured energy efficiency per pulse is 2.1 % and the power consumption is 0.6 mW at 10 Mbps without the buffer amplifier. The chip core size is 0.72 mm^2.**

***Index Terms*—CMOS IC, impulse generator, UWB transmitter, low power, switched LC VCO**

I. INTRODUCTION

Because the Impulse Radio (IR) – Ultra Wide Band (UWB) system has the advantages of high resolution and coexistence with the other communication signals, it would be a strong candidate for the radar sensors and location based systems (LBS). The allowed frequency band includes two subbands of 3 ~ 5 GHz and 6 ~ 10 GHz, and the maximum available power spectral density is under -41.3 dBm/MHz in average, which is known as equivalent isotropically radiated power (EIRP) restriction. Moreover, the transmitted power spectrum must meet the required spectrum mask given from FCC regulation. Furthermore, in multiband UWB RF system, the carrier frequency of UWB impulse should be changed to avoid the collisions among the users in different bands. As for the transmitter of IR-UWB transceiver, many literatures about the digitally synthesized topology and the switched VCO type have been recently reported [1-6]. The carrier-free digitally synthesized transmitter has some drawbacks such as the undesired digital noise and much more sidelobe due to the waveform shape while it has the merits of inductorless small chip area and low power consumption. On the other hand, the switched VCO type transmitter gives the stable oscillation in actual design and the accurate frequency trimming is possible with the varactor control.

One of the design issues of the VCO based UWB transmitter is the different start-up time for the widely variable carrier frequency [6]. The different start-up time produces the different amplitude of the UWB impulse for each channel. In this work, using the switched window of the settled VCO output, the equal amplitudes are provided in cost of a little more current consumption. On the other hand, the sidelobe of UWB impulse signal is also important issue of UWB transmitter. Although there are some low sidelobe UWB transmitters such as Gaussian-shaping transmitters, a simple pulse shaping technique is employed, which uses a RF switch with the finite switching time. The achieved side band rejection is sufficient to be compliant with the desired spectrum mask. The proposed 6.5 – 8.5 GHz IR-UWB transmitter with the uniform impulse amplitude and low sidelobe is fabricated in 0.18 μm CMOS technology.

Manuscript received Mar. 10, 2015; accepted May. 25, 2015
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II. TRANSMITTER ARCHITECTURE AND TIMING PULSE GENERATION

Fig. 1 illustrates the overall architecture of the designed IR-UWB transmitter. It consists of two digital control pulse generator (DPG1 and DPG2), the current controlled LC VCO, and the RF buffer amplifier connected to the off-chip filter and antenna.

In the transmitter, the digital data signal from the baseband modem enters both the DPG1 and DPG2, and it makes the repetitive short pulses for switching the current source of LC VCO and RF switch. And the VCO output is shaped by the RF switch, which is turned on/off by the tunable and shaped pulse from the DPG2. The timing diagram and control signals shown in Fig. 2 explicitly explain how the transmitter is working. From the data input, DPG1 provides the control voltage, which is injected to the control gate of VCO current source switch and determines the VCO turn-on time. It is also digitally tunable via integrated SPI controller. The pulse duration of DPG1 output can be varied from 2 up to 10 ns. The control pulse from DPG1 turns on the LC VCO, and then the oscillation starts, and finally, VCO becomes stable after the settling time depending upon the carrier frequency. Next, the VCO output signal can be selected within the time-window determined by the RF switch turn-on time.

The output pulse from DPG2 is used as the gate control voltage of RF switch as shown in Fig. 1. The control pulse of DPG2 begins when the VCO output arrives at the full-amplitude swing for all frequency bands. Hence, the impulse selected within the time-window defined by DPG2 pulse has the uniform and equal amplitude at all frequency bands. Moreover, the gate control voltage for RF switch is generated with some RC time delay of DPG2 pulse. So the gate voltage of RF switch has the finite rise time and fall time shown in the fifth row of Fig. 2. Consequently, the envelope of UWB impulse signal at the RF switch output is shaped like a triangle, which reduces the undesired sidelobe enough to meet the spectrum emission requirement.

III. UWB TRANSMITTER CIRCUIT DESIGN

The switched LC VCO and RF switch need the very short and tunable control pulses generated by two DPGs. The control pulse of DPG1 has the duration time which includes the VCO set-up time and the needed impulse width with some margin. Actually, since the simulated set-up time is few nano seconds and the target impulse width is 0.5 ~ 2 ns, the tunable range of DPG1 output is determined to be from 2 to 6 ns. And time-duration of DPG2 output corresponds to the UWB impulse width or bandwidth, which is 0.5 ~ 2 ns. Hence, the DPG should make the short control pulse, whose time duration is adaptively trimmable. The short duration pulse can be generated by some combination of the basic digital logic and the reference time delayed inverter blocks.

Fig. 3 demonstrates the circuit schematic of the digital pulse generator both for DPG1 and DPG2. The data

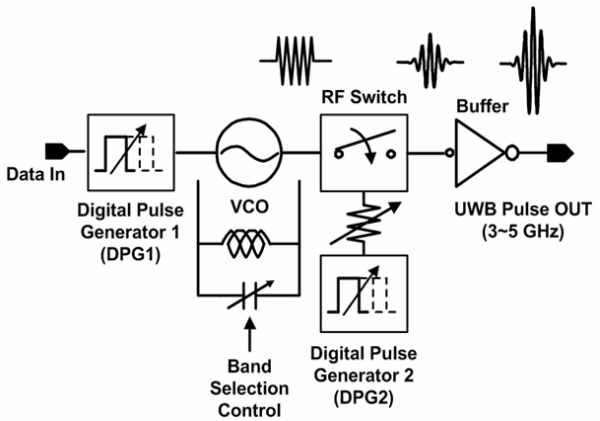

Fig. 1. Architecture of proposed UWB transmitter.

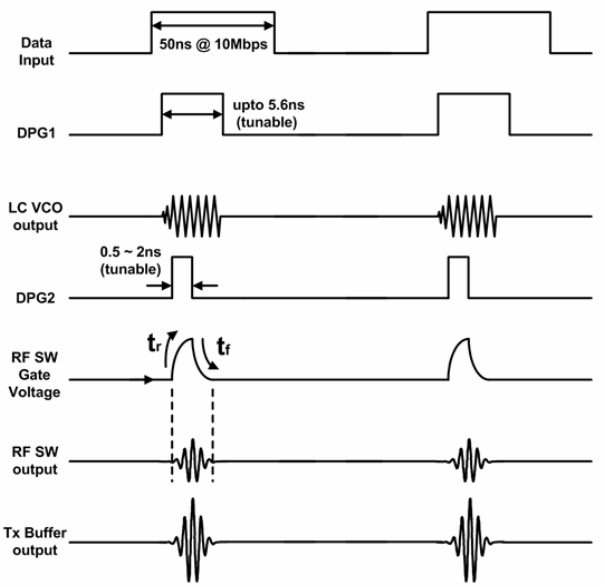

Fig. 2. Block diagram of the proposed transmitter.

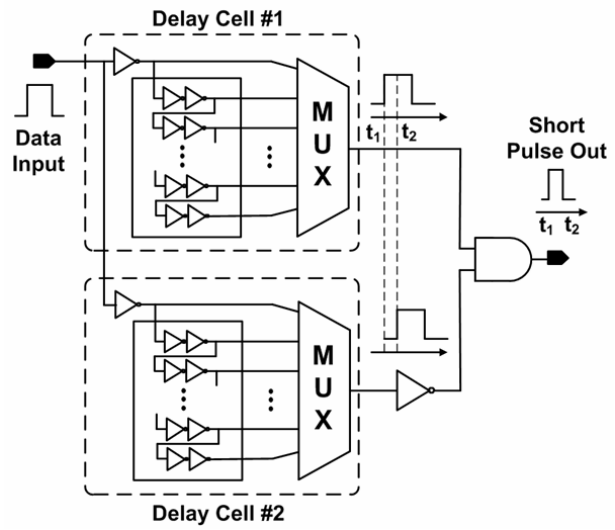

Fig. 3. Schematic of digital pulse generators.

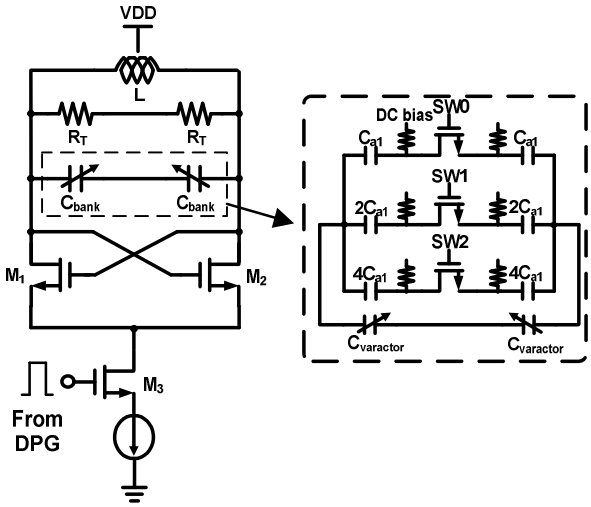

Fig. 4. LC VCO schematic with switched capacitor bank.

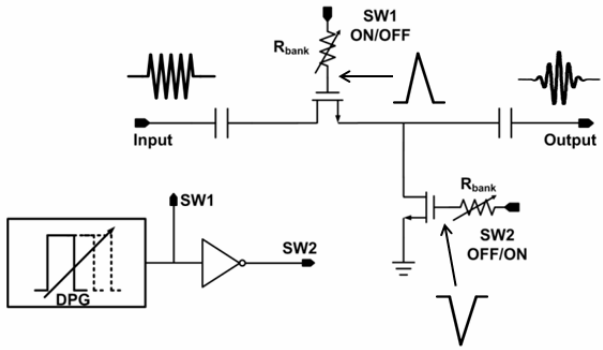

Fig. 5. Schematic of RF switch and gate control circuit.

pulse is passing through the delay line composed of 7 unit delay cells. Each unit delay cell consists of 2 inverters and produces the unit time delay, which is 3-bit digitally trimmable by adjusting the current source of the inverter cell. As shown in Fig. 3, from the cascaded inverter chain, 8 different-delay digital pulses are generated and one of them is selected by 3-bit MUX. The resultant values of time delay t_1 and t_2 as shown in Fig. 3 are to be 0, Δt_d, $2\Delta t_d$, ... , or $7\Delta t_d$, where Δt_d is the tunable time delay of the unit delay cell. The outputs of two delay cells are used as the inputs of AND gate for the digital pulse generation. Since the DPG output pulse has the duration of $t_2 - t_1 = k\Delta t_d$ (k = 0, 1, 2, …, 7) and Δt_d is tunable from 0.15 to 0.8 ns by controlling the current source of the unit delay inverter, the pulse width of the DPG can be tuned from 0.15 to 5.6 ns. Since DPG2 is used for RF switch and determines the UWB pulse width or bandwidth, it needs the time duration range of 0.5 ~ 2 ns, which can be easily obtained by our DPG circuit.

Concerning with the VCO core, a differential LC VCO topology with digitally trimmed capacitor bank is employed as illustrated in Fig. 4. The resonance frequency of LC tank determines the UWB carrier frequency, which ranges over 6.5 – 8.5 GHz. The DPG1 output is used as the control voltage for the VCO current switching. Since the switching pulse signal is injected into the NMOS switch, not into the current source itself, the set-up time, which depends on the gate capacitance of MOS switch size, and the VCO current are independently optimized. In the literature [6], the start-up transient of the oscillator output $V_0(t)$ is derived as follows.

$$V_0(t) = f\left[V_i(t)\right] + A_1 e^{-\frac{\omega_0}{2Q}(1-g_m R_T)t} \cos\left(\omega_0' t\right) \quad (1)$$

Since the equation indicates that the VCO output magnitude depends on the carrier frequency and settling time is shorter at higher carrier frequency, UWB impulse has the different magnitude at a time in the transient region for the different center frequency. To avoid these problems, the DPG2 pulse is turned on after the VCO output sufficiently settles down and tunable, while the additional turn-on time of VCO needs the slightly more power consumption. Concerning with the sidelobe rejection, as shown in Fig. 2, the gate voltage of RF switch has some slope at the rise and fall transitions using the resistor R_S, which is connected in series to the switch MOS gate as shown in Fig. 5. This provides the finite rise and fall time (0.25 ~ 1 ns) of gate control pulse

determined by RC time constant. The C is the RF switch gate capacitance C_{gs} and the resistor R_S is digitally variable. The finite rise and fall time of gate control pulse result in the impulse envelope like the triangular form and reduce the sidelobe consequently. The RF switch consists of series – shunt configuration to enhance the isolation and suppress the undesired pulse following the main impulse. The final buffer amplifier should isolate the VCO resonator core from the low 50 ohm output load and also drive it. The inverter-like push-pull CMOS amplifier is employed due to its convenient power matching over the 6.5 – 8.5 GHz wideband. The bias voltages for PMOS and NMOS are separately provided using the current mirror sources.

III. Measurement Results

A 6.5 – 8.5 GHz switched LC VCO based UWB transmitter is implemented in 0.18 ㎛ CMOS technology and measured. The used modulation is on-off keying (OOK) with 10 Mb/s RZ data. Fig. 6 and 7 show the measured UWB impulse spectrum and waveform at the buffer output, which is measured using power spectrum analyzer (Agilent E4440A) and high speed oscilloscope (R&S®RTO 1044). The measured pulse duration is trimmable from 1 to 2 ns. And the peak voltage amplitude is 250 mV. Fig. 6 presents the measured output power spectrums of the UWB transmitter for three sub-bands, which have the equal power and are also compliant with FCC mask in the range of 6.5 – 8.5 GHz at 10 Mbps data input. The undesired spurious signals around 1 GHz is expected to be easily eliminated with the simple off-chip LC filter. The center frequency is changed from 7 GHz to 8 GHz by trimming the digital capacitor arrays and varactor.

The sidelobe signal rejection is 5 dB improved comparing with the UWB spectrum signal without the impulse-shaping function using RF switch. Table 1 presents the summary of the recently published reports with respect to the power consumption, efficiency, and chip size. The efficiency η is calculated according to the reference [6]. At a data rate of 10 Mbps, the transmitter consumes 0.6 mW from 1.8 V supply in average. The measured energy efficiency per pulse η is 2.1 %

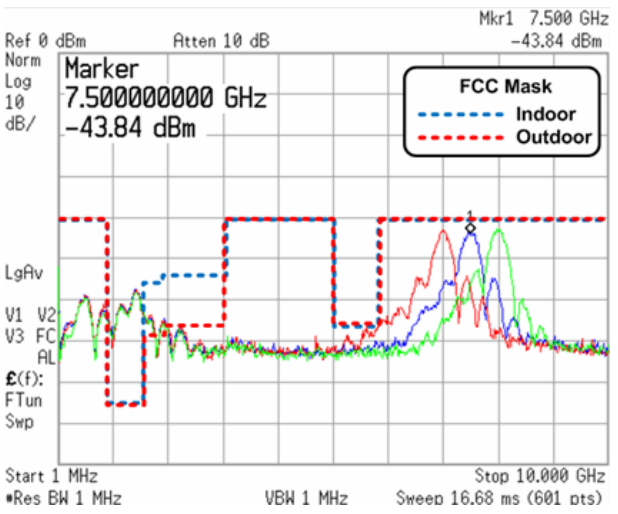

Fig. 6. Measured power spectrum of UWB transmitter.

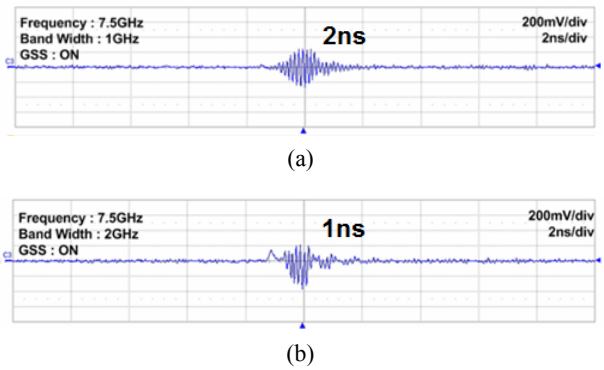

Fig. 7. Measured time-domain UWB waveform (a) 2 ns pulse width, (b) 1 ns pulse width.

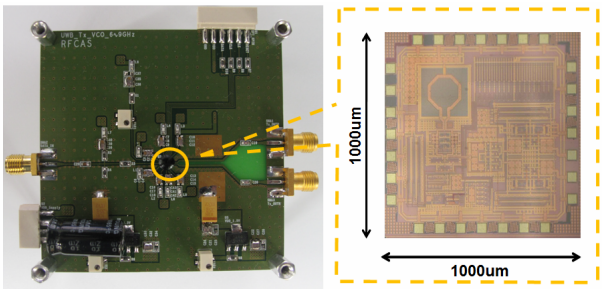

Fig. 8. Photograph of fabricated die and test board Chip layout.

Table 1. Comparison of UWB transmitter performance

Ref.	Technology	η (/pulse)	Power cons. @data rate (W/bps)	Area (mm^2)
[1]. 2007	CMOS 90nm	5.745 %	0.452mW @10M	0.08
[2]. 2007	CMOS 0.18μm	0.22 %	29.7mW @36M	0.4
[3]. 2006	CMOS 0.13μm	0.67 %	10mW @160M	1.56
[4]. 2011	CMOS 0.18μm	0.89%	2.84mW@100M	0.25
[5]. 2007	CMOS 0.18μm	1.575 %	1.823mW @100M	0.394
[6]. 2009	CMOS 0.18μm	25.4%	0.236mW @2M	0.188
This Work	CMOS 0.18μm	2.1 %	0.6mW @10M	0.72

including the power consumption of buffer amplifier. The core size of the implemented CMOS transmitter chip is 0.72 mm^2.

V. CONCLUSIONS

In this work, a switched VCO type IR-UWB impulse generator is implemented in 0.18 ㎛ CMOS technology. The carrier frequency range of the transmitter is 7 ~ 8 GHz. The RF switch and proposed DPG enable us to achieve the tunable pulse width and suppress the undesired sidelobe. The measured results show that the energy efficiency per pulse is 2.1 % and the spectrum for each sub-band meets the regulated spectrum mask.

ACKNOWLEDGMENTS

This work was conducted during the sabbatical year of Kwangwoon University in 2012 and also supported by ICT R&D Program of MSIP/IITP [14-911-01-001, Development of Quasi-Millimeter-Wave Channel-Adaptive Antennas and Transceivers].

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