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SOC Test Compression Scheme Sharing Free Variables in Embedded Deterministic Test Environment

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Abstract—**This paper presents a new SOC test compression scheme in Embedded Deterministic Test (EDT) compression environment. Compressed test data is brought over the TAM from the tester to the cores in SOC and decompressed in the cores. The proposed scheme allows cores tested at the same time to share some test channels. By sharing free variables in these channels across test cubes of different cores decompressed at the same time, high encoding efficiency is achieved. Moreover, no excess control data is required in this scheme. The ability to reuse excess free variables eliminates the need for high precision in matching the number of test channels with the number of care bits for every core. Experimental results obtained for some SOC designs illustrate effectiveness of the proposed test application scheme.**

Index Terms—**SOC testing, test data compression, linear decompression, parallel test, tester channel**

I. INTRODUCTION

System-on-a-chip (SOC) is designed based on reusable intellectual property (IP) cores. SOCs can reduce manufacture cost and offer rapid system implementation. However, the testing for SOC has become a significant and serious challenge. To simplify complexity of test access and application the modular test of the IP cores in an SOC is utilized frequently [1]. In modular test, core test wrapper isolates an embedded core from its environment, and test access mechanism (TAM) which facilitates modular testing is developed to transport test data from the SOC pins to core terminals. For IP cores, it may be infeasible to perform ATPG (Automatic Test Pattern Generation). Thus a set of test cubes provided by core manufacturer must be applied during test. Test cubes is defined as test vectors in which the unassigned inputs are left as don't cares (also called X bits).

SOC test techniques requires specialized hardware infrastructure such as TAM and test wrappers [3, 4]. A lot of schemes tailoring both TAMs and test wrappers have been proposed towards optimal test application time [5, 21], test interface architecture [6], power consumption [7, 8], control logic [9], routing and layout optimization or embedded cores hierarchy [10].

Test data volumes are growing especially for delay test [18] as the VLSI complexity increases. Recently, there is a growing interest in test data compression of SOC testing [12, 22]. On-chip test compression is one of the mainstream DFT methodologies [2]. ATE (Automatic Test Equipment) delivers test data in a compressed form, and on-chip decompressors expand them into the actual test patterns which will be transported into scan chains. Early SOC test compression techniques mostly utilize coding such as nine code words [13], frequency-directed run-length (FDR) codes [14], and XOR networks [15]. In recent years, SOC test compression schemes based on linear decompression which can provide higher compression ratios continue to appear. In [16], test cubes for each core are encoded separately using LFSR reseeding. Seed variables are then delivered from ATE channels by time-multiplexed way to successive cores. The expenses including control data, hardware logic

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needed in the scheme may adversely prohibit its application. The scheme of [17] utilizes a single linear decompressor to expand the tester channels to numerous TAM lines. However, performing decompression outside cores poses larger TAM bandwidth requirement for transporting uncompressed data.

The techniques based on Embedded Deterministic Test described in [19, 20] employ dynamic channel allocation to manage tester channel bandwidth. They allow multiple cores to be tested simultaneously and allocate tester channels dynamically to decompressors as needed. In these approaches, for the application of each test cube test scheduling is needed to determine mapping relationship between tester channels and decompressors. These approaches need corresponding control data on a per test cube basis and additional logic.

The proposed SOC test compression approach aims to improve encoding efficiency of linear decompressors. Encoding efficiency is defined as the ratio of the number of care bits in the test cubes to the number of free variables (i.e., the number of compressed bits stored on the tester). The main idea is that the cores tested simultaneously share part of free variables. Non-pivot free variables for one test cube of a core can be reused to encode test cubes of other cores with negligible impact on the computational complexity in solving the linear equations. This scheme avoids wasting excess free variables and improves the compression ratio of SOC testing. Consequently, it can help with controlling the SOC test cost.

II. BACKGROUND AND MOTIVATION

Conventional SOC test bus architecture with fixed-width is shown in Fig. 1. In the architecture the total TAM width is partitioned among several test buses with fixed-width [11]. Cores using the same TAM lines are tested sequentially unless their test patterns are compatible, while those using the different TAM lines can be tested in parallel. Compressed test data is delivered from tester via TAM to linear decompressor in the cores. Then the test patterns decompressed by linear decompressor are shifted into scan chains in cores.

In the test compression based on sequential linear decompressors, the number of free variables is dependent on the number of care bits in a test cube. When encoding

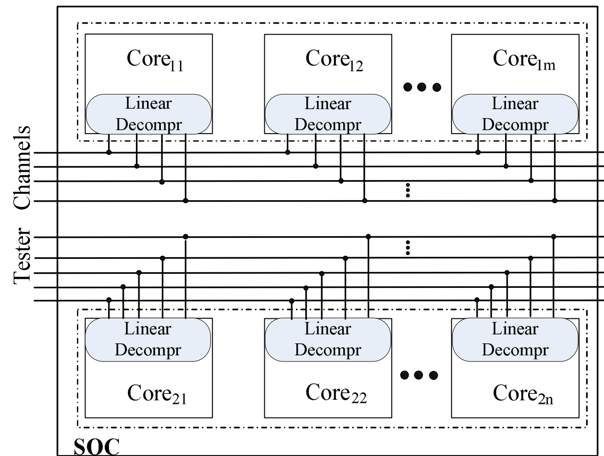

Fig. 1. Conventional SOC test bus architecture.

a test cube, using too few free variables may result in the unsolvability of the linear equations. In test cubes generated by ATPG with dynamic compaction, the rates of care bits range from 5% to 1% only at the beginning of the ATPG process. After a small quantity of test patterns the fill rate may fell below 1%. It can be seen that the fill rates in each test cube varies significantly for a core. To guarantee the compressibility of each test cubes for a single core, the number of free variables of the linear decompressor should be set according to the largest number of care bits in a test cube. In EDT, the free variables are delivered via tester Channel. Thus, tester channels can be in their full capacity to transport necessary test data for a couple of initial test cubes; however, encoding the remaining test cubes may not require so many inputs. In [18], the authors illustrate industrial test cube profiles as shown in Fig. 2. As can be seen from the figure, the fill rate for 8000 initial test patterns varies from 1.1% to 0.02%. Practical ATE channel requirements to encode each test cube are also shown in the same figure. The number of ATE channels is determined on the premise that all test patterns are compressible. Due to using enough test channels to guarantee the compressibility of each test cubes, the compression ratio will be very low in conventional SOC test compression based on sequential linear decompressors.

So our goal is to reuse non-pivot free variables when encoding a test cube with few specified bits.

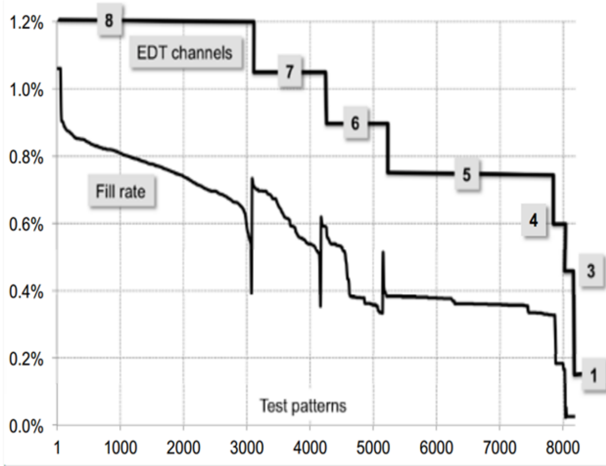

Fig. 2. Test cube specified rate profile and ATE channel requirements.

III. Proposed SOC Compression Test Scheme

1. Proposed SOC test architecture

The proposed SOC test scheme sharing free variables in common tester channels (denoted by bold lines) is illustrated in Fig. 2. As shown in the figure, the cores using the exact same TAM lines are divided into a group. Cores in the same group are tested sequentially unless their test patterns are compatible. Those using not identical TAM lines (in the different groups) can be tested in parallel. Compressed test data is delivered from tester via TAM and decompressed in the cores by linear decompressor. Then the decompressed test patterns are scanned into scan chains in cores. During test, if two cores in the different groups have some common TAM lines (tester channels), the free variables delivered by the common TAM lines can be shared by these cores. When decompressing a test cube for a core in group one/two, if there exist more free variables transported in the common TAM than necessary, then test cubes for other cores in group two/one can be decompressed using these variables.

For a linear decompressor, the relationship between free variables (*X*) and output state vector (*Y*) can be represented by a system of linear equations $MX = Y$, where M is the characteristic matrix for the linear decompressor. Encoding test cubes in test compression based on a linear decompressor requires the solution of a system of linear equations (one equation for each

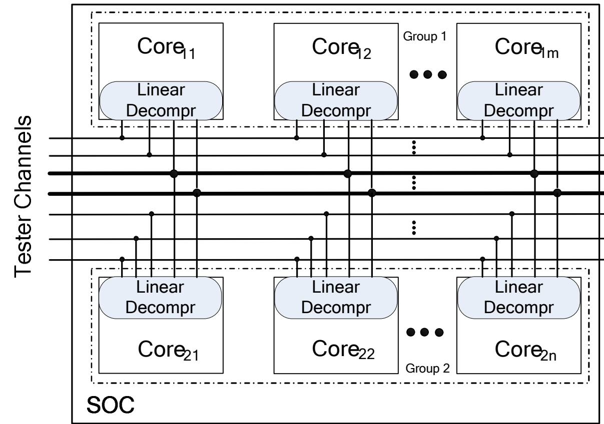

Fig. 3. Proposed SOC test architecture.

specified bit).

Next, we explain the proposed SOC test scheme by an example. Fig. 3 illustrates a linear decompressor with four-bit state and two external inputs. The phase shifter is ignored for simplicity. The free variables for the linear decompressor are represented by (X1 X2 . . . X10). The test cube is represented by (Y1 Y2 . . . Y12). The following system of linear equations describes this configuration.

$$\begin{bmatrix} 0110100000 \\ 0010100000 \\ 0001000000 \\ 1000000100 \\ 0011110000 \\ 0001010000 \\ 1000000100 \\ 0110100010 \\ 1001011100 \\ 1000001100 \\ 0110100010 \\ 0011110001 \end{bmatrix} \times \begin{bmatrix} X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \\ X7 \\ X8 \\ X9 \\ X10 \end{bmatrix} = \begin{bmatrix} Y1 \\ Y2 \\ Y3 \\ Y4 \\ Y5 \\ Y6 \\ Y7 \\ Y8 \\ Y9 \\ Y10 \\ Y11 \\ Y12 \end{bmatrix} \quad (1)$$

Assume that a test cube is T1 (01001XXX1XX0). Encoding the test cube involves solving the following system of linear Eq. (2).

$$\begin{bmatrix} 0110100000 \\ 0010100000 \\ 0001000000 \\ 1000000100 \\ 0011110000 \\ 1001011100 \\ 0011110001 \end{bmatrix} \times \begin{bmatrix} X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \\ X7 \\ X8 \\ X9 \\ X10 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \end{bmatrix} \quad (2)$$

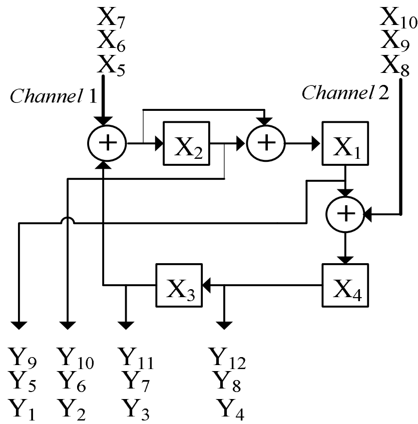

Fig. 4. An example of linear decompressor.

T1 has 7 care bits, thus the formula (2) contain 7 linear equations. According to linear algebra theorem, the system of linear equations can be solved by using Gauss-Jordan elimination method to obtain a set of pivots (one per specified bit). The following system of linear equations is achieved by implementing Gauss-Jordan elimination on formula (2).

$$\begin{bmatrix} 1000000100 \\ 0100000000 \\ 0010100000 \\ 0001000000 \\ 0000010000 \\ 0000001000 \\ 0000000001 \end{bmatrix} \times \begin{bmatrix} X1 \\ X2 \\ X3 \\ X4 \\ X5 \\ X6 \\ X7 \\ X8 \\ X9 \\ X10 \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \end{bmatrix} \quad (3)$$

The free-variables except for pivots are called non-pivots which can be assigned any value without impact on solving the system of linear equations. After assigning random values to the non-pivots, appropriate values for the pivots can always be obtained to solve the system of linear equations. As can be seen from formula (3), X1, X2, X3, X4, X6, X7 and X10 are pivots, while X5, X8, X10 are non-pivots. For encoding the test cube T1, these non-pivots are helpless. That is, these free variables are wasted only if reuse technology is introduced. If test channel 1 is shared by other core, the two free variables X8 and X9 can be reused as pivots to encode a test cube for this core. This is the key idea of this paper.

2. The test flow of the proposed SOC test scheme

To guarantee that test cubes for two cores tested simultaneously can be encoded successfully, the use for free variables in common test channels must be limited. These test cubes should be chosen under the constraint that there exist enough free variables to solve successfully the system of linear equations corresponding to all specified bits. The specified rate of test cubes for a core varies considerably, so the requirements to test channels are obviously different. Assume that core-1 and core-2 are tested simultaneously in the SOC test. When a test cube with large number of specified bits for core-1 (core-2) is applied, encoding a test cube with fewer specified bits for core-2 (core-1) will contribute to achieve the sharing and optimized distribution of test channels. The detailed test flow is depicted as shown in Fig. 4.

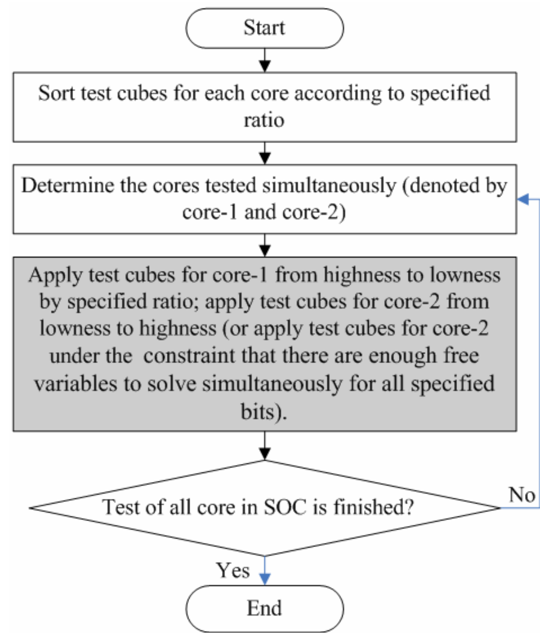

Fig. 5. The test flow of the proposed SOC test scheme.

3. Determination of the number of common channels

The number of common channels concerns the compression efficiency in the proposed SOC test scheme. If the proportion of common channels for the core is too high, maybe no test cube of the core can be encoded successfully when other core are tested with test cubes containing many specified bits. Conversely, low proportion of common channels for the cores tested simultaneously may reduce compression efficiency in the SOC test scheme. It is necessary to determine the number of common channels reasonably.

For a certain core, let k_{max} be the largest number of channels required in encoding test cubes with most specified bits, and k_{min} be the smallest number of channels required in encoding test cubes with fewest specified bits. Let l be the number of common channels. To guarantee that the cores can be tested simultaneously, l should satisfy:

$$0 < l \leqslant k_{max} - k_{min} \tag{4}$$

To maximize the SOC test compression gains, the larger l should be considered on the premise of satisfying the smooth progress of cores parallel testing.

IV. EXPERIMENTAL RESULTS

To verify the efficiency of the proposed SOC test scheme, experiments are performed on five large SOC designs. The targeted fault model is stuck-at fault. The basic characteristics regarding the designs are summarized in Table 1. These characteristics include (isolated) cores count, the number of (total) gate, the number of scan cells, the number of test patterns (for all the cores), the total bit count in test data, as well as fill ratio in all tests.

Table 2 shows the simulation results for conventional SOC test scheme introduced in section 2 and the proposed SOC test scheme. In these experiments 100 scan chains are configured uniformly for each core. Only the situation is considered that two groups of cores share the common tester channels. Ring generator is used as linear decompressor. Three fault simulation runs are also carried out for each circuit. For the proposed scheme, two test cases are reported.

Case 1: For each core, the number of common channels l should satisfy: $0 < l \leqslant \lceil (k_{max} - k_{min})/2 \rfloor$. Meanwhile, it is guaranteed that the cores sharing common channels can be always tested simultaneously. k_{max} denotes the largest number of channels required in encoding test cubes with most specified bits, and k_{min} denotes the smallest number of channels required in encoding test cubes with fewest specified bits.

Table 1. SOC Characteristics

Charact. \ SOC	A1	A2	A3	A4	A5
Cores	10	12	18	30	40
Gates	0.30M	1.21M	4.79M	5.48M	7.38M
Scan cells	65.6K	187.7K	199.7K	437.4K	446.2K
No. test	3125	5112	8964	15315	16540
Test data	20.4M	80.5M	102.6M	237.4M	179.8M
Fill ratio	4.03%	4.93%	4.90%	4.21%	5.12%

Case 2: For each core, the number of common channels l should satisfy: $0 < l \leqslant k_{max} - k_{min}$. Meanwhile, it is guaranteed that the cores sharing common channels can be always tested simultaneously.

In Table 2, columns 2-3 designate test data volume stored in tester and the compression ratio for conventional SOC test scheme respectively. Columns 4-5 present test data volume stored in tester and the compression ratio for proposed SOC test scheme with case 1, respectively. The sixth column show the reduction percentage of tester data compared with conventional SOC test scheme. The following three columns give the similar simulation results for the proposed SOC test scheme with case 2. The last row illustrates the average results of the five SOC designs. The compression ratio is calculated by the formula (5):

$$compression\ ratio = 1 - \frac{bits\ stored\ in\ tester}{total\ bits\ in\ original\ test\ set} \tag{5}$$

Table 2. Simulation results for the proposed SOC test scheme

SOC	Conventional SOC test scheme		Proposed scheme with $l \leq \lceil (k_{max} - k_{min})/2 \rfloor$			Proposed scheme with $l \leq k_{max} - k_{min}$		
	Tester Data	Compression Ratio%	Tester Data	Compression Ratio%	%Percent Reduction	Tester Data	Compression Ratio%	%Percent Reduction
A1	1349210	93.39	1012987	95.04	24.92	788839	96.14	41.53
A2	5094000	93.67	3856052	95.21	24.30	2988540	96.29	41.33
A3	6926985	93.25	5384962	94.75	22.26	4356947	95.75	37.10
A4	15043140	93.66	11285038	95.25	24.98	8780030	96.30	41.63
A5	12678283	92.95	9752525	94.58	23.08	7395665	95.89	38.46
Average	-	93.38	-	94.97	23.91	-	96.07	40.01

As shown in the Table 2, the compression ratio of conventional SOC test scheme for these five SOC designs is around 93.38%. The proposed SOC test approach raises the compression ratio significantly. From the last two parts of Table 2, we can see that, the improvement of test compression ratio increases as the percentage of common channels increases. Comparing with the results of conventional SOC test scheme, Tester Data volumes for the proposed scheme with case 1 and case 2 are cut down by 23.91 and 40.01 percentage points on average, respectively.

The proposed SOC test scheme reduces test data volumes by reasonable scheduling of test cubes for tested cores based on the analysis and precomputing of test sets. It does not impose extra requirement on the hardware overhead. Instead, the shared test channels can bring down the complexity of TAM to a certain extent. Besides, the control information is also not needed in the proposed approach.

V. CONCLUSIONS

The aggressive shrinking of characteristic size and rapid increase of the integrated degree in the electronics industry will bring forward higher requirement on SOC design and test procedures. By sharing free variables between cores tested simultaneously in SOC, the proposed SOC test technique provides greater flexibility in test compression. It does not have detrimental effects on an additional area and potential performance overhead. Experimental results on several larger SOC designs demonstrate the efficiency of the proposed technique. The proposed scheme can also be expanded by sharing common channels among three or more core groups to obtain better results. Meanwhile, the proposed approach can be combined with other approaches, such as test scheduling, to reach higher efficiency.

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REFERENCES

[1] Marinissen, E.J.: ‘The role of test protocols in automated test generation for embedded-core-based system ICs’, *J. Electron. Test., Theory Appl.*, vol.18, no.4, pp. 435–454, 2002.

[2] J. Rajski, J. Tyszer, M. Kassab, and N. Mukherjee, “Embedded deterministic test,” *IEEE Trans. CAD*, vol. 23, no.5, pp. 776-792, 2004.

[3] V. Iyengar, K. Chakrabarty, and E. J. Marinissen, “Test wrapper and test access mechanism co-optimization for system-on-chip,” *J. Electron. Test., Theory Appl.*, vol.18, no.2, pp. 213-230, 2002.

[4] G. Giles, J. Wang, A. Sehgal, K. J. Balakrishnan, and J. Wingfield, “Test access mechanism for multiple identical cores,” *Proc ITC*, paper 2.3, 2008.

[5] M. Agrawal, K. Chakrabarty, “Test-time optimization in NOC-based manycore SOCs using multicast routing,” *Proc. of IEEE VLSI Test Symposium*, pp.276-281, 2014.

[6] T. Han, I. Choi, H. Oh, and S. Kang, “A Scalable and Parallel Test Access Strategy for NoC-Based Multicore System,” *Proc. of Asian Test Symposium*, pp.81-86, 2014

[7] C. Yao, K.K.Saluja, P. Ramanathan, “Power and Thermal Constrained Test Scheduling Under Deep Submicron Technologies,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 30, no. 2 , pp. 317- 322, 2011.

[8] R. Michael and C. Krishnendu, “Optimization of Test Pin-Count, Test Scheduling, and Test Access for NoC-Based Multicore SoCs,” *IEEE Trans. on Computers*, vol. 63, no.3, pp. 691-702, 2014.

[9] Q. Xu and N. Nicolici, “Time/area tradeoffs in testing hierarchical SOCs with hard mega-cores,” *Proc. ITC*, pp. 1196-1202, 2004.

[10] S. K. Goel, E. J. Marinissen, A. Sehgal, and K. Chakrabarty “Testing of SoCs with hierarchical cores: common fallacies, test access optimization, and test scheduling,” *IEEE Trans. Comput.*, vol. 58, no.3, pp. 409-423, 2009.

[11] Q. Xu and N. Nicolici, “Resource-Constrained System-on a-Chip Test: A Survey”, *IEE Proc. Computers & Digital Techniques*, vol. 152, no. 1, pp. 67-81, 2005.

[12] Z. Wang, K. Chakrabarty, and S. Wang,

"Integrated LFSR reseeding, test-access optimization, and test scheduling for core-based system-on-chip," *IEEE Trans. CAD*, vol. 28, no.8, pp. 1251 -1263, 2009.

[13] M. Tehranipoor, M. Nourani, and K. Chakrabarty, "Nine-Coded Compression Techniques for Testing Embedded Cores in SoCs," *IEEE Trans. on VLSI Systems*, vol. 13, no. 6, pp. 719-722, 2005.

[14] V. Iyengar, and A. Chandra, "Unified SOC Test Approach based on Test Data Compression and TAM Design," *IEE Proc. Computers & Digital Techniques*, vol.152, no. 1, pp. 82-88, 2005.

[15] P.T. Gonciari, P. Rosinger, and B.M. Al-Hashimi, "Compression Considerations in Test Access Mechanism Design," *IEE Proc. Computers & Digital Techniques*, vol.152, no. 1, pp. 89-96, 2005.

[16] A. B. Kinsman and N. Nicolici, "Time-multiplexed test data decompression architecture for core-based SOCs with improved utilization of tester channels," *Proc. ETS*, pp. 196-201, 2005.

[17] Z. Wang., K. Chakrabarty, S. Wang, "SoC Testing Using LFSR Reseeding, and Scan-Slice-Based TAM Optimization and Test Scheduling," *Design, Automation &Test in Europe Conference & Exhibition*, pp.1-6, 2007.

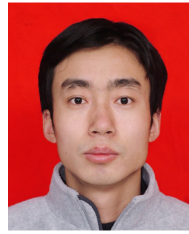
[18] Tieqiao Liu, Yingbo Zhou, Yi Liu and Shuo Cai, "Harzard-Based ATPG for Improving Delay Test Quality," *Journal of Electronic Testing*, vol.31, no.1, pp. 27-34, 2015.

[19] J. Janicki, J. Tyszer, G. Mrugulski, and J. Rajski, "Bandwidth-Aware Test Compression Logic for SoC Designs," *Proc. of European Test Symp.*, 2012

[20] J. Janicki, J. Tyszer, W.-T. Cheng, Y. Huang, M. Kassab, N. Mukherjee, J. Rajski, Y. Dong, G. Giles, "EDT Bandwidth Management – Practical Scenarios for Large SoC Designs," *Proc. of International Test Conference*, Paper 4.3, 2013.

[21] M. Trawka, G. Mrugalski, N. Mukherjee, A. Pogiel, J. Rajski, J. Janicki, J. Tyszer, "High-Speed Serial Embedded Deterministic Test for System-on-Chip Designs," *Proc. of Asian Test Symposium*, pp.74-80, 2014.

[22] S.S. Muthyala, N.A Touba, "SOC Test Compression Scheme Using Sequential Linear Decompressors with Retained Free Variables," *Proc. of VLSI Test Symposium*, pp.31-36, 2013.



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