JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.3, JUNE, 2015
http://dx.doi.org/10.5573/JSTS.2015.15.3.356
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Study on the Thermal Transient Response of TSV Considering the Effect of Electronic-Thermal Coupling

Chunquan Li, Meng-Qiang Zou, Yuling Shang*, and Ming Zhang

***Abstract*—The transmission performance of TSV considering the effect of electronic-thermal coupling is an new challenge in three dimension integrated circuit. This paper presents the thermal equivalent circuit (TEC) model of the TSV, and discussed the thermal equivalent parameters for TSV. Si layer is equivalent to transmission line according to its thermal characteristic. Thermal transient response (TTR) of TSV considering electronic-thermal coupling effects are proposed, iteration flow electronic-thermal coupling for TSV is analyzed. Furthermore, the influences of TTR are investigated with the non-coupling and considering coupling for TSV. Finally, the relationship among temperature, thickness of SiO_2, radius of via and frequency of excitation source are addressed, which are verified by the simulation.**

***Index Terms*—TSV, thermal transient response, electronic-thermal coupling, thermal equivalent circuit, thermal equivalent parameters**

I. INTRODUCTION

Three-dimension (3D) integration, especially 3D integrated circuit (IC) integration, is taking the semiconductor industry by storm. Through Silicon Via (TSV) is one of the most important key enabling technologies of 3D silicon (Si) integration and 3D integration [1]. TSV, which can be used for routing signals, power delivery, and heat extraction [2], provide the structure for the shortest chip-to-chip interconnects and the smallest pad sizes and pitches of interconnects. Compared with other interconnect technologies, such as wire bonding, the advantages of TSV include (1) better electrical performance,(2) higher package density,(3) lower power consumption,(4) lightweight,(5) improved reliability,(6) wider data bandwidth [1, 3]. However, for fabricating vertical interconnects that pass through dies containing substrate, devices and interconnect, the new challenges of TSV are increased especially. With higher signal frequency and more complicated work condition, the impact of electronic-thermal coupling on transmission performance of TSV is a key issue that cannot be ignored.

Experimental method and numerical method can be both used to analyze TSV and other microelectronic units [4-7]. The method based on the equivalent thermal circuits is one of the effective methods in recent researches, in which the thermal transient response can be analyzed accurately and quickly by extracting the thermal resistance, thermal capacity and building the equivalent thermal circuit model [8, 9]. Lau J.H. [10-12] presented an origin of 3D integration, discussed the evolution, challenges, and outlook of 3D IC/Si integrations, and proposed a few generic, low-cost, and thermal-enhanced 3D IC integration system-in-packages with various passive TSV interposes. Yen Y.G [13] elaborated the effect of TSV parameters on the thermal equivalent conductivity of TSV interposer , and studied the effect of TSV interposer on thermal performance of the package based on the objective of compact modeling. Ho S.W·[14] presented a coaxial TSV structure in silicon carrier for high frequency applications. Electrical modeling of the coaxial TSV structure was obtained for impedance matching. Katti G [15] modeled

Manuscript received Dec. 9, 2014; accepted May. 29, 2015
* Corresponding author :Yuling Shang
School of Electrical Engineering and Automation, Guilin University of Electronic Technology,Guilin, Guangxi 541004, China
E-mail : shang_yuling@qq.com

the RLC parameters of the TSV as a function of physical parameters and material characteristics, and proposed a simplified lumped TSV model that can be used to simulate 3-D circuits. The TSV RLC model is applied to predict the resistance, inductance, and capacitances of small geometry TSV architectures. Cadix L [16] proposed a full parametric and frequency dependent model of high aspect ratio TSV based on both electromagnetic simulations and RF measurements. This model enables to extract TSV resistance, self-inductance, oxide capacitance and parasitic elements due to the finite substrate resistivity. Zhu Z.M [17] presented the equivalent thermal model for TSV Based on the one dimensional analytical thermal model for N strata stacked chips without TSV. Zhang Y [18] discussed the Effects of horizontal heat transfer with number of strata, TSV density, TSV diameter and thickness of back end of the line(BEOL) layer under specific process and thermal parameters. Matsumoto K [19] discussed the equivalent thermal conductivity of the interconnection, including BEOL layer, and measured the thermal effect of Cu TSV, meanwhile, the transient thermal measurement was performed and its result was compared with steady state measurement result. Chen Z.H [20] established an analytical solution to calculate equivalent thermal resistances of the TSV structure in both z direction and x-y directions. The effects of the structural parameters such as the thickness of the die, the diameter of copper via and the pitch of the copper via on the equivalent thermal conductivity of composite TSV structure have been investigated.

This paper is organized as follows. In Section II, the thermal equivalent circuit (TEC) model of the TSV is presented. In Section III, thermal transient response (TTR) of TSV interconnection considering electronic-thermal coupling effects are studied. In Section IV, the impact of electronic-thermal coupling on transmission performance of TSV is analyzed. In Section V, Some conclusions are made.

II. MODELING OF TEC FOR TSV INTERCONNECT

1. Structure and Model of TEC for TSV

TSV, shown in Fig. 1 is a cylindrical conduct with an insulating layer filling the gap between the copper metal and the silicon substrate [21], which provides a vertical interconnection to enable different dies to electrical connect. Meanwhile, TSV is electrically isolated from the substrate by a liner formed using an insulating material such as Silicon Dioxide (SiO_2). According to the shape of TSV, there exists several TSV types, such as cylindrical TSV, annular TSV, tapered TSV and coaxial TSV. The most common TSV shape is cylindrical, as shown in Fig. 2(a).

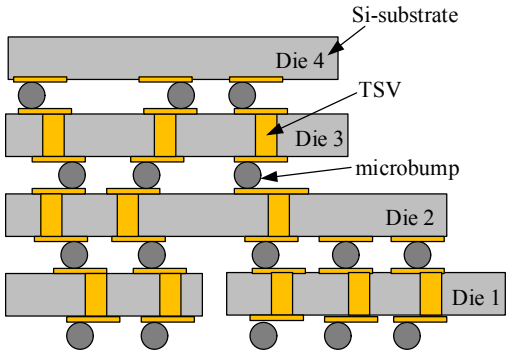


Fig. 1. Structure of TSV.

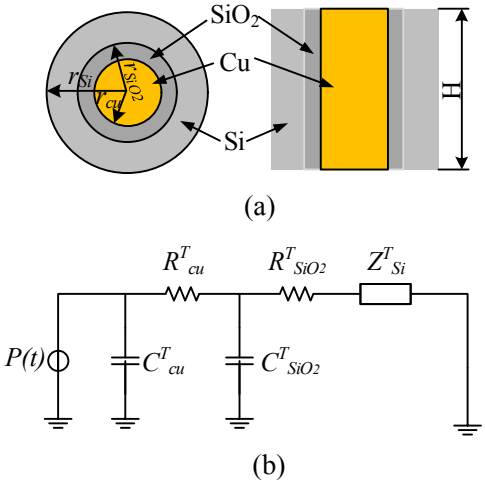


Fig. 2. TEC of TSV.

2. Modeling of TEC

As the slender structure of TSV, the effect of thermal conductivity along vertical direction of TSV is very smaller than that along Radial direction of TSV, and the thermal conductivity along vertical direction can be ignored [20]. So, thermal management mainly focuses on the radial direction for single cylindrical TSV. Radial direction model of lumped TEC for TSV is built as

shown in Fig. 2(b), in which, P is applied power, R_{Cu}^T, $R_{SiO_2}^T$ is the thermal resistance of Cu layer and SiO_2 layer, respectively, C_{Cu}^T, $C_{SiO_2}^T$ is the thermal capacity of Cu layer and SiO_2 layer respectively. The precise thermal characteristic of the Si layer cannot be equivalent to thermal capacitance and thermal resistance. As the distance between TSV are relatively farther than the diameters of Cu, there exists large temperature gradient in the Si layer with the effect of thermal conductivities. With the farther distance from the Cu via, the temperature gets lower, which is the same as transmission line characteristic. Thus, model of TEC for Si layer is equivalent to the transmission line, and Z_{Si}^T is equivalent thermal parameters.

3. Thermal equivalent parameters of TEC

3.1 Thermal resistance

According to the first law of thermo dynamics, thermal resistance with homogeneous materials can be given by [22]:

$$R^T = \frac{\sigma}{\lambda A} \tag{1}$$

where σ is the thickness of the material, λ is the thermal conductivity of the material, A is the area. So thermal resistance of Cu, thermal resistance of SiO_2 and thermal resistance of unit thickness Si can be given by :

$$R_{Cu}^T = \frac{1}{\lambda 2\pi H}\ln r_{cu} \tag{2}$$

$$R_{SiO_2}^T = \frac{1}{\lambda 2\pi H}\ln \frac{r_{sio_2}}{r_{cu}} \tag{3}$$

$$R_{Si}^T = \frac{1}{\lambda 2\pi r_{si} H} \tag{4}$$

where r_{cu}, r_{sio_2} and r_{si} is the radius of Cu, SiO_2 and Si, respectively. H is the height of the TSV.

3.2 Thermal capacity

The thermal capacity of TSV is given by [22]:

$$C^T = \rho.c_p.V \tag{5}$$

where ρ is the density of the material, c_p is specific heat of the material. V is the volume of the material. So, the thermal capacity of Cu, SiO_2 and the unit layer of Si can be given by:

$$C_{Cu}^T = \rho_{Cu}.c_{Cu}.V_{Cu} \tag{6}$$

$$C_{Sio_2}^T = \rho_{Sio_2}.c_{Sio_2}.V_{Sio_2} \tag{7}$$

$$C_{Si}^T = 2\rho_{Si}.c_{Si}.\pi r_{Si} H \tag{8}$$

3.3 Impedance of Si layer

The silicon layer between TSV is simplified to uniform transmission line in this paper, according to the property of the transmission line, and the input impedance is given by [23]:

$$Z_{Si}^T(s) = Z_0^T \tanh(\theta h_{si}) \tag{9}$$

where (9) can be represented by Taylor expansion:

$$\begin{aligned} Z_{Si}^T(s) &= Z_0^T \tanh(\theta h_{si}) \\ &= R_{Si}^T h_{si} - \frac{1}{3}R_{Si}^{T2}C_{Si}^T h_{si}s + \frac{2}{15}R_{Si}^{T3}C_{Si}^{T2}h_{si}s^2 + \ldots \end{aligned} \tag{10}$$

where

$\theta = \sqrt{sR_{Si}^T C_{Si}^T}$

$Z_0^T = \sqrt{R_{Si}^T / sC_{Si}^T}$

$h_{si} = r_{si} - r_{sio2}$, h_{si} is the thickness of Si layer.

III. Thermal Transient Response of TSV Considering Electronic-Thermal Coupling Effects

1. Equation of TTR

According to Fig. 2(b), the input impedance of TEC for TSV is given by:

$$Z_{in}^T(s) = \cfrac{1}{sC_{Cu}^T + \cfrac{1}{\cfrac{1}{\cfrac{1}{Z_{Si}^T(s) + R_{SiO_2}^T} + sC_{sio_2}^T} + R_{Cu}^T}} \tag{11}$$

where $Z_{in}^{T}(s)$ is the input impedance of TEC. Based on model reduction of moment matching, Eq. (11) can be represented by:

$$Z_{in}^{T}(s) = R_q / (1+\tau_q s) \tag{12}$$

where

$$R_q = R_{Cu}^{T} + 1/m_1$$

$$\tau_q = (R_{Cu}^{T} + 1/m_1).(m_2/m_1(R_{Cu}^{T} + 1/m_1)^2 + C_{Cu}^{T})$$

$$m_1 = 1/(R_{sio_2}^{T} + R_{Si}^{T} h_{si})$$

$$m_2 = C_{Cu}^{T} + r^2 C_{Si}^{T} h^3{}_{si}/3\left(R_{SiO_2}^{T} + R_{Si}^{T}\,\mathrm{h}_{si}\right)^2$$

Temperature of TSV in Complex frequency domain is given by [24]:

$$T^{tsv}(s) = Z_{in}^{T}(s)P(s) \tag{13}$$

where $T^{tsv}(s)$ is the temperature of TSV, $P(s)$ is applied power in the frequency domain.

The excitation source of periodic square wave is used in this paper, which is represented as:

$$v_{in}(t) = v[u(t) - u(t-\frac{T}{2}) + u(t-T) - ...] \tag{14}$$

where v is the applied voltage, $u(t)$ is unit step function, T is the period of excitation source. The Laplace transform of $v_{in}(t)$ is:

$$v_{in}(s) = v\frac{1}{s(1-e^{(-sT)})})[1-e^{(-\frac{sT}{2})}] \tag{15}$$

According to equipment model of power [25], power caused by the *n*th period of excitation source is obtained:

$$p_n(t) = \frac{v_{in}(t)^2}{R^E} = \frac{v^2}{R^E} e^{[-\frac{2t-nT}{R^E C^E}]}.u(t-\frac{nT}{2}) \tag{16}$$

In which, n = 0,1,2,3,$\cdots$, R^E is the resistance of Cu, C^E is the capacitance of Cu.

$$R^E = \rho\frac{H}{\pi r_{cu}^2}$$

$$C^E = (1/C_{Si}^{E} + 1/C_{SiO_2}^{E} + 1/C_{Cu}^{E})^{-1}$$

The Laplace transform of $p_n(t)$ is:

$$p_n(s) = \frac{v^2}{R^E}.\frac{1}{s+\frac{2}{R^E C^E}} e^{(-\frac{snT}{2})} \tag{17}$$

The increased temperature at the *n*th period of the excitation source:

$$T_n^{tsv}(s) = \frac{v^2 R_q}{R^E \tau_q}.\frac{1}{[s+\frac{2}{R^E C^E}][s+\frac{1}{\tau_q}]} e^{(-\frac{snT}{2})} \tag{18}$$

The Laplace inverse transform of $T_n^{tsv}(s)$ is:

$$T_n^{tsv}(t) = \frac{V^2.R_q}{R^E(\frac{2\tau_q}{C^E} - R^E)}[e^{-\frac{t-\frac{nT}{2}}{\tau_q}} - e^{-\frac{2t-nT}{R^E C^E}}].u(t-\frac{nT}{2}) \tag{19}$$

The transient temperature of TSV at the *n*th period of excitation source is:

$$T^{tsv}(t) = \sum_{k=0}^{n}\frac{V^2 R_q}{R^E(\frac{2\tau_q}{C^E} - R^E)}[e^{-\frac{t-\frac{kT}{2}}{\tau_q}} - e^{-\frac{2t-kT}{R^E C^E}}].u(t-\frac{kT}{2}) + T_0 \tag{20}$$

where T_0 is the initial temperature.

2. TTR of TSV Considering Electronic-Thermal Coupling Effects

However, resistivity is related to temperature. With the increase of temperature, the resistivity of Cu increases. $R^E(t)$ is represented as:

$$R^E(t) = [1 + a_0 T(t)]R^E(t_0) \tag{21}$$

In which, a_0 is the temperature coefficient of Cu. Substitute (21) into (16), $p_n(t)$ is as follows:

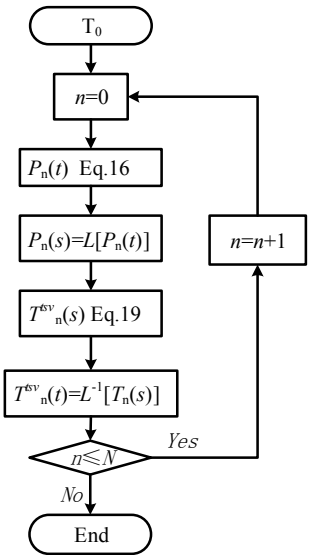


Fig. 3. Iteration flow electronic-thermal coupling for TSV.

$$p_n(t) = \frac{v_{in}(t)^2}{[1+a_0T(t)]R^E(t_0)} = \frac{v^2}{[1+a_0T(t)]R^E(t_0)} e^{\left[-\frac{2t-nT}{[1+a_0T(t)]R^E(t_0)C^E}\right]} u(t-\frac{nT}{2}) \quad (22)$$

Temperature considering electronic-thermal coupling effects is obtained by iteration computation, which is shown in Fig. 3. N is the maximum iteration of stopping iteration.

IV. SIMULATION AND DISCUSSIONS

1. Simulation

Table 1 shows the thermal parameters of TSV. The initial temperature is 20℃, the voltage and frequency of excitation source is 0.2v and 1 GHz, respectively. r_{cu} is 4um, thickness of SiO_2 layer(h_{sio_2})is 100 nm, h_{si} is 10 um, and H is 100 um. TTR of TSV is shown in Fig. 4, which compares the temperature transient response of three-dimensions (3D) field simulation software (COMSOL Multi-physics ®) with that of the thermal circuit model proposed in this paper. ΔT_m is the difference of temperature between considering coupling of TEC and non-considering coupling of TEC, ΔT_c is the difference of temperature between considering coupling of COMSOL and non-considering coupling of COMSOL, ε_1 is the difference of temperature between non-considering coupling of TEC and that of COMSOL, and ε_2 is the difference of temperature between considering coupling of TEC and that of COMSOL. Fig. 4 indicates that the results of two methods are very similar with ε_1 or ε_2 < 3%. For ΔT_m or ΔT_c , the temperature at considering coupling is higher than temperature at non-considering coupling. Setting difference coefficient for temperature is defined by $\delta(t) = \Delta T(t) / T(t) \times 100\%$. When t = 5000ns, difference coefficient of TEC $\delta_m(5000)$ = 10.36%, difference coefficient of COMSOL $\delta_c(5000)$ = 12.37%. So it proved that the effects of coupling are obviously. However, the calculation time of TEC is 0.1s, which is far more less than that of COMSOL(4580s).

Tab1e 1. Thermal parameters of the interconnect system

Materials	$K(W/{}^0C.m)$	$\rho(kg/m^3)$	$c_p(J/{}^0C.kg)$
Cu	400	8700	390
SiO_2	1.4	2200	730
Si	130	2329	700

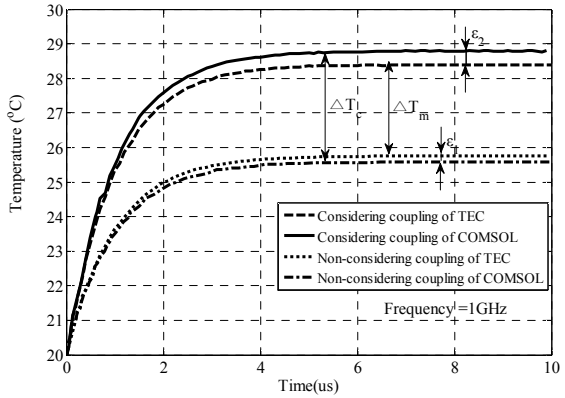


Fig. 4. Temperature transient response of TSV.

2. Discussions

2.1 Relationship between temperature and frequency of excitation source.

When the signal frequency is applied by 100 MHz, 1 GHz, 10 GHz on the TSV respectively, the transient temperature responses are in Fig. 5.

Fig. 5 indicates that (1) the variation trend of TTR is that temperature gradually increases with the increase of

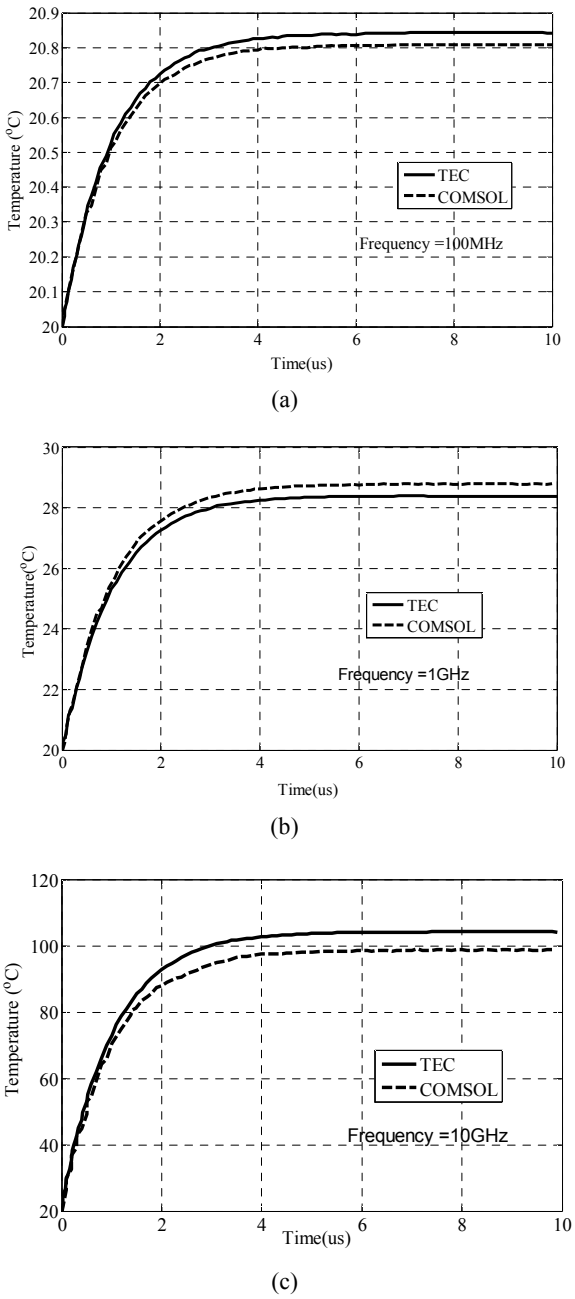


Fig. 5. Transient thermal responses of the TSV under different frequencies.

time. Temperature grows rapidly in initial part (t<4000 ns), and it grows smoothly in the later period (t≥4000 ns).(2) When the frequency gets higher, the steady state temperature response grows larger. At 10000 ns, the steady state temperature response are 20.84℃, 28.4℃ and 104℃ for the frequency of 100 MHz, 1 GHz and 10 GHz, respectively.(3) The rise rate of transient temperature grows with the increase of frequency. At 4000 ns, in Fig. 5(a), the improved

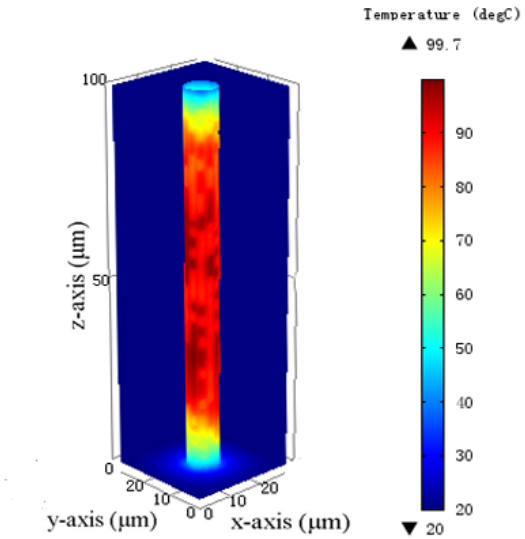


Fig. 6. Three-dimensional temperature distribution over the TSV at the time of $t \approx 10$ μs.

temperature is 0.8℃ when frequency is 100 MHz, and the rise rate of temperature is 0.8/20×100% = 4%. In Fig. 5(b), the improved temperature is 8.4℃ when frequency is 1 GHz, the rise rate of temperature is 8/20×100% = 40%. In Fig. 5(c), the improved temperature is 80℃ when frequency is 1 GHz, the rise rate of temperature is 80/20×100% = 400%. So, the Condition of steady state response of temperature for TSV is:

$$\Delta T^{tsv} = T^{tsv}(t+\frac{T}{2}) - T^{tsv}(t) = \frac{V^2 R_q}{R^E(2\frac{\tau_q}{C^E} - R^E)}(e^{-\frac{1}{\tau_q}} - e^{-\frac{2t}{RC}})u(t) < \varepsilon \quad (23)$$

where ΔT^{tsv} is the variation of temperature for TSV.

The increase of temperature is caused by applied power of each periodic square wave pulse. With the increasing of frequency of applied excitation source, periodic pulse is increase, and then the power is accumulated which lead to the increase of temperature. So, the temperature of TSV reaches over 100℃ during applying 10 GHz power to the TSV.

The 3-D temperature distribution obtained by COMSOL software of TSV is as shown in Fig. 6. The initial temperature is 20℃. Air convection with convection coefficient of 10W/m^{2}K is applied to the both top and bottom of the TSV[27]. Its geometry is described

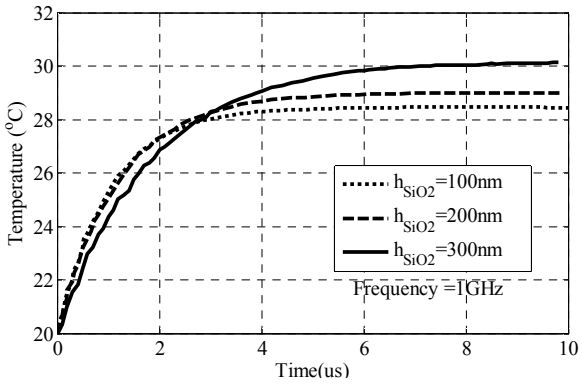


Fig. 7. Temperature response of TSV under the variation of h_{SiO_2}.

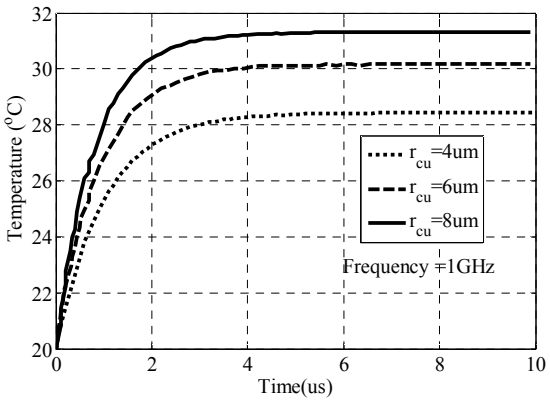


Fig. 8. Temperature response of TSV under the variation of r_{cu}.

by r_{cu} = 4 um, h_{sio2} = 10 um, H = 100 um, h_{si} = 10 um, respectively. The applied voltage pulse and frequency of excitation source is 0.2 V and 10 GHz, respectively. The maximum temperature of the TSV is about 99.7℃ in Fig. 6, which appears near the middle of Cu layer for there exists a heat transfer along vertical TSV.

2.2 Relationship between temperature and thickness of SiO_2

Fig. 7 shows the Relationship between temperature and thickness of SiO_2, in which applied voltage is 0.2 v, initial temperature is 20℃, frequency is 1 GHz.

With the increase of h_{sio_2}, Fig. 7 illustrates that (1) the steady temperature of TSV gets higher;(2) response time of steady temperature for TSV gets longer. The reason is that R_q and τ_q is increased with the increase of h_{sio_2}, and then the transient temperature for TSV is getting higher when the R_q increases. Meanwhile, the response rate of transient temperature is related to τ_q, response time of steady temperature is slower while τ_q gets larger.

2.3 Relationship between temperature response and radius of Cu

With the increase of r_{cu}, Fig. 8 illustrates that (1) the steady temperature of TSV gets higher; (2) response time of steady temperature for TSV get shorter. The reason is that R^E and is decreased with the in-crease of r_{cu}, and then the transient temperature for TSV is getting higher when the R^E decreases. Meanwhile, the response time of steady temperature is shorter while τ_q gets smaller.

V. CONCLUSIONS

There are more and more attention paid to the development of TSV interconnect for its high functionalize and good performance in 3D IC system integration. This paper presents the TEC model of the TSV, and then it discusses the thermal equivalent parameters for TSV. According to the thermal characteristic of Si layer, the model of Si layer is equivalent to the transmission line. TTR of TSV considering electronic-thermal coupling effects are proposed, the equation of analytical solution of TEC is obtained under the excitation source of periodic square wave, and then the iteration flow electronic-thermal coupling for TSV is analyzed. The influences of TTR are investigated with the non-coupling and considering coupling for TSV, which are proved that: (1) the results of two method, TEC and FEM, are very similar with ε_1 or ε_2 < 3%;(2) the temperature at considering coupling is higher than temperature at non-considering coupling, the effects of coupling are obviously;(3) the calculation time of the TEC is far less than that of FEM. Finally, the relationship among temperature, thickness of SiO2, radius of Cu and frequency of excitation source are addressed. The following are verified by the simulation: (1) the rise rate of transient temperature grows with the increase of frequency; (2) the steady temperature of TSV gets higher with the increase of thickness of SiO_2;(3) the steady temperature of TSV gets higher with the increase of radius of Cu.

ACKNOWLEDGMENTS

The research work reported in this paper is supported by the National Natural Science Foundation of China (Nos.51165004, 51465013), the Natural Science Foundation of Guangxi Province (No.2012GXNSFDA0530 29), Guangxi Key Laboratory of Manufacturing System and Advanced manufacturing technology (Nos. 10-046-07_004), Innovation Project of GUET Graduate Education(Nos.GDYCSZ201443, GDYCSZ201480) and Guangxi Key Laboratory of Automation Test and Instrumentation (No.YQ15109)

REFERENCES

[1] Lau, J.H., "Through-Silicon Vias for 3D Integration," *New York, McGraw-Hill*, 2012

[2] Bakir, Muhannad S., et al., "3D heterogeneous integrated systems: liquid cooling, power delivery, and implementation." *Custom Integrated Circuits Conference, IEEE*, pp.663–670. Sep., 2008

[3] Khan, N. and S. Hassoun, "Designing TSVs for 3D Integrated Circuits," *New York, Springer*, 2012.

[4] Yang, Ping, and Zixia Chen. "Experimental approach and evaluation on dynamic reliability of PBGA assembly," *Electron Devices, IEEE Transactions on* 56.10, pp.2243-2249, 2009.

[5] Liu, D. J., et al. "Effect of temperature and voltage on LED luminaries reliability." *International Journal of Materials and Structural Integrity*, Vol.6(2), pp. 270-283, 2012.

[6] Xi, T., et al., "Numerical investigation on the thermal reliability and layout optimization of printed circuit board level," *International Journal of Materials and Structural Integrity*,. Vol.6(2), pp. 309-318, 2012.

[7] Shang, Yuling, et al. "Study on the crosstalk characteristic of non–ideal interconnect structure," *International Journal of Materials and Structural Integrity,* Vol.7(1), pp.144-159, 2013

[8] Jang, Dong Min, et al. "Development and evaluation of 3-D SiP with vertically interconnected through silicon vias (TSV)," *Electronic Components and Technology Conference, 2007, ECTC'07, Proceedings. 57th. IEEE*, pp. 847-852, May, 2007

[9] Swift, G., T.S. Molinski and W. Lehn, "A fundamental approach to transformer thermal modeling. I. Theory and equivalent circuit," *Power Delivery, IEEE Transactions on*, Vol.16(2): pp. 171-175, 2001

[10] Lau, John H. "Evolution and outlook of TSV and 3D IC/Si integration," *Electronics Packaging Technology Conference, 2010, EPTC, 12th. IEEE*, pp. 560-570, 2010

[11] Lau, J. H. "Evolution, challenge, and outlook of TSV, 3D IC integration and 3D silicon integration," *Advanced Packaging Materials (APM), 2011 International Symposium on IEEE*, pp. 462-488, Oct. 2011

[12] Lau J H. "TSV manufacturing yield and hidden costs for 3D IC integration," *Electronic Components and Technology Conference (ECTC), 2010 Proceedings 60th. IEEE*, pp.1031-1042, June, 2010

[13] Hoe Y Y G, Yue T G, et al. Effect of TSV interposer on the thermal performance of FCBGA package," *Electronics Packaging Technology Conference, 2009. EPTC'09. 11th. IEEE*, pp.778-786, Dec. 2009

[14] Ho S W, Yoon S W, Zhou Q, et al. "High RF performance TSV silicon carrier for high frequency application," *Electronic Components and Technology Conference, 2008. ECTC 2008. 58th. IEEE*, pp.1946-1952, May, 2008

[15] Katti G, Stucchi M, De Meyer K, et al. "Electrical modeling and characterization of through silicon via for three-dimensional Ics," *Electron Devices, IEEE Transactions on*, pp.256-262, 2010

[16] Cadix L, Farcy A, Bermond C, et al. "Modelling of through silicon via RF performance and impact on signal transmission in 3D integrated circuits," *3D System Integration, 2009. 3DIC 2009. IEEE International Conference on. IEEE*, pp.1-7, Sep. 2009

[17] Zhu, Z., Z. Ping and Y. Yintang, "An analytical thermal model for 3D integrated circuit considering through silicon via," *Chinese Journal of Physics*, Vol.60(11), pp. 118401-118406, 2011

[18] Yan, Z., et al., "Thermal Management of 3D Integrated Circuits Considering Horizontal Heat Transfer Effect," *Chinese Journal of Computational Physics*, Vol.30(5), pp.753-758, 2013

[19] Matsumoto K, Ibaraki S, Sueoka K, et al. "Experimental thermal resistance evaluation of a three-dimensional (3D) chip stack, including the transient measurements," *Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2012 28th Annual IEEE. IEEE*, pp.8-13, 2012

[20] Chen Z, Luo X, Liu S. "Thermal analysis of 3D packaging with a simplified thermal resistance network model and finite element simulation," *Electronic Packaging Technology & High Density Packaging (ICEPT-HDP), 2010 11th International Conference on IEEE*, pp.737-741, 2010

[21] Kannan, S., B. Kim and B. Ahn, "Fault Modeling and Multi-Tone Dither Scheme for Testing 3D TSV Defects," *Journal of Electronic Testing*, Vol.28(1), pp. 39-51, 2012

[22] Salome P, Leroux C, Crevel P, et al. "Investigations on the thermal behavior of interconnects under ESD transients using a simplified thermal RC network," *Microelectronics Reliability*, Vol.39(11), pp.1579-1591, 1999

[23] Uchino T, Cong J. "An interconnect energy model considering coupling effects," *Computer-Aided Design of Integrated Circuits and Systems, IEEE* Transactions on, Vol.21(7), pp.763-776, 2002

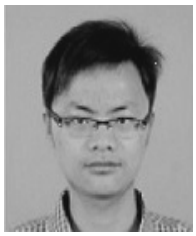
[24] Papanikolaou, A., D. Soudris and R. Radojcic, "Three Dimensional System Integration," *New York, Springer*, 2011

[25] Li X C, Mao J F, Huang H F. "Accurate analysis of interconnect trees with distributed RLC model and moment matching," *Microwave Theory and Techniques, IEEE Transactions on, Vol.52(9)*: pp.2199-2206, 2004

[26] Wang X P, Yin W Y, He S L. "Multiphysics Characterization of Transient Electrothermomechanical Responses of Through-Silicon Vias Applied With a Periodic Voltage Pulse," *Electron Devices, IEEE Transactions on, Vol.57(6)*: pp.1382-1389, 2010

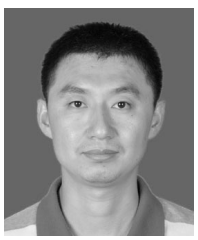
[27] Xie J Y, Xie B C, Madhavan S. "Electrical-thermal modeling of through-silicon via (TSV) arrays in interposer." *International Journal of Numerical Modelling*, *Vol.26 (6)* : pp.545-559, 2013

Chunquan Li is a professor in Guilin University of Electronic Technology. He received his Ph.D in Mechanical Engineering from Shanghai University in 2010. He has authored over 40 professional and scholarly publications in famous international journal or international conference in the specialized field of the microelectronics manufacturing technology, advanced manufacturing technology.



Meng-Qiang Zou received the Bachelor of Engineering degree in the Department of mechanical design manufacturing and automation from Jinggangshan University, China, in 2013. He is currently pursuing the Master of Engineering degree in Guilin University of electronic technology, China, where he has been working in the cable multidisciplinary analysis. His interests include the TSV signal integrity analysis and cable reliability analysis.

Yuling Shang is currently an associate professor in Guilin University of Electronic Technology in China. She received her PhD in Circuits and Systems from Xi'an University of Electronic Science and Technology in 2010. Her research interests focus on the signal integrity, fault diagnosis and testing technique. She has authored over 10 professional and scholarly publications in famous international journal or international conference in the specialised field of the signal integrity, fault diagnosis and testing technique.



Ming Zhang received the B.Eng. and M.Eng. degrees from Guilin University of Electronic Technology Engineering, Guilin, China, in 2001 and 2006. After graduation, he joined the Guilin University of Electronic Technology Engineering. He is the Faculty of Teaching and Practice Center, Guilin University of Electronic Technology Engineering, Guilin, China, where he is currently Lecturer. His research interests include the microelectronics manufacturing technology, advanced manufacturing technology.