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An OTA with Positive Feedback Bias Control for Power Adaptation Proportional to Analog Workloads

Byungsub Kim, Jae-Yoon Sim, and Hong-June Park

Abstract—**This paper reports an adaptive positive feedback bias control technique for operational transconductance amplifiers to adjust the bias current based on the output current monitored by a current replica circuit. This technique enables operational transconductance amplifiers to quickly adapt their power consumption to various analog workloads when they are configured with negative feedback. To prove the concept, a test voltage follower is fabricated in 0.5-μm CMOS technology. Measurement result shows that the power consumption of the test voltage follower is approximately linearly proportional to the load capacitance, the signal frequency, and the signal amplitude for sinusoidal inputs as well as square pulses.**

Index Terms—**Analog circuits, bias adaption, low power circuits, operational trans-conductance amplifier, positive feedback bias control**

I. INTRODUCTION

Bio-medical devices [1] have large demand for low-power operational trans-conductance amplifiers (OTAs) because OTAs are typically the most power-consuming blocks in these applications. However, conventional OTAs are not power-efficient because their bias currents are fixed for the expected worst workloads (load capacitance, signal frequency, and signal amplitude) even though workloads are usually time-varying [2, 3]. For example, electrocardiography (EKG) pulses sparsely occur and also the workloads do [4]. In a switched-capacitor circuit, load capacitance varies when connection changes [5, 6]. Therefore, OTAs designed for the peak workload without adaptive bias control waste unnecessary power.

To improve OTAs' power efficiency, various bias control techniques were proposed [7-10]. Bias control based-on input motoring [7, 8] improved slew rate with little additional power, and thus achieved the same performance consuming less power. Load adaptation also improved slew rate by 400%-500% with only additional 5% power and 20% chip area [9]. A positive feedback bias control technique [10] adapted OTA's power consumption proportional to various workloads.

However, the previous research [7-10] did not demonstrate subtle power adaption to sophisticated analog signals. Some previous articles [7-9] focused mostly on OTAs' slew rate improvement in driving square pulses. The report on positive feedback bias control [10] discussed power adaption only to square pulse signals. For square pulses, the bias adaption is similar to simple digital bias programming [11] or simple bias switching [12]: the bias current either 1) stays constant while input stays constant or 2) abruptly peaks during transition period. This control is different from sophisticated power adaption required for other analog signals such as sinusoids.

This paper shows that the positive feedback technique can subtly adapt power consumption of an OTA to sinusoidal signals as well as square pulse signals. In experiment, a test voltage follower adaptively consumed power roughly proportional to the signal frequency, the

Manuscript received Sep. 29, 2014; accepted Nov. 20, 2014
Department of Electrical Engineering, Pohang University of Science and Technology, Pohang, Gyeongbuk, Republic of Korea
E-mail : byungsub@postech.ac.kr

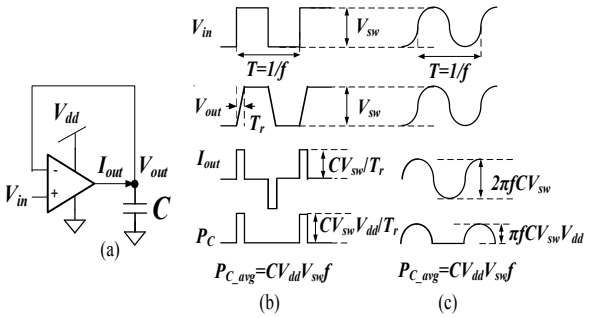


Fig. 1. An example of OTA operation in a voltage follower (a) driving a square pulse (b) and driving a sinusoid (c). V_{in} is the input voltage. V_{out} and I_{out} are the voltage follower's output voltage and current. P_C is the power drawn from the supply to charge the load capacitor. P_{C_avg} is the average of P_C.

signal swing, and the load capacitance not only for square pulses but also for sinusoidal inputs, showing that OTA-based analog circuits can adapt to sophisticated analog signals using the concept.

This paper is organized as follows. Section II explains power waste in a typical OTA usage. Section III describes the mechanism and circuit implementation of the positive feedback bias control technique for OTAs. Section IV shows the experimental results. Finally, Section V concludes this paper.

II. POWER WASTED BY AN OTA

Conventional OTAs, which always provide large driving ability, waste unnecessary power because large driving strength is only occasionally required in typical bio-applications [1]. Fig. 1 shows an example OTA operation in a voltage follower driving a square pulse or a sinusoid. For a square pulse in Fig. 1(b), the OTA does not have to conduct large current to the load while the input and output (V_{in} and V_{out}) stay constant, but must have large gain to maintain negative feedback. Therefore, during this phase, the OTA needs only small power just enough to maintain the large gain. In contrast, at signal transition (during the rise time T_r), the OTA's differential input becomes abruptly large and the OTA must conduct large current to the load, burning large instantaneous power. Once the output voltage follows to the input voltage, the OTA does not have to conduct large current to the load capacitor anymore consuming little instantaneous power.

For a square wave with amplitude of V_{sw}, the power drawn from the supply to charge the load capacitor is

$$P_C = CV_{dd}V_{sw}f\,, \tag{1}$$

where P_C, V_{dd}, C, V_{sw}, f (= $1/T$), and T are the power drawn from the supply to charge the load capacitor, the supply voltage, the load capacitance, the voltage swing, the switching frequency, and the clock period, respectively. Similarly, when the voltage follower drives a sinusoid as shown in Fig. 1(c), the ideal power dissipation can be expressed by Eq. (1) too.

Since a conventional OTA always prepares for the peak workload, we can find the minimum bound of the OTA power consumption as

$$P_{OTA} > V_{dd}C_{\max}V_{sw\_\max}/T_r > 2V_{dd}C_{\max}V_{sw\_\max}f_{\max}\,, \tag{2}$$

where P_{OTA}, C_{max}, V_{sw_max}, and f_{max} are the minimum bound of the OTA power consumption, the maximum load capacitance, the largest voltage swing, and the maximum signal frequency, respectively. Conventional OTAs burn unnecessary power most of the time since the peaking times of C, V_{sw}, and f are generally short in bio-medical applications.

III. A POSITIVE FEEDBACK BIAS CONTROL FOR OTA

Fig. 2 shows a schematic diagram of an OTA with the positive feedback bias controller. The OTA core has three bias control transistors: M_1, M_2, and M_3. The transistor M_1 controls most of OTA's the bias current ($i_1(t)$) through positive feedback. The transistor M_2 sets the maximum current limitation ($i_{\max}$) flowing through M_1 by the bias voltage V_{b1}. The transistor M_3 provides the small minimum bias current $i_{\min}$ when M_1 transistor completely turns off. Therefore, the OTA's bias current can be approximated as $i_{bias}(t) = i_1(t)+i_{min} \approx i_1(t)$. The current replica duplicates the output current $i_{out}(t)$ of the OTA and feed it to the current rectifier which produces $|4i_{out}(t)|$ by current mirroring. The current comparator compares $|4i_{out}(t)|$ with $i_1(t)/5+i_b$, where i_b is the minimum current provided by M_6 transistor to prevent the comparator to turn off completely. Because i_{min} and i_b are small, $i_1(t)/5+i_b \approx i_1(t)/5 \approx (i_1(t)+i_{min})/5 \approx i_{bias}(t)/5$. Therefore, the current comparator approximately compares $|4i_{out}(t)|$ with the scaled bias current $i_{bias}(t)/5$ to determine adaption direction. If $|4i_{out}(t)|$ is approximately

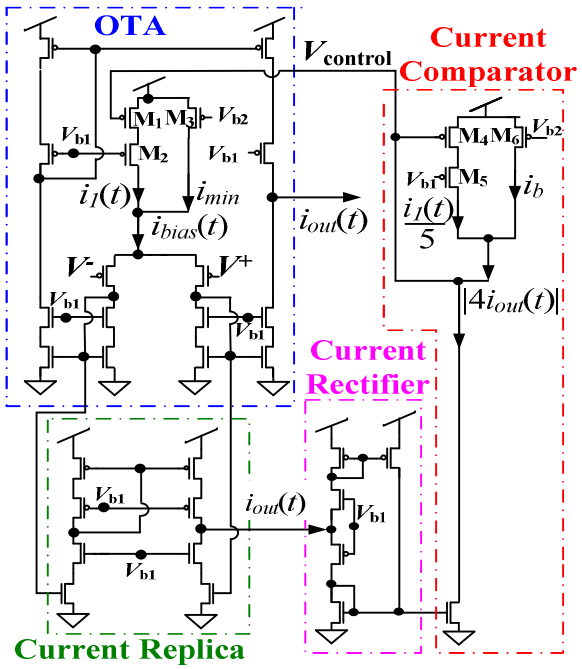


Fig. 2. An OTA with positive feedback bias control [7].

larger than $i_{bias}(t)/5$, i.e. $|i_{out}(t)| > 0.05 i_{bias}(t)$, then the controller increases the bias current considering that it is too small. Otherwise, the controller reduces the bias current.

This bias control algorithm forms a positive feedback because increasing the output current increases the OTA's trans-conductance by increasing the bias current, and thus further raises the output current. Similarly, decreasing the output current also eventually further decreases the output current. By the nature of positive feedback, the bias controller quickly responds to small change of the output current.

Divergence of the bias current from the proper range due to the positive feedback is prevented 1) by the overall negative feedback and also 2) by the bias current limitations. OTAs are typically configured with negative feedback as shown in Fig. 1(a). Even though the positive feedback changes the bias current and the OTA's gain, the output voltage will eventually converge to the input voltage making the OTA's output current small due to the negative feedback. For a small output current, the positive feedback will eventually decrease the bias current. Therefore, the negative feedback prevents the positive feedback to keep increasing the bias current. Another mechanism to prevent the bias current from diverging is maximum/minimum bias current limitations. The positive feedback may keep increasing/reducing the bias current until it becomes infinity/zero causing circuit problems. For example, if the rise time T_r is too long in Fig. 1(b), then the positive feedback may increase the bias current too much and transistors may not stay in the saturation region. In contrast, if the input in Fig. 1(b) stays settled too long, then the positive feedback will make the bias current too small for the OTA to response to input quickly. Current limiters constraining the maximum/minimum bias current can easily fix these problems. To guarantee that the two mechanisms collaboratively maintain stability, the OTA is designed to be stable for any fixed bias value within the range between the minimum and the maximum bias currents. When the OTA is stabilized well by these mechanisms, the OTA's bias current decreases from the maximum current to the minimum current for a step input [10]. The settling time can be approximated by taking into account the slew time, exponential transition time, and bias changing time as discussed in [10].

IV. Experiment

A test voltage follower in Fig. 1(a) using the OTA in Fig. 2 was fabricated in 0.5-μm CMOS technology and operated with a 3 V supply. To test the adaptation to various loads, three load capacitors (1 pF, 10 pF, and 100 pF) were selectively connected during the test with various input signals.

1. DC Characteristics

Table 1 summarizes the dc characteristics of the test voltage follower measured for a dc 1.5 V (half-rail voltage) input. The idle power including the OTA core, the controller, and the bias voltage generator is 1.38 μW. Within the measured input range (0.37 V-2.66 V), the measured differential error input (V_{in} - V_{out}) is less than 15 mV showing that the output tracks the input well.

Due to the positive feedback, the bias current has two stable states for dc inputs. Fig. 3 shows the output voltage and the supply current versus the input voltage measured at dc. The output tracks the input well within the operating range because the OTA maintains large gain for negative feedback in this region. As explained in Section III, as long as the negative feedback works, for

Table 1. Measured DC characteristics of the voltage follower using the OTA with positive feedback bias control

Supply voltage	3 V
Reference voltage	1.5 V
Idle power (1.5 V DC input)	1.38 μW
Operating input voltage range	0.37 V - 2.66 V
V_{in} - V_{out}	< 15 mV

The measured power consumption includes the op-amp core, the bias controller, and the bias voltage generator.

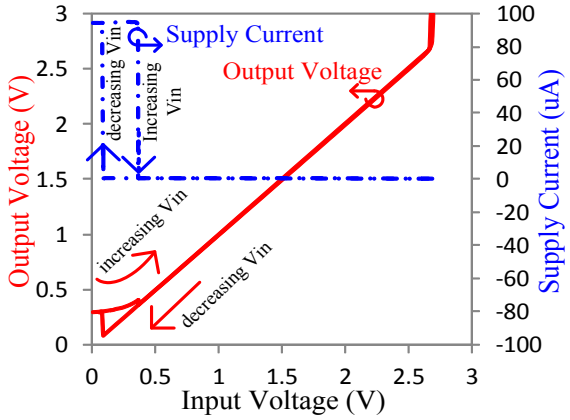
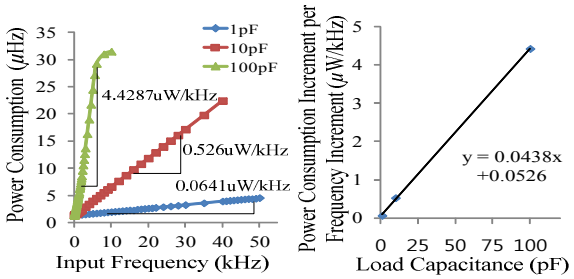


Fig. 3. The measured output voltage and supply current versus the input voltage: The measurement was done twice with a 1-pF load capacitor increasing and decreasing V_{in}.

dc input, the positive feedback keeps decreasing the bias current to the minimum value resulting in the minimum supply current within this region as shown in Fig. 3. However, because the OTA loses large gain outside this region, the negative feedback may not work, resulting in large differential input which may flip the direction of the positive feedback toward increasing the bias current up to the maximum limit. In Fig. 3, by this mechanism, the supply current below operating range is the maximum value.

The two stable the bias current values (the minimum and maximum limitations) cause the hysteresis in Fig. 3. Because the bias current determines the operating input voltage range, different initial bias currents result in different flipping points for the positive feedback direction. For example, when V_{in} is increasing from V_{in} = 0, the initial bias current is the maximum value causing the maximum supply current (94 μA) when V_{in} = 0 as Fig. 3 shows. The minimum operating input voltage for this bias current is 0.37 V, and thus the OTA does not properly work for V_{in} < 0.37 V. As V_{in} slowly increases, the OTA starts working around at V_{in} = 0.37 V, and thus the bias current as well as the supply current decreases to



(a) (b)

Fig. 4. Measured power consumption of the voltage follower versus input frequency [7] (a), and power consumption increment per frequency increment versus the load capacitance (b). The input signal was a 0.5V_{pp} square wave.

the minimum as shown in Fig. 3. On the other hand, when V_{in} is decreasing, the initial bias current is the minimum value and the minimum operating input voltage is about 0.08 V. As Fig. 3 shows, the supply current suddenly increases to its maximum value around 0.08 V due to the sudden increase of the bias current as V_{in} increases.

Since the hysteresis occurs outside the operating ranges of two cases, restricting the operating range as the intersection of the both regions makes the dc characteristic of the voltage follower similar to the one of a normal voltage follower with the minimum bias current.

2. Adaptation to Square Wave Inputs

Various square pulses are applied to the voltage follower with various load capacitors to test the adaptation. The measured power dissipation is approximately proportional to the frequency, the load capacitance, and the signal swing.

Fig. 4(a) shows the measured power consumption versus the input frequency for various load capacitors. The power consumption is linearly proportional to the frequency within the adaptation range. The power consumption saturates at around 30 μW due to the maximum bias limit with a 100-pF load, but does not saturate with 10-pF and 1-pF loads because the required current is not large. The slopes of plots in Fig. 4(a) are also proportional to the load capacitance as Fig. 4(b) shows. The measured power consumption change per signal frequency and per load capacitance is approximately 0.0438 μW/kHz/pF.

As expected by Fig. 4(b), the measured power

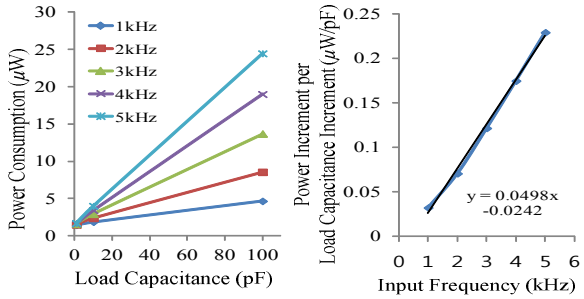


Fig. 5. Measured power consumption versus load capacitance [7] (a) and power consumption increment per load capacitance increment (b). The input signal was a 0.5 V_{pp} square wave.

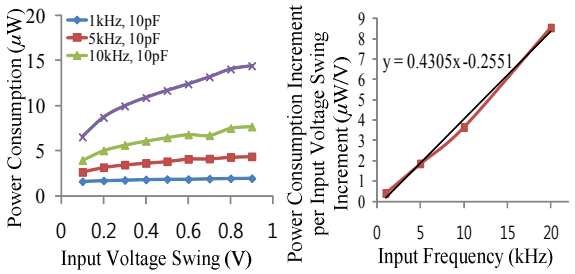


Fig. 6. Measured power consumption versus input voltage swing driving a 10-pF capacitor [7] (a) and power consumption increment per input frequency increment extracted within a linear region (b).

consumption is also linearly proportional to the load capacitance. Fig 5(a) shows this relationship more explicitly. Since larger load capacitors require larger driving currents, the linear relationship between power consumption and load capacitance implies that the bias current is adjusted well based on the needed driving current. The extracted slope of each plot in Fig. 5(a) is also linearly proportional to the frequency as Fig. 5(b) shows. The rate of power consumption increment per load capacitance increment and per signal frequency increment is 0.0498 μW/*k*Hz/pF which is similar to the value in Fig. 4(b).

Fig. 6(a) shows the measured power consumption versus the input voltage swing. The power consumption linearly increases as the voltage swing increases around 0.5 V. However, for a small swing, the power consumption does not fit in the linear curve because the bias voltage generator consumes significant power. Although not exactly linear, Fig. 6(a) shows that the power consumption is roughly proportional to the voltage swing within the preferred input range. The slope of each curve is also roughly proportional to the frequency as Fig. 6(b) shows.

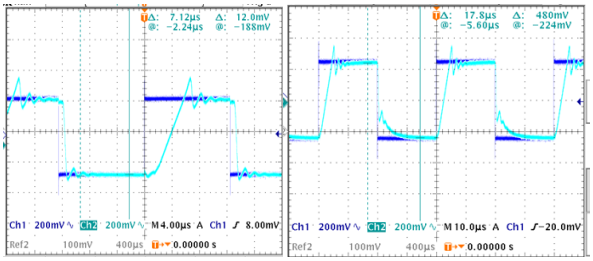


Fig. 7. Measured 0.5-V peak-to-peak square pulse input and output waveforms of the test voltage follower driving a 10-pF load at 40 kHz (a) and (b) a 100-pF load at 25 kHz [7].

Fig. 7 shows the measured input and output waveforms of the voltage follower driving a 10-pF capacitor at 40 kHz and a 100-pF capacitor at 25 kHz. To demonstrate the maximum speed, the operating frequency had been increased until the output hardly followed the input. The ringing in Fig. 7 might be the result of unexpected parasitic in the feedback path and the variation in the on-chip bias generator because the OTA did not have the ringing behavior in the simulation. Unlike conventional OTAs, the maximum frequency decreased only by 37.5% when the load capacitance increased by ten times. This implies that the bias current level is properly increased for higher speed as the load capacitance increased.

3. Adaptation to Sinusoidal Wave Inputs

The positive feedback bias controller can adapt not only to square pulses but also to sinusoids. To test the adaptation to sinusoids, various sinusoidal inputs are applied. The measured power consumption is also approximately proportional to the frequency, the load capacitance, and the signal swing showing dynamic adaptation to a sophisticated analog signal.

Fig. 8(a) shows the measured power consumption versus the signal frequency for a sinusoidal input. With 1-pF and 10-pF loads, the power consumption almost linearly increases as the frequency increases. The 100-pF plot is linear at low frequencies but saturates at high frequencies due to the maximum bias current limitation. The slope of the 10-pF curve is almost ten times as large as the one of the 1-pF curve, implying that the power consumption is proportional to the load capacitance too. However, the slope of the 100-pF curve is not exactly

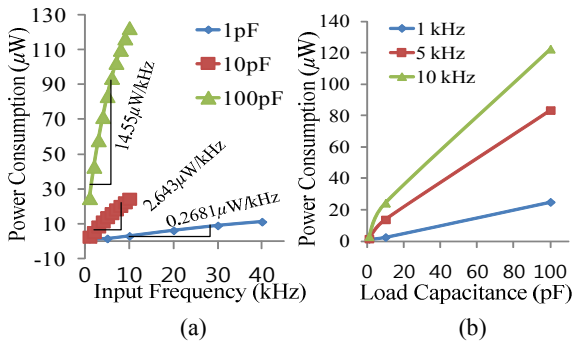


Fig. 8. Measured power consumption versus frequency (a) and load capacitance (b). A 0.5-V peak-to-peak sinusoidal waves with various frequency is fed to the voltage follower driving 1-pF, 10-pF, and 100-pF capacitors.

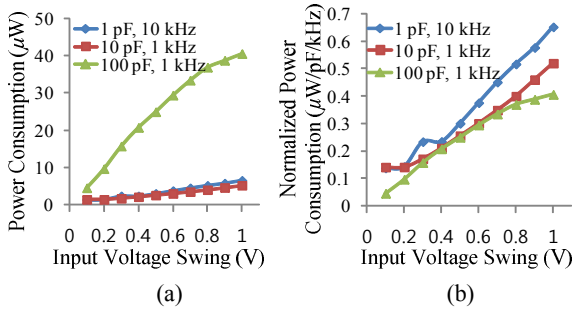


Fig. 9. Power consumption (a) and normalized power consumption (b) versus the voltage swing of a sinusoidal input. The voltage follower drove a 1-pF, 10-pF, and 100-pF capacitors at 10 kHz, 1 kHz, and 1 kHz, respectively.

proportional to the load capacitance due to the peak bias current limit.

The measured power consumption of the voltage follower increases with the load capacitance for sinusoidal inputs as well. Fig. 8(b) shows the measured power consumption versus the load capacitance. The power consumption increases as the load capacitance increases, but it is not exactly proportional to the load capacitance due to the maximum current limit.

The power consumption is linearly proportional to the input voltage swing too. Fig. 9(a) shows the measured power consumption versus the peak-to-peak voltage swing for sinusoidal inputs while the voltage follower drives 1-pF, 10-pF, and 100-pF capacitors at 10 kHz, 1 kHz, and 1 kHz, respectively. For 1-pF, and 10-pF loads, the power consumption is approximately linearly proportional to the voltage swing. With a 100-pF load, the power consumption is linear for small voltage swing and saturates for large voltage swing due to the maximum bias current limitation. Note that the 1-pF-and-10-kHz plot and the 10-pF-and-1-kHz plot are close each other in Fig. 9(a), indicating that the power consumption profile is proportional to the product of the load capacitance and the input frequency. Fig. 9(b) shows the power consumption normalized to the load capacitance and the operating frequency versus the voltage swing. The normalized power consumption curves are similar to each other. The slope of the 10-pF and 1-kHz curve is 0.4954 μW/pF/kHz/V.

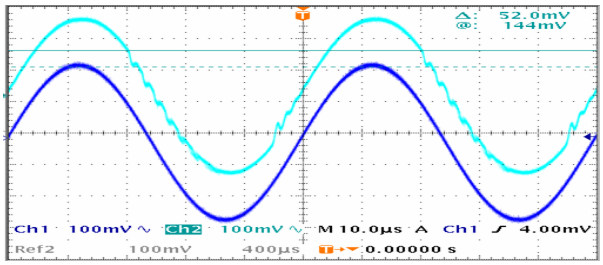


Fig. 10. Measured input and output waves of the voltage follower driving a 1-pF load capacitor. The input was a 0.5 V peak-to-peak 20-kHz sinusoid.

Fig. 10 shows the measured input and output waves of the voltage follower driving a 1-pF capacitor. The input was a 0.5 V peak-to-peak 20-kHz sinusoid. Similar to the previous experiment, the frequency had been increased until the output hardly tracked the input. The measured peak error is about 50 mV as Fig. 10 shows. Even though little ringing behavior is observed, the output closely tracked the input sinusoidal wave well, indicating that the voltage follower can work as an analog buffer for various sophisticated analog signals.

V. CONCLUSIONS

This paper reports a positive feedback bias control technique for OTAs configured with negative feedback. The bias current is adjusted based on monitoring of the OTA's output current forming a positive feedback loop that boosts the adaptation speed. The unstable behavior of the positive feedback is controlled by the outer negative feedback as well as the minimum and maximum bias current limitations. The basic concept of the reported technique is demonstrated by experiment using a test voltage follower circuit fabricated in 0.5-μm CMOS technology. The voltage follower could quickly adapt its power consumption roughly linearly proportional to the frequency, the load capacitance, and the signal swing for

both square and sinusoidal inputs. Therefore, the reported technique has potential to adaptively and quickly reduce the power consumption of various OTA applications handling various sophisticated analog signals.

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REFERENCES

[1] Mohammad Mahdi Ahmadi and Graham A. Jullien, "A Wireless-Implantable Microsystem for Continuous blood Glucose Monitoring," *IEEE Transaction on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 169-180, June 2009.

[2] Jae-Seung Lee, Jae-Yoon Sim, and Hong June Park, "A Design Guide of 3-stage CMOS Nested Gm-C Operational Amplifier with Area or Current Minimization," in *Proceedings of IEEE International SoC Design Conference*, Nov. 2008, pp. II-9-II-12.

[3] Jae-Seung Lee, June Hyun Bae, Ho-Young Kim, Ji-Yong Um, Jae-Yoon Sim, and Hong-June Park, "A Design Guide of 3-stage CMOS Operational Amplifier with Nested Gm-C Frequency Compensation," *IEIE Journal of Semiconductor Technology and Science*, vol. 7, no. 1, pp. 20-27, March 2007.

[4] Joyce Kwong and Anantha P. Chandrakasan, "An Energy-Efficient Biomedical Signal Processing Platform," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 7. pp.1742-1753, July 2011.

[5] Huikwan Yang, Sanhyun Cha, Seungyun Lee, Sangheon Lee, Jinup Lim, and Joongho Choi, "A 1.2-V Wide-Band SC Filter for Wireless Communication Transceivers," IEIE Journal of Semiconductor Technology and Science, vol. 6, no. 4, pp. 286-291, Dec. 2006.

[6] Won-Chul Song et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," IEEE J. of Solid-State Circuits, vol. 30, no. 5, pp. 514-521, May 1995.

[7] S. Baswa et al., "Low-voltage power-efficient adaptive biasing for CMOS amplifiers and buffers," IEE Electronic Letters, vol. 40, no. 4, Feb., 2004.

[8] Juan A. Galan, et al., "Super Class-AB OTAs With Adaptive Biasing and Dynamic Output Current Scaling," IEEE Transaction on Circuits and Systems-I: Regular Papers, vol. 54, no. 3, Mar., 2007.

[9] Jesus Aguado-Ruiz et al., "Power Efficient Class AB OP-Amps With High and Symmetrical Slew Rate," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. PP, no. 99, pp. 1-6, June, 2013.

[10] Byungsub Kim et al., "Power-Adaptive Operational Amplifier with Positive-Feedback Self Biasing," in Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS), 2006, pp.4883-4886.

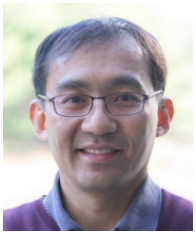
[11] Kwang S. Yoon, "A CMOS Digitally Programmable Slew-Rate Operational Amplifier," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 42, no. 11, Nov, 1995.

[12] H. Wakaumi, "A Three-Stage CMOS OP amplifier with a dynamic switching bias circuit," International Conference on Control, Automation, and Systems, 2012.

[13] Rahul Sarpeshkar, Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems. New York: Cambridge University Press, 2010.

Byungsub Kim received the B.S. degree in Electronic and Electrical Engineering (EEE) from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2000, and the M.S. (2004) and Ph.D. (2010) degrees in Electrical Engineering and Computer Science (EECS) from Massa-

chusetts Institute of Technology (MIT), Cambridge, USA. From 2010 to 2011, he worked as an analog design engineer at Intel Corporation, Hillsboro, OR, USA. In 2012, he joined the faculty of the department of Electronic and Electrical Engineering at POSTECH, where he is currently working as an assistant professor. He received several honorable awards. In 2011, Dr. Kim received MIT EECS Jin-Au Kong Outstanding Doctoral Thesis Honorable Mentions, and IEEE 2009 Journal of Solid-State Circuits Best Paper Award. In 2009, he received Analog Device Inc. Outstanding Student Designer Award from MIT, and was also a co-recipient of the Beatrice Winner Award for Editorial Excellence at the 2009 IEEE Internal Solid-State Circuits Conference.



Jae-Yoon Sim received the B.S., M.S., and Ph.D. degrees in Electronic and Electrical Engineering from Pohang University of Science and Technology (POSTECH), Korea, in 1993, 1995, and 1999, respectively. From 1999 to 2005, he worked as a senior engineer at Samsung Electronics, Korea. From 2003 to 2005, he was a post-doctoral researcher with the University of Southern California, Los Angeles. From 2011 to 2012, he was a visiting scholar with the University of Michigan, Ann Arbor. In 2005, he joined POSTECH, where he is currently an Associate Professor. He has served in the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC), Symposium on VLSI Circuits, and Asian Solid-State Circuits Conference. He is a co-recipient of the Takuo Sugano Award at ISSCC 2001. His research interests include high-speed serial/parallel links, PLLs, data converters and power module for plasma generation.

Hong-June Park received the B.S. degree from the Department of Electronic Engineering, Seoul National University, Seoul, Korea, in 1979, the M.S. degree from the Korea Advanced Institute of Science and Technology, Taejon, in 1981, and the Ph.D. degree from the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, in 1989. He was a CAD engineer with ETRI, Korea, from 1981 to 1984 and a Senior Engineer in the TCAD Department of INTEL from 1989 to 1991. In 1991, he joined the Faculty of Electronic and Electrical Engineering, Pohang University of Science and Technology (POSTECH), Gyeongbuk, Korea, where he is currently Professor. His research interests include CMOS analog circuit design such as high-speed interface circuits, ROIC of touch sensors and analog/digital beamformer circuits for ultrasound medical imaging. Prof. Park is a senior member of IEEE and a member of IEEK. He served as the Editor-in-Chief of Journal of Semiconductor Technology and Science, an SCIE journal (http://www.jsts.org) from 2009 to 2012, also as the Vice President of IEEK in 2012 and as the technical program committee member of ISSCC, SOVC and A-SSCC for several years.