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Microfabrication of Vertical Carbon Nanotube Field-Effect Transistors on an Anodized Aluminum Oxide Template Using Atomic Layer Deposition

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Abstract – This paper presents vertical carbon nanotube (CNT) field effect transistors (FETs). For the first time, the author successfully fabricated vertical CNT-based FETs on an anodized aluminum oxide (AAO) template by using atomic layer deposition (ALD). Single walled CNTs were vertically grown and aligned with the vertical pores of an AAO template. By using ALD, a gate oxide material (Al_2O_3) and a gate metal (Au) were centrally located inside each pore, allowing the vertical CNTs grown in the pores to be individually gated. Characterizations of the gated/vertical CNTs were carried and the successful gate integration with the CNTs was confirmed.

Keywords: Anodized aluminum oxide (AAO), Atomic layer deposition (ALD), Carbon nanotube (CNT), Field effect transistor (FET)

1. Introduction

Various configurations of semiconducting single-walled carbon nanotube field effect transistors (CNT FET) have been explored since the first CNT FETs was introduced [1-3]. In most of the CNT FETs reported in the literature, the CNTs were horizontally engaged as they allow easy integration with a gate metal, but the area densities of the CNTs with the horizontal configurations are significantly limited as the horizontal arrangement requires spacing to allow the gate metal to be placed between connecting electrodes. As an alternative, the vertical arrangement of CNTs has been suggested, which is potentially able to greatly increase the areal density of the CNTs. However, since vertical growth of CNTs and integration of the gates with the vertical CNTs are challenging, only limited works on fabrication of vertical CNT-based devices have been reported. Recently, gated/vertical CNTs were fabricated on an anodized aluminum oxide (AAO) template where CNTs were vertically oriented inside the pores, but no successful I-V characterizations of the fabricated CNT devices for verification was demonstrated [4]. To the best knowledge of the author, no successful demonstration of fabrication of the vertical CNT-based FETs has been reported.

The present author proposes to fabricate a vertical CNT-based FET on an AAO template by using atomic layer deposition (ALD), which is known to be used for conformal deposition. Using ALD was intended to achieve direct deposition of the gate oxide and the gate metal to gate CNTs which are vertically oriented inside the vertical pores of the AAO template. The gate oxide and the gate metal are centrally placed in the pores by the conformal deposition enabled by ALD, individually gating the vertical CNTs as shown in Fig. 1.

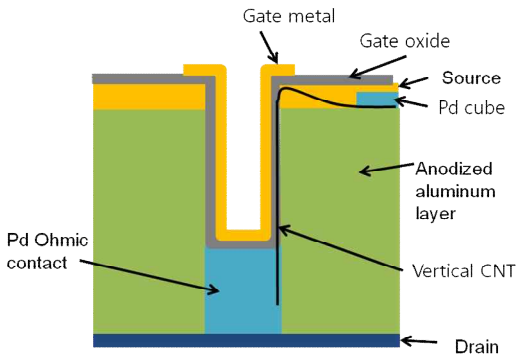

Fig. 1. Conceptual configuration of the AAO-based vertical CNT FET. The gate metal and the gate oxide are conformally deposited inside the pore byatomic layer deposition.

In this paper, the fabrication details engaging ALD for the deposition of the gate metal and gate oxide inside the pores of the AAO template are presented. In the end, the transfer characteristics of the gated vertical CNTs are illustrated and highlighted. Further challenges with the fabrication are also addressed.

2. Device Fabrication

The device fabrication mainly consists of anodization of an aluminum layer, CNT catalyst deposition, CNT synthesis, and ALD deposition of the gate oxide and the gate metal. The fabrication process flow is illustrated in Figs. 2 and 3.

The AAO template with the vertical pores and the

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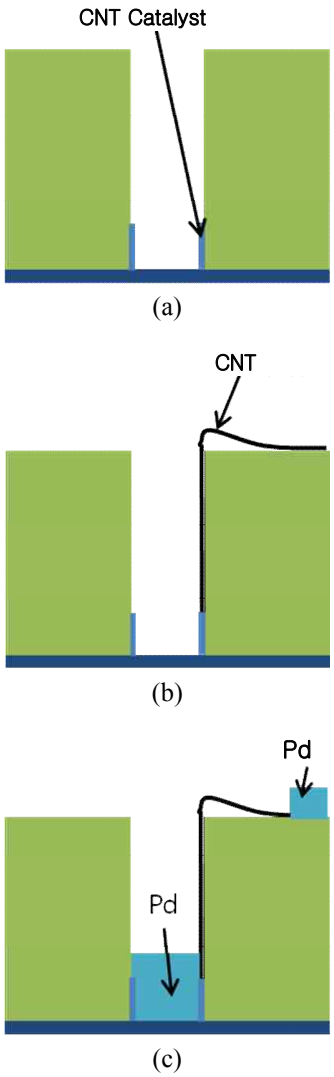


Fig. 2. Vertical growth of CNT: (a) Catalyst isolation at the bottom of the vertical pores using redeposition of the catalyst by ion milling [5]; (b) CNT vertical growth. CNTs were adherent to the sidewall due to van der Waals force; (c) Pd electrodeposition to establish Ohmic contacts with semiconducting CNTs with electrodes. Pd cluster appearing at the top surface confirmed that electrodeposited Pd contacted the bottom ends of the vertical CNTs.

thickness of 1 μm was fabricated using anodization. 20 nm of Mo, 50 nm of Ti and 3 μm of Al were deposited on a silicon substrate in series using thermal evaporation. Mo will be used as a drain electrode and Ti was added to promote adhesion between the layers of Al and Mo. Here, Al was not fully anodized in one single step, but instead it was anodized with three separate steps combined with chemical etch of the anodized aluminum, which was conducted after each separate anodization step, in order to improve regularity of the produced vertical pores in spacing and size. The resulting thickness of the AAO template after the three runs of anodization (combined with the chemical etch) was ~ 1μm. After anodization was completed, the vertical pores of AAO were further widened by using phosphoric acid. The resulting opening diameters of the pores after the pore widening process were ~ 100 nm making the aspect ratio of the pore depth to the pore diameter 1:10. The further details of anodization for the AAO template was provided elsewhere [5]. The AAO template was then pre-annealed at 820 ^{o}C to remain structurally stable during the CNT synthesis to be later conducted [5].

The CNT iron catalyst was introduced and isolated at the bottom of the pores by combining an angled evaporation of the catalyst and ion-milling-based re-deposition (Fig. 2 (a)). 5nm of iron catalyst was first deposited in the exposed area by an angled thermal evaporation (which is in the thickness range to allow for growth of single-walled CNTs) and then angled ion milling was carried to sputter the deposited iron catalyst on the sidewalls of the pores and re-deposit it at the bottom of the pores, which, in turn, achieved isolation of catalyst located at the bottom of the pores. The isolated CNT catalyst placed at the bottom of the pores was to allow for vertical growth of CNTs crossing from bottom to top of the template as shown in Fig. 2 (b). Technical details on the catalyst deposition and bottom-placed isolation were provided in [5]. The CNT synthesis was carried at 820 ^{o}C and the pressure of 10^5 Pa with reacting chemical gases containing 20 ccm of C_2H_4, 1000 ccm of CH_4, and 500 ccm of H_2 which were carried by argon into the chamber. The synthesis was conducted for 3 minutes and then the supplies of reacting gases were turned off and the chamber was set to be cooled. The CNTs vertically grown on the template was treated with O_2 plasma in order to selectively remove metallic CNTs against semiconducting CNTs [6].

The templates with the CNTs grown were then patterned to separate active CNT zones for separate device characterizations which were to be carried later. The active CNT zones was separated as the CNTs in the exposed regions were deactivated by the O_2 plasma while the CNTs in the regions covered with a patterned photoresist were protected and remained active. The photoresist for the patterning was a double stacked layer of Polymethyl Methacrylate (PMMA) and AZ5214R. PMMA with the thickness of 700 nm was used as the bottom layer directly contacting the CNTs since PMMA can be easily stripped off from CNTs, while AZ4215 with the thickness of 1400 nm was used as the upper layer to be consumed to protect the CNTs underneath the layer during the O_2 plasma process. The photoresist was exposed with a photomask patterned for separate active CNT zones, and developed. The O_2 plasma treatment was set at the pressure of 300 mTorr and carried for 10 minutes. After deactivation, only the CNTs placed in the active CNT zones that were protected by the photoresist layer remained active to serve as the vertical pathway. Electrodeposition of Pd on the CNTs followed to coat the ends of the remaining/active

CNTs with Pd to form Ohmic contacts between the semiconducting CNTs and the metal electrodes [7, 8] (Fig. 2 (c)). The electrodeposition was carried at a current density of 50 mA/cm^2 for 10 ms in a solution containing $Pd(NH3)_4Cl_2$-NH_4Cl. After electrodeposition, Pd cluster appeared in cubic forms at the top surface of the AAO template, confirming that the electrodeposited Pd contacted the CNTs at the bottom of the pores, making the vertical conductive ways. Then, layers of 5 nm of Ti and 250 nm of Au were deposited by an angled evaporation and integrated with the vertical CNTs as the source electrode (Fig. 3 (a)).

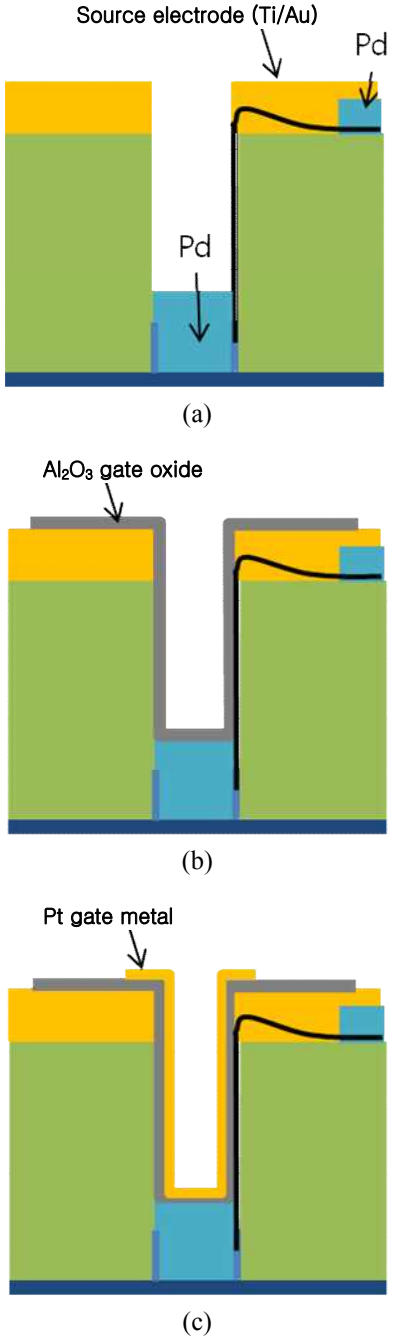


Fig. 3. Integration of source and gate electrodes: (a) Angled thermal evaporation of source electrode; (b) Substrate assisted growth-based atomic layer deposition of the gate oxide Al_2O_3 on the vertical CNTs supported on the sidewall of the pores; (c) Atomic layer deposition of the gate metal Pt.

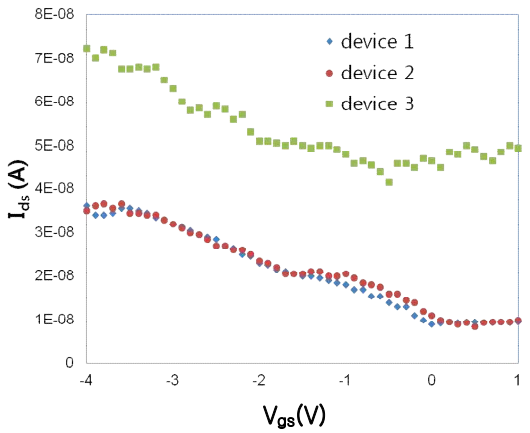
After the CNT pathways vertically crossing the template thickness were established as described above, the vertical CNTs were individually gated by using ALD. For electrical insulation of the CNTs from the gate electrode, there can be suggested two methods of ALD: the direct ALD deposition of the dielectric material on the surface of CNTs (designed especially for suspended CNTs) [9, 10] and the substrate-assisted growth-based ALD where the dielectric material is deposited and grown on a supporting substrate to cover the CNTs supported on (and in contact with) the substrate [3]. Since the present CNTs grown inside the pores (especially nanometer-wide single walled CNTs) are generally in contact with the sidewall of the vertical pores due to van der Waals force rather than standing free, the substrate-assisted growth-based ALD is found more suitable for the present case than the direct deposition. In addition, the substrate-assisted growth-based ALD of Al_2O_3 is more reliable than the direct deposition of Al_2O_3 on the CNTs as the former can be carried without surface functionalziation which can degrade the unique electrical properties of the CNTs. Thereby, the substrate-assisted growth-based ALD (Fig. 3 (b)) was chosen here for the CNT insulation. The substrate assisted growth-based ALD of Al_2O_3 was conducted at 300 ^oC with trimethylaluminum (TMA) and H_2O. The pulse time for each of TMA and H_2O was set to 15 m sec. The purge was carried with N_2 for 20 sec to prevent direct contact between the gases of TMA and H_2O. The thickness of the Al_2O_3 layer that covers the vertical CNTs was estimated to be ~ 20 nm. It should be also noted that parts of the CNTs that lied outside the pores could be unattached (meaning that they are suspended) and, therefore, likely remained un-insulated even after the substrate-assisted growth-based ALD of the oxide, which, in turn, may cause electrical shorts between the gate and the CNTs. Thus, in order to eliminate the possibility of introducing the electrical short in the fabrication, the O_2 plasma treatment was conducted here at 300 mTorr for 10 minutes, removing any unattached/un-insulated parts of the CNTs. After the O_2 plasma treatment, Pt was deposited by ALD on the deposited Al_2O_3 layer, making the gate electrode for the vertical CNTs (Fig. 3(c)). ALD of Pt was carried at 300 ^oC with trimethylplatinum (TMP) and H_2O. The pulse time for each of TMP and H_2O was set to 15 ms. The purge using N_2 was carried for 20 sec.

3. Results

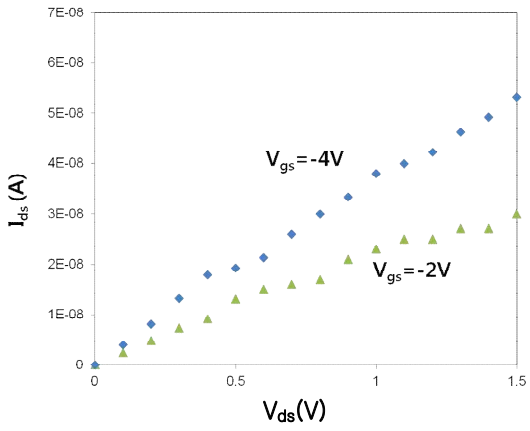
Fig. 4 shows the transfer characteristics of the gated / vertical CNTs. Fig. 5 conceptually presents the band diagrams of the gated CNT illustrating that, for the negative gate voltage, the electrical pathways engaging

the p-type semiconducting single-walled CNTs were in the "ON" state while for the positive gate voltage the pathways were in the "OFF" state. The gate voltage V_{gs} was swept from -4 V to 1 V while the source to drain bias was set to 1V. As shown in Fig. 4 (a), the on-off ratios of the current achieved from the gated/vertical CNTs were in the range between 1.5 and 5. The rather limited on-off ratios suggested that metallic CNTs were not fully removed from the template even after the selective etching aiming to remove metallic CNTs [6] was conducted. Nevertheless, the present fabrication engaging central placement of the gate metal in the pores based on ALD clearly demonstrated that the vertical single walled CNTs inside the pores were individually gated. Fig. 4 (b) shows the drain current, I_{ds}, against the drain voltage, V_{ds}. Based on the square law model for MOSFET, the correlation between the drain current and the drain voltage is fitted on the equation of

$$I_{ds} = CV_{ds}\left(2V_{gs} - V_{ds}\right) + V_{ds} / R_{metal} \quad (1)$$



(a)



(b)

Fig. 4. Transfer characteristics of the CNT FETs integrating the gated/vertical CNTs: (a) I_{ds} Vs. $V_{gs,}$. The source-to-drain bias was set to 1V; (b) I_{ds} Vs. V_{ds} for device 1 of (a).

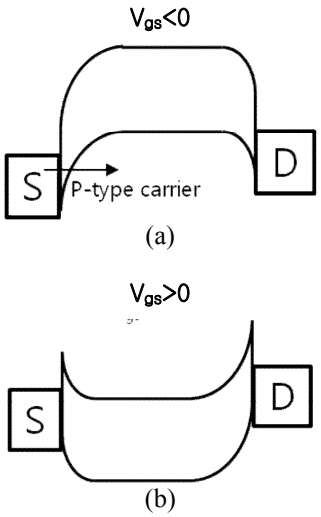


Fig. 5. Band diagrams of gated p-type CNT: (a) "ON" state. $V_{gs} < 0$; (b) "OFF" state . $V_{gs} > 0$.

where C is~ 3.8×10^{-9} (A/V^2) and R_{metal}, the collective metallic CNTs' resistance of the vertical path is ~ 10MΩ. It should be noted that V_{ds} / R_{metal} is added in Eq. (1) for the proper fitting as a few metallic CNTs remained in the vertical path, playing a part in the conductance. R_{metal} was achieved with V_{gs} set to 0 V.

The current densities of the fabricated devices appeared rather low, suggesting that the contact resistance of CNTs with the electrodes remained very high. Therefore, further optimization for the present fabrication process needs to be carried to improve the device performance.

4. Conclusion

Individually gated / vertical CNTs grown inside the vertical pores of an AAO template were successfully achieved. ALD was involved to achieve conformal deposition of the gate oxide and the gate metal inside the high-aspect ratio vertical pores where deposition uniformity using other existing deposition methods is significantly limited. The present ALD process for the deposition of the gate oxide was carried based on the substrate-assisted growth, where the deposition material is grown from the supporting substrate to cover the CNTs, since the vertical CNTs inside the vertical pores were in contact with the sidewalls of the pores. The on-off ratios of the fabricated CNT FETs integrating the gated vertical CNTs were in the range between 1.5 and 5. The rather limited on-off ratios suggested that metallic CNTs remained in the vertical path degrading the device performance. Thus, the present selective killing technique to remove the metallic tubes needs to be improved. In future, further optimization remains to be carried to improve the on-off ratios and the current density of the vertical CNT FETs.

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