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Electrical Characteristics of Enhancement-Mode n-Channel Vertical GaN MOSFETs and the Effects of Sidewall Slope

Sung Yoon Kim*, Jae Hwa Seo*, Young Jun Yoon*, Jin Su Kim*, Seongjae Cho, Jung-Hee Lee* and In Man Kang†**

Abstract – Gallium nitride (GaN) is a promising material for next-generation high-power applications due to its wide bandgap, high breakdown field, high electron mobility, and good thermal conductivity. From a structure point of view, the vertical device is more suitable to high-power applications than planar devices because of its area effectiveness. However, it is challenging to obtain a completely upright vertical structure due to inevitable sidewall slope in anisotropic etching of GaN. In this letter, we design and analyze the enhancement-mode n-channel vertical GaN MOSFET with variation of sidewall gate angle by two-dimensional (2D) technology computer-aided design (TCAD) simulations. As the sidewall slope gets closer to right angle, the device performances are improved since a gradual slope provides a leakage current path through the bulk region.

Keywords: Gallium nitride (GaN), Power device, Enhancement mode, Vertical channel, TCAD

1. Introduction

The wide bandgap, high electron mobility, high critical electric field, and good thermal conductivity of gallium nitride (GaN) make GaN useful for high-power and high-temperature applications [1-6]. In recent studies, most of attention has been drawn to either silicon carbide (SiC) power metal-oxide-semiconductor field-effect transistors (MOSFETs) or high electron mobility transistors (HEMTs) [7-12]. However, the continuous developments of SiC MOSFETs and GaN HEMTs have been hindered by their own limits. SiC MOSFET has weaknesses that it is hard to form high-quality oxide/SiC interface and its channel mobility and device reliability are relatively low [13, 14]. Although the GaN HEMT has high two-dimensional electron gas (2-DEG) density and high mobility, it suffers from current collapse which is mainly due to the electric field induced from the AlGaN surface under the gate and large gate leakage current which is owing to the absence of gate insulator [15]. It also operates at normally-on mode due to the existence of 2-DEG populated below fermi level under equilibrium condition at zero bias. The GaN MOSFET can be also operated at a normally-off mode with much lower gate leakage current under certain design conditions while its high electron mobility and density can be somehow sacrificed. Although SiC MOSFET has been a dominant power device, GaN MOSFET has superiority in terms of high-quality GaN channel-gate insulator interface, high mobility, and blocking voltage [5, 14]. Vertical channel provides advantages of high current density per unit area and scalability of gate length. Also, it helps achieving simpler and less destructive processing (less damage) getting rid of either ion implantation process or electron-beam irradiation in device fabrication than lateral channel, since a vertical GaN device is usually fabricated by epitaxial growths [16-18]. In addition, the cylindrical-shaped structure brings higher gate controllability and enhanced current drivability [19-22]. However, fabrication of a complete vertical structure can be challenging due to the etching process for sidewall formation that substantially controls the device performances. For this reason, the sidewall gate slope can be regarded as one of the design variables.

In this work, the effects of sidewall gate slope and the electrical characteristics of enhancement-mode n-channel vertical GaN MOSFET are closely investigated. The device was designed by a two-dimensional (2D) technology computer-aided design (TCAD) simulations [23]. Maximum drain current (I_{max}), on-state resistance (R_{on}), threshold voltage (V_{th}), subthreshold swing (S), transconductance (g_m), and breakdown voltage (V_B) are examined.

2. Simulation Results and Discussions

2.1 Device structure

Figs. 1(a)-(b) present the three-dimensional schematic view and the cross-sectional view of the simulated GaN MOSFET with an indication of the current path. The high-κ gate oxide material is Al_2O_3 and its equivalent oxide thickness (EOT) is 30 nm. The gate workfunction is 5.2 eV.

† Corresponding Author: School of Electronics Engineering, Kyungpook National University, Korea. (imkang@ee.knu.ac.kr)
* School of Electronics Engineering, Kyungpook National University, Korea. (4bass@knu.ac.kr)
** Department of Electronics Engineering, Gachon University, Korea. (felixcho@gachon.ac.kr)
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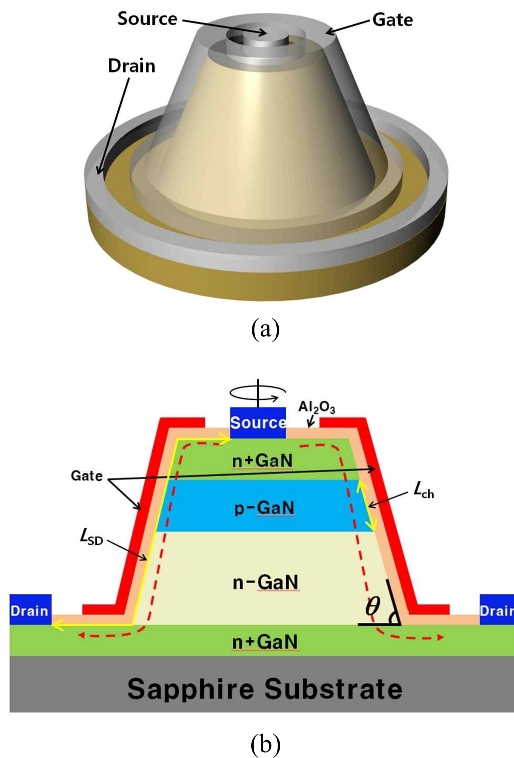

Fig. 1. (a) Three-dimensional schematic view and (b) Cross-sectional view of the simulated enhancement-mode n-channel vertical GaN MOSFET.

The GaN layers consist of 0.5-μm n^+ GaN for drain junction, 1-μm n^- GaN for the drift region, 0.3-μm p^- GaN for channel, and 0.5-μm n^+ GaN for source junction. The doping concentrations of these GaN layers are 1×10^{18} cm^{-3}, 1×10^{16} cm^{-3}, 1×10^{17} cm^{-3}, and 1×10^{18} cm^{-3}, in sequence. The sidewall gate angle is defined as the acute angle between the substrate and the sidewall, as indicated at the right-side bottom of the gate in Fig. 1(b). The p-GaN channel lengths (L_{ch}) are 1.15 μm, 0.51 μm, 0.34 μm, and 0.3 μm at sidewall angles (θ) of 15°, 36°, 60°, 90°, respectively. Also, at these angles, the source-to-drain lengths (L_{SD}) are 23.2 μm, 19.4 μm, 18.4 μm, and 18.1 μm, in sequence.

For higher accuracy and quality in simulation work, we have been included the k.p band parameter model for wurtzite structure of GaN in order to calculate the effective masses and band edge energies. We also added the specific electric field-dependent mobility models for GaN and the direct recombination model accounting for high level injection effects. The Fowler-Nordheim tunneling model has been included for the analysis of electron tunneling phenomenon into conduction band of the gate dielectric when the electric field across the gate dielectric is adequately high. In addition to this, the Shockley-Read-Hall (SRH) recombination model, the Selberherr's impact ionization model for the off-state breakdown characteristic, and other material-related parameters for GaN have been included [23].

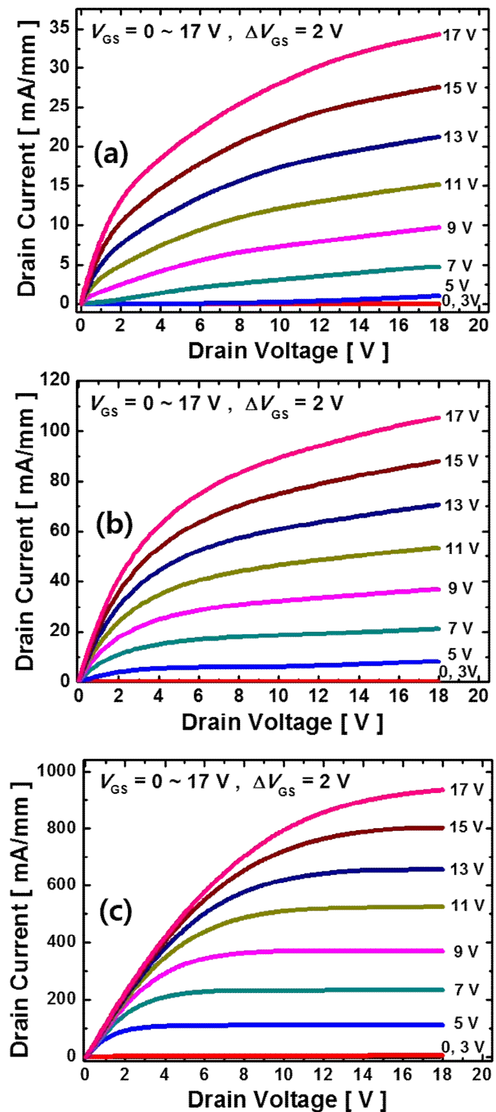

Fig. 2. Output characteristics of n-channel vertical GaN MOSFET with the sidewall angles of (a) 15°, (b) 36°, and (c) 90°.

2.2 Results and discussions

With above-mentioned structure, its device characteristics are investigated at different sidewall angles. Figs. 2(a)-(c) show the output characteristics of the simulated n-channel vertical GaN MOSFET as the sidewall angle varies. As the sidewall angle increases, I_{max} increases owing to reduction of channel resistance and R_{on}, accordingly: a larger sidewall angle shortens the channel length and drift region. In the same manner, I_{max} decreases and R_{on} increases as the sidewall angle gets smaller.

Fig. 3(a) depicts R_{on} and I_{max} as a function of sidewall angle, where R_{on} and I_{max} show monotonic decrease and increase, respectively, as could be inferred by Figs. 2(a)-(c). I_{max} values were 34.3 mA/mm, 105.5 mA/mm, and 934.0 mA/mm, respectively, when the sidewall angles were 15°, 36°, and 90°. Also, at these angles, R_{on}'s were 36.7 mΩ·cm^2,

9.7 mΩ·cm^2, and 1.6 mΩ·cm^2, in sequence. In practice, GaN layer has wurtzite crystal structure. After the mesa etching process, GaN layer has the sidewall slope and the dislocations such as defects or traps may occur due to the anisotropic effect. Owing to these defects of traps in the surface of sidewall, the electron mobility and the drain current are expected to decrease due to the current collapse [24, 25]. In this paper, however, the influence of channel length modulation is investigated in priority because the change of the L_{ch} and L_{SD} by sidewall slope is more dominant. Fig. 3(b) shows the method of extracting R_{on} of a device of which sidewall angle is 36°. The above simulation results show that larger sidewall angle warrants better R_{on} and I_{max} at the same time.

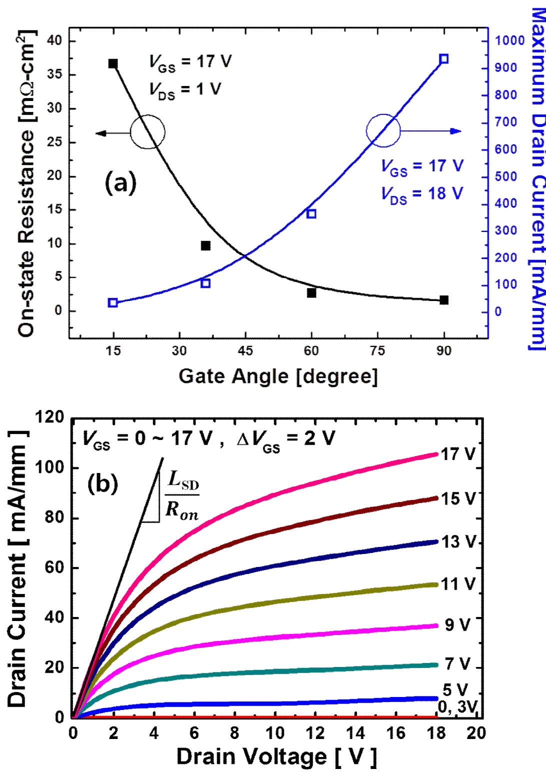

Fig. 3. Sidewall angle-dependent direct-current (DC) performances. (a) R_{on} and I_{max} as a function of sidewall angle. (b) Extraction of R_{on} (sidewall angle = 36°).

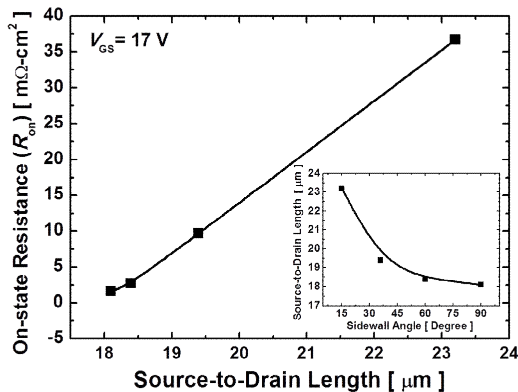

Fig. 4. R_{on} as a function of source-to-drain length (L_{SD}). The inset shows the L_{SD} with different sidewall angles.

Fig. 4 shows the change of R_{on} as a function of L_{SD} and the change of L_{SD} with different sidewall angles is displayed in inset of figure. As the sidewall angle varies, the L_{SD} also varies with the variation of L_{ch}. As shown in Fig. 4, the R_{on} is directly proportional to the L_{SD}. In other words, there is a linear relationship between R_{on} and L_{SD} because the distance between the source and drain behaves like a resistor towards electrons.

Figs. 5(a)-(c) demonstrate the I_D-V_{GS} transfer curves and transconductances (g_m) at different sidewall angles. V_{th} was extracted based on the constant current method (at the gate voltage for which I_{DS}= 10^{-1} mA/mm). V_{DS} was kept constant at 10 V during the V_{GS} sweep. V_{th}'s were 4.9 V, 3.5 V, and 2.9 V at sidewall angles of 15°, 36°, and 90°,

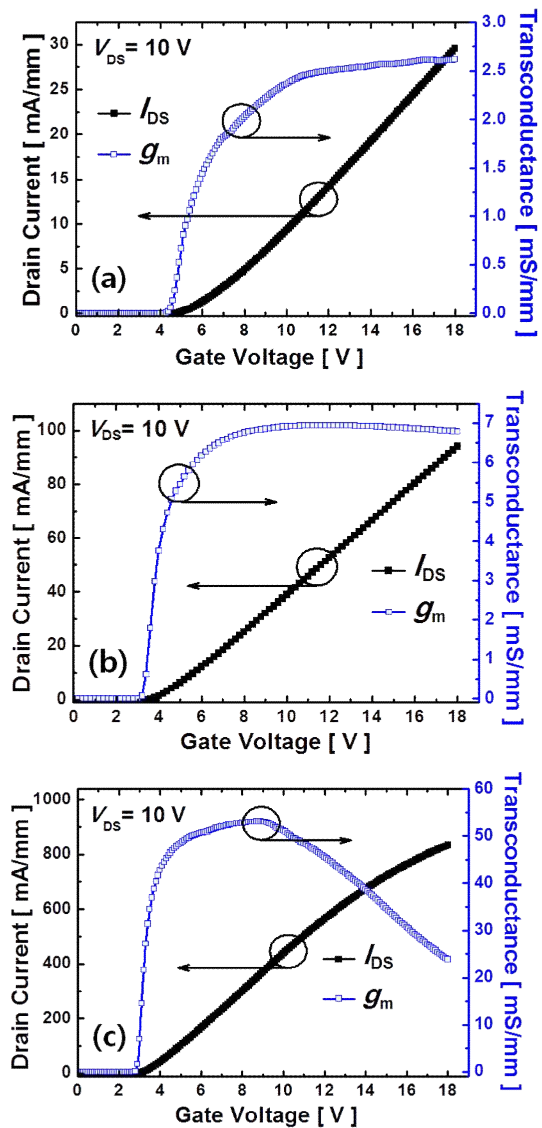

Fig. 5. I_D-V_{GS} characteristics of the simulated n-channel vertical GaN MOSFET with sidewall angles of (a) 15°, (b) 36°, and (c) 90° at V_{DS} = 10 V.

respectively, where the lowering at higher angles was due to the reduction of physical channel length. Peak transconductance was 2.6 mS/mm at a sidewall angle of 15°, 6.9 mS/mm at 36°, and 53.2 mS/mm at 90°. Again, these results support that larger sidewall angle ensures better DC performances along with the parameters in the previous part.

Fig. 6 demonstrates the I_D-V_{GS} curves at different sidewall angles (V_{DS} = 10 V for V_{GS} sweep). It is shown that the off-state currents (I_{off}'s) of the devices are below nA level, which indicates that the devices are in the complete pinch-off states. The current ratios (I_{on}/I_{off}) are 1.8×10^{11} at a sidewall angle of 15°, 1.6×10^{12} at 36°, and 4.5×10^{13} at 90°. Further, S values were 157.1 mV/dec, 119.3 mV/dec, and 87.6 mV/dec at 15°, 36°, and 90°, respectively. These results also stem from the effect of physical channel length modulated by controlling the sidewall angle. The increase of the sidewall angle results in shortening the channel length alongside increasing the threshold voltage. Therefore, on-state current increases drastically. The on-state currents vary depending on the sidewall angles, whereas the off-state currents are kept similarly. For this reason, S is also influenced by the sidewall angles.

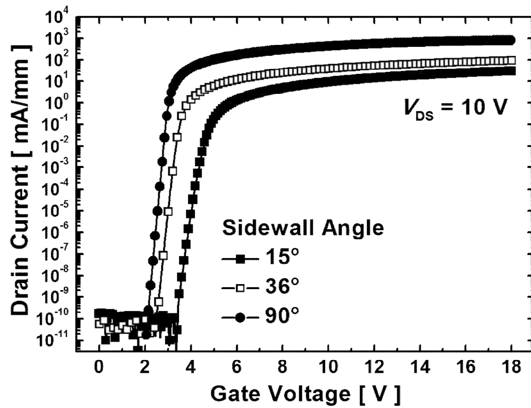

Fig. 6. I_D-V_{GS} transfer curve (logarithmic scale) at different sidewall angles at V_{DS} = 10 V.

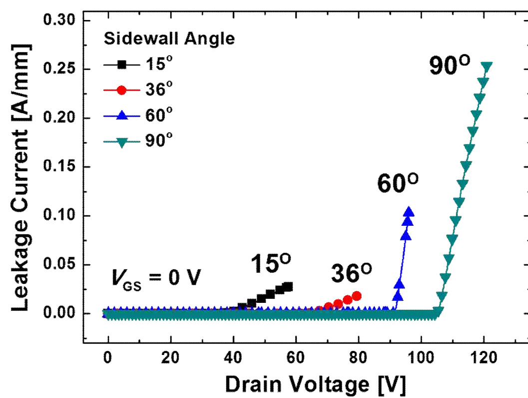

Fig. 7. Off-state breakdown characteristics at different sidewall angles at V_{GS} = 0 V.

Fig. 7 shows the off-state breakdown characteristics at different sidewall angles at V_{GS} = 0 V, where it is found that breakdown voltage (V_B) increases as the sidewall angle gets larger. V_B's were 37 V at a sidewall angle of 15°, 65 V at 36°, 91 V at 60°, and 106 V at 90°. Thin region of GaN layer gets wider as the sidewall angle gets smaller and the leakage current flows through the this region. For this reason, when the sidewall angle is relatively small, the

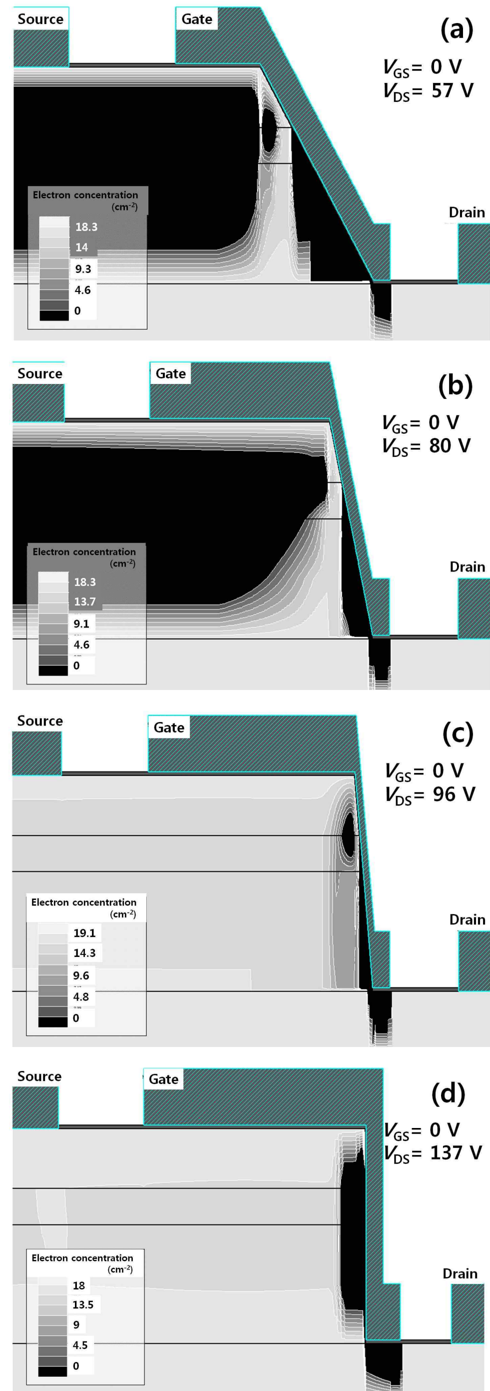

Fig. 8. Electron concentrations which indicate breakdown leakage currents with the sidewall angles of (a) 15°, (b) 36°, (c) 60°, and (d) 90°.

leakage current tends to flow through the bulk region of GaN layer more probably. On the contrary, the leakage current conducts not through the bulk region of GaN layer but through the gate electrode as the sidewall angle is relatively large. This gate leakage current results from high electric field at the drain-side gate edge.

Figs. 8(a) - (d) indicate the electron concentrations after the occurrence of breakdown leakage currents and each biases are displayed in inset of figures. With the aforementioned off-state breakdown characteristics, introduction of a proper passivation layer such as either AlN thin film [26, 27] or field plate [28, 29] enhances the robustness against the breakdown.

3. Conclusion

In this work, we investigated the effects of sidewall angles on electrical characteristics of enhancement-mode n-channel vertical GaN MOSFET in terms of I_{max}, R_{on}, V_{th}, S, and V_B. As the result, larger sidewall angle improves the overall device performances. Therefore, it would be critical to construct the sidewall gates with right angles as much as the anisotropic dry etching permits, for both device performances and area-effectiveness. One drawback that sharp slope might bring is the breakdown characteristics but it would overcome by appropriate passivation techniques relieving the electric field at the gate edge.

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References

[1] B. Gelmont, K. Kim, and M. Shur, "Monte Carlo simulation of electron transport in gallium nitride," *J. Appl. Phys.*, vol. 74, no. 3, pp. 1818-1820, Aug. 1993.

[2] H. Yu, L. McCarthy, S. Rajan, S. Keller, S. Denbaars, J. Speck, and U. Mishra, "Ion implanted AlGaN-GaN HEMTs with nonalloyed ohmic contacts," *IEEE Electron Device Lett.*, vol. 26, no. 5, pp. 283-285, May 2005.

[3] M. Micovic, N. X. Nguyen, P. Janke, W.-S. Wong, P. Hashimoto, L.-M. McCray, and C. Nguyen, "GaN/AlGaN high electron mobility transistors with f_T of 110 GHz," *IEEE Electronics Lett.*, vol. 36, no. 4, pp. 358-359, Feb. 2000.

[4] U. K. Mishra, L. Shen, T. E. Kazior, and Y.-F. Wu, "GaN-Based RF power devices and amplifiers" *Proc. IEEE*, vol. 96, no. 2, pp.287-305, Feb. 2008.

[5] W. Huang, T. Khan, and T. P. Chow, "Enhancement-Mode n-Channel GaN MOSFETs on p and n-GaN/Sapphire Substrates," *Proc. of the 18th International Symposium on Power Semiconductor Devices & IC's*, Jun. 2006.

[6] M. S. P. Reddy, M.-K. Kwon, H.-S. Kang, D.-S. Kim, J.-H. Lee, V. R. Reddy, and J.-S. Jang, "Influence of Series Resistance and Interface State Density on Electrical Characteristics on Ru/Ni/n-GaN Schottky Structure," *J. Semicond. Technol. Sci.*, vol. 13, no. 5, pp. 492-498, Oct. 2013.

[7] M.-S. Kang, W. Bahng, N.-K. Kim, J.-G. Ha, J.-H. Koh, and S.-M. Koo, "Impact of Interface Charges on the Transient Characteristics of 4H-SiC DMOSFETs," *J. Electr. Eng. Technol.*, vol. 7, no. 2, pp. 236-239, Mar. 2012.

[8] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O.W. Holland, M.K. Das, and J.W. Palmour, "Improved Inversion Channel Mobility for 4H-SiC MOSFETs Following High Temperature Anneals in Nitric Oxide," *IEEE Electron Device Lett.*, vol. 22, no. 4, pp. 176-178, Apr. 2001.

[9] Guoen Cao, and Hee-Jun Kim, "A Novel Circuit for Characteristics Measurement of SiC Transistors," *J. Electr. Eng. Technol.*, vol. 9, no. 4, pp. 1332-1342, Jul. 2014.

[10] M. Kim, O. Seok, M.-K. Han, and M.-W. Ha, "High-Voltage AlGaN/GaN High-Electron-Mobility Transistors Using Thermal Oxidation for NiO_X Passivation," *J. Electr. Eng. Technol.*, vol. 8, no. 5, pp. 1157-1162, Sep. 2013.

[11] M. Kanamura, T. Ohki, T. Kikkawa, K. Imanishi, T. Imada, A. Yamada, and N. Hara, "Enhancement-Mode GaN MIS-HEMTs With n-GaN/i-AlN/n-GaN Triple Cap Layer and High-k Gate Dielectrics," *IEEE Electron Device Lett.*, vol. 31, no. 3, pp. 189-191, Mar. 2010.

[12] Y. Oh, and Y. Kim, "Gate Workfunction Optimization of a 32 nm Metal Gate MOSFET for Low Power Applications," *J. Electr. Eng. Technol.*, vol. 1, no. 2, pp. 237-240, Jun. 2006.

[13] D. Okamoto, H. Yano, K. Hirata, T. Hatayama, and T. Fuyuki, "Improved Inversion Channel Mobility in 4H-SiC MOSFETs on Si Face Utilizing Phosphorus-Doped Gate Oxide," *IEEE Electron Device Lett.*, vol. 31, no. 7, pp. 710-712, Jul. 2010.

[14] K. Matocha, T. Paul Chow, and R. J. Gutmann, "High-voltage normally off GaN MOSFETs on sapphire substrates," *IEEE Trans. Electron Devices*, vol. 52,

no. 1, pp. 6-10, Jan. 2005.
[15] G. Simin, A. Koudymov, A. Tarakji, X. Hu, J. Yang, M. A. Khan, M. S. Shur, and R. Gaska, "Induced strain mechanism of current collapse in AlGaN / GaN heterostructure field-effect transistors," *Appl. Phys. Lett.*, vol. 79, no. 16, pp. 2651-2653, Oct. 2001.
[16] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," *Appl. Phys. Express*, vol. 1, no. 1, pp. 011105-1-3, Jan. 2008.
[17] S. Yaegassi, M. Okada, Y. Saitou, M. Yokoyama, K. Nakata, K. Katayama, M. Ueno, M. Kiyama, T. Katsuyama, and T. Nakamura, "Vertical heterojunct-ion field-effect transistors utilizing re-grown AlGaN/ GaN two-dimensional electron gas channels on GaN substrates," *Phys. Status Solidi*, vol. 8, no. 2, pp. 450-452, Feb. 2011.
[18] S. K. Oh, C. G. Song, T. Jang, and J. S. Kwak, "Effect of electron-beam irradiation on leakage current of AlGaN/GaN HEMTs on sapphire," *J. Semicond. Technol. Sci.*, vol. 11, no. 6, pp. 617-621, Dec. 2013.
[19] H. Takato, K. Sunouchi, N. Okabc, A. Nitayama, K. Hieda, F. Horiguchi, and F. Masuoka, "High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs," in *IEDM Tech. Dig.*, pp. 222-225, Dec. 1988.
[20] S. Cho, J. S. Lee, K. R. Kim, B.-G. Park, James S. Harris, Jr., and I. M. Kang, "Analyses on Small-Signal Parameters and Radio-Frequency Modeling of Gate-All-Around Tunneling Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4164-4171, Dec. 2011.
[21] M. Karthigai Pandian, and N. B. Balamurugan, "Analytical Threshold Voltage Modeling of Surrounding Gate Silicon Nanowire Transistors with Different Geometries," *J. Electr. Eng. Technol.*, vol. 9, no. 6, pp. 2079-2088, Nov. 2014.
[22] P. Anandan, and N. Mohankumar, "Optimization and Characterization of Gate Electrode Dependent Flicker Noise in Silicon Nanowire Transistors," *J. Electr. Eng. Technol.*, vol. 9, no. 4, pp. 1343-1348, Jul. 2014.
[23] SILVACO International, ATLAS User's Manual, Apr. 2012.
[24] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proc. IEEE*, vol. 9, no. 6, pp. 1048-1058, Jun. 2002.
[25] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra, C. Canali, and E. Zanoni, "Surface-Related Drain Current Dispersion Effects in AlGaN-GaN HEMTs," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1554-1561, Oct. 2004.
[26] S. Huang, Q. Jiang, S. Yang, C. Zhou, and K. J. Chen, "Effective Passivation of AlGaN/GaN HEMTs by ALD-Grown AlN Thin Film," *IEEE Electron Device Lett.*, vol. 33, no. 4, pp. 516-518, Apr. 2012.
[27] S. Huang, Q. Jiang, S. Yang, Z. Tang, and K. J. Chen, "Mechanism of PEALD-Grown AlN Passivation for AlGaN / GaN HEMTs: Compensation of Interface Traps by Polarization Charges," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 193-195, Feb. 2013.
[28] S. Karmalkar and U. K. Mishra, "Enhancement of Breakdown Voltage in AlGaN/GaN High Electron Mobility Transistors Using a Field Plate," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1515-1521, Aug. 2001.
[29] J. -G. Lee, H. -J. Lee, H. -Y. Cha, M. Lee, Y. Ryoo, K. -S. Seo, and J. -K. Mun, "Field Plated AlGaN/GaN-on-Si HEMTs for High Voltage Switching Applications," *J. Korean Phys. Soc.*, vol. 59, no. 3, pp. 2297-2300, Sep. 2011.

Sung Yoon Kim He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2014. He is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of junctionless transistors, III-V tunneling FETs, and GaN-based devices.

Jae Hwa Seo He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2012. He is currently working toward the Ph.D. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of nanoscale CMOS, tunneling FET, III-V compound transistors, and junctionless silicon devices.

Young Jun Yoon He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2013. He is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of

nanoscale tunneling FET, GaN-based transistors, and GaN-based circuit.

Jin Su Kim He received the B.S. degree in electrical engineering from the School of Electronics Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2014. He is currently working toward the M.S. degree in electrical engineering with the School of Electronics Engineering (SEE), Kyungpook National University (KNU). His research interests include design, fabrication, and characterization of III-V compound transistors, GaN-based devices, and RF transistors.

Seongjae Cho He received the B.S. and Ph.D. degrees in electronic engineering from Department of Electrical Engineering and Computer Science, Seoul National University, Seoul, Korea, in 2004 and 2010, respectively. He worked as an Exchange Researcher at the National Advanced Industrial Science and Technology (AIST), Tsukuba, Japan, in 2009. He worked as a Postdoctoral Researcher at Seoul National University in 2010, and at the Department of Electrical Engineering, Stanford University, from 2010 to 2013. He has been working as an Assistant Professor at the Department of Electronic Engineering and the Department of IT Convergence Engineering, Gachon University, Seongnam-si, Korea, since 2013. His main research interests include nanoscale CMOS devices, emerging memory technologies, photonic devices, and integrated systems.

Jung-Hee Lee He received the B.S. and M.S. degrees in electronic engineering from Kyungpook National University, Daegu, in 1979 and 1983, respectively, the M.S. degree in electrical and computer engineering from Florida Institute of Technology, Melbourne, in 1986, and the Ph.D. degree in electrical and computer engineering from North Carolina State University, Raleigh, in 1990. His doctoral research concerned carrier collection and laser properties in monolayer-thick quantum-well heterostructures. From 1990 to 1993, he was with the Compound Semiconductor Research Group, Electronics and Telecommunication Research Institute, Daejeon, Korea. Since 1993, he has been a Professor with the School of Electronics Engineering (SEE), Kyungpook National University, Daegu. He is the author or coauthor of more than 200 publications on semiconductor materials and devices. His current research is focused on the growth of nitride-based epitaxy, the fabrication and characterization of gallium-nitride-based electronic and optoelectronic devices, atomic layer epitaxy for metal-oxide-semiconductor application, and characterizations and analyses for the 3-D devices such as fin-shaped FETs.

In Man Kang He received the B.S. degree in electronic and electrical engineering from School of Electronics and Electrical Engineering, Kyungpook National University (KNU), Daegu, Korea, in 2001, and the Ph.D. degree in electrical engineering from School of Electrical Engineering and Computer Science (EECS), Seoul National University (SNU), Seoul, Korea, in 2007. He worked as a teaching assistant for semiconductor process education from 2001 to 2006 at Inter-university Semiconductor Research Center (ISRC) in SNU. From 2007 to 2010, he worked as a senior engineer at Design Technology Team of Samsung Electronics Company. In 2010, he joined KNU as a full-time lecturer of the School of Electronics Engineering (SEE). Now, he has worked as an assistant professor. His current research interests include CMOS RF modeling, silicon nanowire devices, tunneling transistor, low-power nano CMOS, and III-V compound semiconductors. He is a member of IEEE EDS.