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RF MOSFET의 바이어스 종속 게이트-드레인 오버랩 캐패시턴스의 새로운 SPICE 모델링

(New SPICE Modeling for Bias-Dependent Gate-Drain Overlap Capacitance in RF MOSFETs)

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(Sangjun Lee and Seonghearn Lee©)

요 약

기존의 BSIM4 모델과 다이오드를 사용한 BSIM4 Macro 모델의 바이어스 종속 게이트-드레인 오버랩 캐패시턴스 C_{gdo} 시뮬레이션의 부정확성에 대하여 자세히 분석하였다. 이러한 Macro 모델은 기존의 BSIM4 모델보다 더 정확하지만 선형영역에서 사용될 수 없음을 발견하였다. 기존 모델들의 부정확성을 제거하기 위해서 물리적인 바이어스 종속 C_{gdo} 모델 방정식을 사용한 새로운 BSIM4 Macro 모델을 제안하였고 전체 바이어스 영역에서 유효함을 입증하였다.

Abstract

The inaccuracy of the bias-dependent gate-drain overlap capacitance C_{gdo} simulation in original BSIM4 and BSIM4 macro model using a diode is analyzed in detail. It is found that the accuracy of the macro model is better than of the BSIM4. However, the macro model cannot be used in the linear region. In order to remove the inaccuracy of the conventional models, a new BSIM4 macro model with a physical bias-dependent C_{gdo} equation is proposed and its accuracy is validated in the full bias range.

Keywords : MOSFET, RF, Modeling, SPICE model, overlap capacitance

I. Introduction

For the accurate design of RF integrated circuits (ICs), it is important that MOSFETs should be modeled at the high-frequency region and wide voltage range. For accurate modeling of RF MOSFETs, the gate-drain overlap capacitance C_{gdo} is a very important parameter as the feedback capacitance affecting power gain. An inaccurate C_{gdo} model can lead to incorrect SPICE simulation results for the cut-off frequency f_T and the maximum oscillation frequency $f_{\max}$[1].

Recently, BSIM4[2] is widely used as a RF SPICE model of MOSFETs. In the original BSIM4, C_{gdo} is modeled as the bias-dependent $CGDL$ in the LDD (lightly doped drain) region and bias-independent $CGDO$ in the $Non-LDD$ region in the gate-drain

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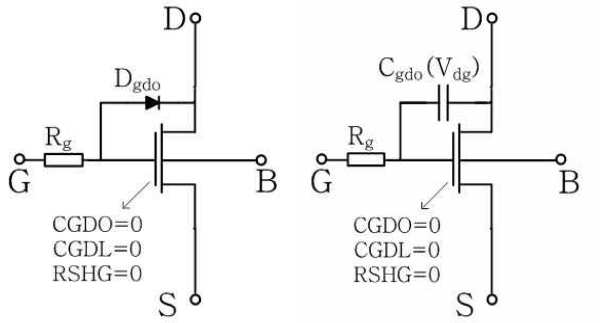
overlap region. However, when the drain-gate voltage V_{dg} $(= V_{ds} - V_{gs})$ for N-MOSFETs is in the negative range, the BSIM4 is unable to model C_{gdo}.

In order to improve the original BSIM4, a BSIM4 macro model adding the gate-drain junction diode D_{gdo}[3] has been used for a N-MOSFET in Fig. 1(a). The bias-dependent C_{gdo} due to the depleted $n^- - LDD$ below the oxide layer in the gate-drain overlap region in the positive V_{dg} is modeled by adding D_{gdo}. However, D_{gdo} is unable to model C_{gdo} in the negative V_{dg}. In particular, the macro model does not work in the linear region of $V_{dg} < -V_{th}$ because D_{gdo} turns on.

In order to model C_{gdo} in the negative V_{dg} accurately in this paper, an improved bias-dependent C_{gdo} equation is constructed by modeling a parasitic MOS capacitor in the gate-drain overlap LDD region.



(a) (b)

그림 1. 두 가지 BSIM4 macro MOSFET 모델. C_{gdo}와 R_g의 내부 값을 제거하기 위하여 BSIM4 파라미터 $CGDO$, $CGDL$과 $RSHG$가 0으로 설정됨
(a) 다이오드를 사용한 BSIM4 macro N-MOSFET모델
(b) 바이어스 종속 C_{gdo}를 사용한 새로운 BSIM4 macro 모델

Fig 1. Two BSIM4 macro MOSFET models. The BSIM4 parameters of $CGDO$, $CGDL$, and $RSHG$ are set to zero to eliminate the internal values of C_{gdo} and R_g.
(a) A BSIM4 macro model using a diode for N-MOSFET.
(b) A new BSIM4 macro model using a bias-dependent C_{gdo}.

Ⅱ. Modeling and Analysis

1. C_{gdo} Measurement

S-parameters are measured on multi-finger N-MOSFETs with the gate length (L_g = 0.18㎛), the gate finger number (Nf = 16) and the unit finger width (W_u = 5㎛). An accurate de-embedding procedure was carried out to remove pad and interconnection parasitics from measured S-parameters[4].

After the drain, source and substrate resistances are determined by using a RF direct extraction method[5~6] and the gate resistance is extracted from a non-quasi-static model[7], intrinsic Y^i-parameters are determined by subtracting them from measured S-parameters. Using Y_{12}^i-parameter in the low-frequency(LF) region, C_{gdo} in the saturation region is extracted by[6]:

$$C_{gdo} \approx -\frac{1}{\omega} Imag(Y_{12}^i)_{LF} \quad (1)$$

Fig. 2 shows (1) versus frequency along the wide variation of V_{gs} at V_{ds} = 1V for a N-MOSFET. Since the surface depletion width in the gate-drain overlap $n^- - LDD$ region decreases with increasing V_{gs}, C_{gdo} increases.

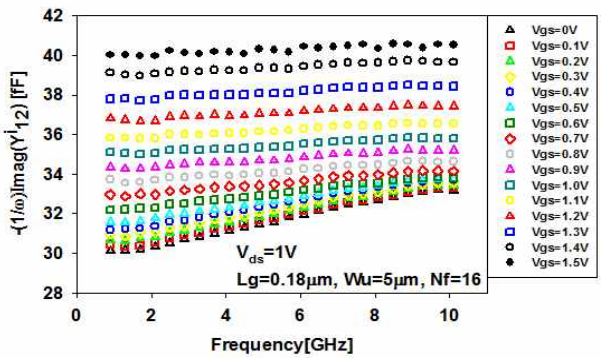


그림 2. V_{gs} 변화에 따라 추출된 $(-1/\omega)Imag(Y_{12}^i)$ 대 주파수 그래프

Fig 2. Extracted $(-1/\omega)Imag(Y_{12}^i)$ values versus frequency at various V_{gs}.

2. Analysis of Conventional Models

In Fig. 3, C_{gdo} values extracted from Fig. 2 in the low-frequency region are plotted as a function of V_{dg} with those of the original BSIM4 and BSIM4 macro model using D_{gdo}. Since the surface of $n^- - LDD$ region under the oxide layer begins to be depleted from V_{dg} of flat-band voltage V_{FBO} in the drain overlap region for N-MOSFET, C_{gdo} decreases with increasing V_{dg} in the saturation region of $V_{dg} > -V_{th}$ at V_{th} =0.46V. The measurement data at $V_{dg} < -0.46$ V are excluded in Fig. 3, because the channel capacitance in the linear region is included in the data.

The BSIM4 drain overlap capacitance is modeled by the differential $dQ_{overlap,d}/dV_{gd}$ of the following charge equation[2]:

$$\frac{Q_{overlap,d}}{W_{active}} = CGDO \cdot V_{gd} + CGDL\left[V_{gd} - V_{gd,overlap} - \frac{CKAPPAD}{2}\left(-1+\sqrt{1-\frac{4V_{gd,overlap}}{CKAPPAD}}\right)\right] \quad (2)$$

$$V_{gd,overlap} = \frac{1}{2}\left(V_{gd}+\delta_1 - \sqrt{(V_{gd}+\delta_1)^2+4\delta_1}\right) \quad where \quad \delta_1 = 0.02V \quad (3)$$

where $CKAPPAD$ is defined as the coefficient of bias-dependent overlap capacitance for the drain side.

The decreasing surface depletion capacitance at the positive $V_{dg}(=-V_{gd})$ in Fig. 3 can be modeled by fitting $dQ_{overlap,d}/dV_{dg}$ of (2). However, C_{gdo} becomes saturated in the range of $V_{dg} < -0.2$V because $V_{gd,overlap}$ of (3) rapidly approaches to zero with decreasing $V_{dg}(=-V_{gd})$ in the negative range. Thus, the BSIM4 drain overlap capacitance model shows the substantial disagreement with the measurement data below V_{dg} = -0.2V in Fig. 3.

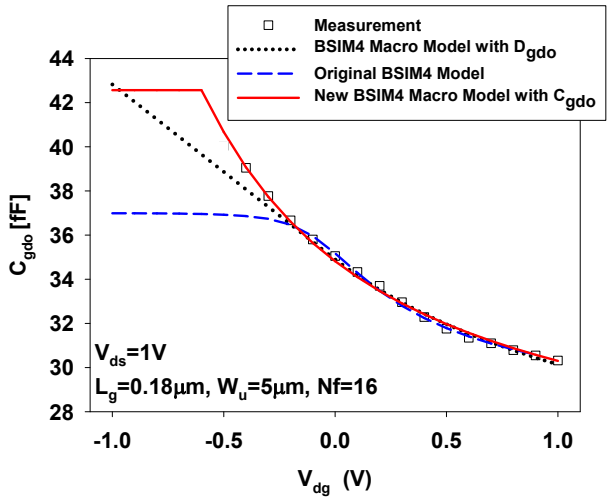


그림 3. N-MOSFET의 측정값과 모델된 C_{gdo} 대 V_{dg}
Fig 3. Measured and modeled C_{gdo} versus V_{dg} for N-MOSFET.

For the BSIM4 macro model using D_{gdo}[3] in Fig. 1(a), the junction diode C_{gdo} equation is defined by[8]:

$$C_{gdo} = \frac{C_{jo}}{\left[1+\left(\frac{V_{dg}}{V_j}\right)\right]^{M_j}} \quad \text{for } V_{dg} > 0 \quad (4)$$

$$C_{gdo} = C_{jo}\left[1 - M_j\left(\frac{V_{dg}}{V_j}\right)\right] \quad \text{for } V_{dg} < 0 \quad (5)$$

where C_{jo}, M_j and V_j are defined as the junction capacitance at zero-bias, the grading coefficient and built-in voltage, respectively. Although (4) and (5) are physically unacceptable for a parasitic MOS capacitor in the gate-drain overlap LDD region, these can be used for an empirical model.

The surface depletion capacitance decreased at $V_{dg} > 0$ is accurately fitted by (4) in Fig. 3. However, the depletion capacitance at $V_{FBO} < V_{dg} < 0$V in Fig. 3 can not be modeled by the linear dependent equation of (5).

Theoretically, C_{gdo} is unchanged as the oxide capacitance C_{OLD} over the drain overlap region at $V_{dg} \leq V_{FBO}$, because the surface of $n^- - LDD$ in the gate-drain overlap region is accumulated. Thus, the linear equation of (5) is unable to model the bias-independent C_{gdo} at $V_{dg} \leq V_{FBO}$.

3. New BSIM4 Macro Modeling

In order to overcome the problems of the conventional models, a physical bias-dependent C_{gdo} model is newly developed in this work. The new C_{gdo} model parameters are represented in Fig. 4. L_{OV} is

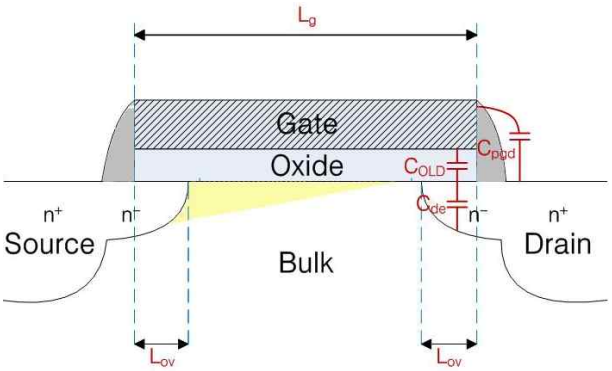


그림 4. 새로운 BSIM4 오버렙 캐패시턴스 모델의 파라미터 성분들을 나타낸 포화영역에서의 MOSFET 단면도

Fig 4. Schematic diagram of a MOSFET structure in the saturation region to explain overlap capacitance model parameters in a new BSIM4 macro model

defined as the drain overlap length at the drain overlap LDD region.

In a parasitic MOS capacitor in the gate-drain overlap $n^- - LDD$ region , the oxide capacitance C_{OLD} is connected in series with the surface depletion capacitance C_{de} in the drain LDD region[9]. Together with the series capacitances, the parasitic gate-drain capacitance C_{pgd} occurring to the exterior of the drain LDD region is connected in parallel[9].

Thus, a physical bias-dependent C_{gdo} model is expressed as:

$$C_{gdo} = \frac{C_{OLD} \cdot C_{de}}{C_{OLD} + C_{de}} + C_{pgd} \tag{6}$$

In this work, the depletion capacitance at the surface of the LDD region is modeled by:

$$C_{de} = C_o\left(1 - \frac{V_{dg}}{V_{FBO}}\right)^{-M} \quad \text{for } V_{dg} > V_{FBO} \tag{7}$$

where V_{FBO} is a negative number for N-MOSFETs, and C_o and M are defined as the zero-bias capacitance and the grading coefficient, respectively. This capacitance is generated by the expansion of the depleted surface layer of $n^- - LDD$ region due to more band bending at higher V_{dg}[9].

Since C_{OLD} is independent of the bias and C_{de} is reduced with increasing V_{dg}, C_{gdo} decreases as shown in Fig. 3. If C_{de} in (6) is significantly decreased until $C_{de} << C_{OLD}$ at very high V_{dg}, (6) is reduced by:

$$C_{gdo} \approx C_o\left(1 - \frac{V_{dg}}{V_{FBO}}\right)^{-M} + C_{pgd} \tag{8}$$

Thus, C_{pgd} of 24.16fF is accurately extracted by fitting (8) to C_{gdo} data at V_{dg} = 0.7 ~ 1V. When the $n^- - LDD$ region is accumulated at $V_{dg} \leq V_{FBO}$, C_{gdo} is determined by C_{OLD}+C_{pgd}. However, C_{OLD} is unable to be directly extracted from measured C_{gdo} data at $V_{dg} \leq V_{FBO}$, because the channel capacitance C_{GC} is added in the linear region ($V_{dg} < -V_{th}$). Thus, C_{OLD} needs to be independently extracted using another method.

In order to extract C_{OLD}, the oxide capacitance per unit area C_{OX} is accurately extracted by the following equation at V_{ds} = 0V:

$$C_{OX} = \frac{C_G - C_{PG}}{NF \cdot W_u \cdot (L_g - 2L_{OV})} \tag{9}$$

where C_{PG} is the extrinsic parasitic capacitance outside the channel area at V_{ds} = 0V.

The total gate capacitance C_G at L_g is extracted by using the data of $(-2/\omega)Imag(Y_{12}^i)_{LF}$ at V_{ds} = 0V and V_{gs} = 0.7V under the assumption of symmetric source and drain for the N-MOSFETs[10].

In order to determine L_{OV}, a RF direct extraction method[11] is applied as follows: The gate-bulk capacitance C_{gb} in the low-frequency region is determined by:

$$C_{gb} \approx \frac{1}{\omega} Imag(Y_{11}^i + 2Y_{12}^i)_{LF} \tag{10}$$

Since the inversion charge layer totally shields the intrinsic bulk region from the gate, the intrinsic gate-bulk capacitance C_{GBI} in the channel area is masked due to the inversion region at $V_{gs} > V_{th}$. Thus, the extrinsic gate-bulk capacitance C_{GBE} is

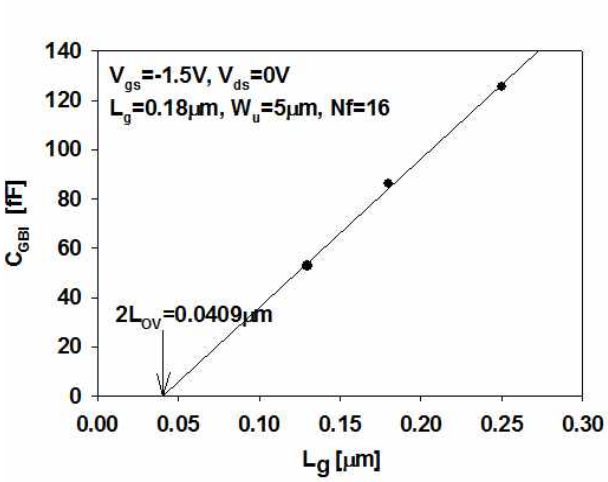


그림 5. 추출된 C_{GBI} 대 L_g 데이터와 피팅 선
Fig 5. Extracted values and their regression line of C_{GBI} versus L_g.

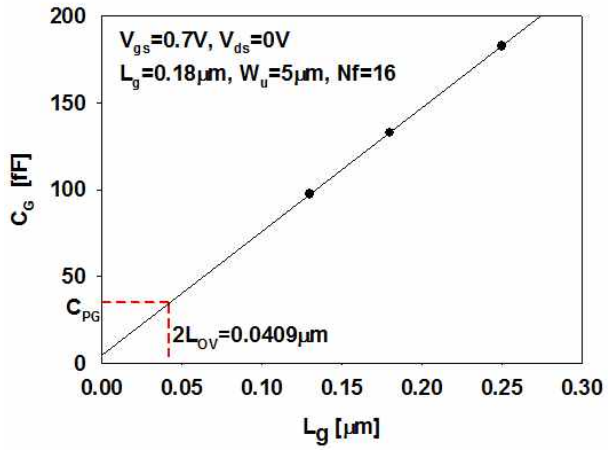


그림 6. 추출된 C_G 대 L_g 데이터와 피팅 선
Fig 6. Extracted values and their regression line of the C_G versus L_g.

accurately extracted by (10) at $V_{gs} > V_{th}$. In this method, C_{GBI} is extracted by subtracting (10) at V_{gs} = 0.6V and V_{ds} = 0V from (10) at V_{gs} = -1.5V and V_{ds} = 0V. As shown in Fig. 5, L_{OV} is determined from the x-intercept of a linear regression line for C_{GBI} vs. L_g at V_{gs} = -1.5V that is the flat band voltage of the channel region.

In order to extract the oxide capacitance C_G-C_{PG} in the channel area in (9), C_{PG} is determined from C_G value at $L_g = 2L_{OV}$[10] as shown in Fig. 5. After C_{OX} is extracted by substituting C_{PG} and L_{OV} into (9), C_{OLD} is calculated by $C_{OX} \cdot NF \cdot W_u \cdot L_{OV}$.

In order to extract M, C_o and V_{FBO} accurately, (6) at $V_{dg} \geq V_{FBO}$ is rewritten by:

$$\frac{1}{C_{gdo}-C_{pgd}} = \frac{1}{C_{OLD}} + \frac{1}{C_{de}} = \left[\frac{1}{C_{OLD}} + \frac{1}{C_o}\left(1-\frac{V_{dg}}{V_{FBO}}\right)^M\right] \quad (11)$$

The values of V_{FBO} = -0.6V, C_o = 25.3fF and M =1.03 are extracted by fitting (11) to $1/(C_{gdo}-C_{pgd})$ data in the saturation region of $V_{dg} \geq$ -0.5V.

For HSPICE modeling, a following bias-dependent C_{gdo} equation is constructed by:

$$C_{gdo} = \frac{1}{\frac{1}{C_{OLD}} + \frac{1}{C_o}\left(\frac{1+sgn(V_{dg}-V_{FBO})}{2}\right)\left(1-\frac{V_{dg}}{V_{FBO}}\right)^M} + C_{pgd} \quad (12)$$

where the sgn(x) function (= 1 at x > 0, 0 at x=0, -1 at x < 0) is a HSPICE built-in function[8] used to define the effective range of $V_{dg} \geq V_{FBO}$ in (7).

4. Accuracy Analysis of the New Model

As shown in Fig. 3, a modeled C_{gdo} curve of Fig. 1(b) using (12) exhibits better agreement with the measurement data than the conventional ones. Unlike the conventional models, the new macro model with C_{gdo} provides a more accurate overlap capacitance simulation in the range of $V_{dg} < 0$ by modeling a parasitic MOS capacitor in the gate-drain overlap region physically.

As shown in Fig. 7 and table I, in order to confirm the RF accuracy of the new BSIM4 macro model with a bias-dependent C_{gdo} in Fig. 1(b), frequency-dependent power gain Gmax curves and average Gmax errors for the new and conventional models are compared with measurement data at V_{gs} = 1.4V and V_{ds} = 1V. The modeled Gmax values and errors of the conventional models is much larger than those of the new one, because C_{gdo} is underestimated in the original one. Although the BSIM4 macro model

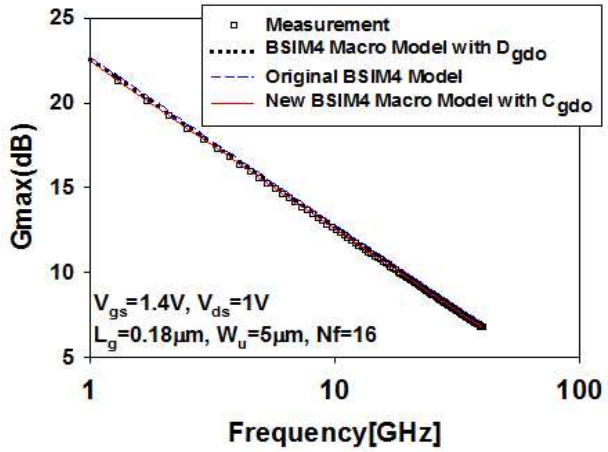


그림 7. 측정값과 모델된 주파수 종속 전력 종속 곡선
Fig 7. Measured and modeled frequency-dependent power gain curves.

표 1. 측정값과 모델된 주파수 종속 전력종속 곡선 데이터의 에러율(Vgs= 1.4V and Vds = 1V)
Table 1. The average errors of measured and modeled frequency-dependent power gain curves data (Vgs= 1.4V and Vds = 1V).

Models	$Average\ G_{\max} Error(\%)$
Original BSIM4 model	5.99
BSIM4 macro model with D_{gdo}	2.63
New BSIM4 macro model with C_{gdo}	0.18

* $Average\ G_{\max} Error(\%) = \frac{100}{N}\sum_{f}\left|\frac{measured\ G_{\max} - \mathrm{model}ed\ G_{\max}}{measured\ G_{\max}}\right|$

where N is the number of frequency f

with a diode shows the better agreement than the original BSIM4, it still results in larger simulation errors than the new one at $V_{dg} < -V_{th}$ as a result of (5).

As a result, the new model shows the best agreement with measured one than the conventional models.

Ⅲ. Conclusions

The inaccuracy of the original BSIM4 and BSIM4 macro model using a diode is revealed in detail. In order to get rid of the inaccuracy, a physical bias-dependent C_{gdo} equation for N-MOSFETs is derived by modeling a parasitic MOS capacitor using the series connection of C_{OLD} and C_{de} with the paralleled C_{pgd} in the gate-drain overlap region. Unlike the conventional models, a new BSIM4 macro model with the C_{gdo} equation is able to accurately model C-V characteristics at full bias region. This new model is demonstrated by observing much better agreements with measured power gain versus frequency than that of the original BSIM4.

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