Wide-Input Range Dual Mode PWM / Linear Buck Converter with High robustness ESD Protection Circuit

Bo-Bae Song and Yong-Seo Koo*

Abstract—**This paper proposes a high-efficiency, dual-mode PWM / linear buck converter with a wide-input range. The proposed converter was designed with a mode selector that can change the operation between PWM / linear mode by sensing a load current. The proposed converter operates in a linear mode during a light load and in PWM mode during a heavy load condition in order to ensure high efficiency. In addition, the mode selector uses a bit counter and a transmission gate designed to protect from a malfunction due to noise or a time-delay. Also, in conditions between -40 °C and 140 °C, the converter has variations in temperature of 0.5mV/°C in the PWM mode and of 0.24 mV/°C in the linear mode. Also, to prevent malfunction and breakdown of the IC due to static electricity, the reliability of IC was improved by embedding a self-produced 8 kV-class(Chip level) ESD protection circuit of a P-substrate Triggered SCR type with high robustness characteristics.**

Index Terms—PWM, linear, dual-mode, buck-converter, load-current

I. INTRODUCTION

The differential power management ICs (PMIC) are commonly used in battery-powered portable electronics, including smartphones and research and development of high-efficiency PMICs is essential in order for the power

consumption of portable devices to be adequate for a greater range of functions than in the past.

High-efficiency PMICs have generally shown drastic changes in their use, from linear regulators to switching regulators, but switching regulators have a disadvantage in that they offer low efficiency relative to that of linear regulators under a light load condition. This paper therefore presents a dual-mode converter that increases the efficiency of power consumption by operating as a linear regulator under a light load and as a switching regulator under a heavy load condition.

The PWM mode switching regulator can operate at 1.8 MHz to obtain a low ripple voltage. In the linear mode, the proposed LDO regulator operates with a high efficiency relative to that with the PWM mode under a light load. Two methods are presented in this paper to change the mode of the controller by sensing the load current [1, 2].

II. PWM / LINEAR DUAL MODE BUCK CONVERTER

1. Proposed Buck Converter

The proposed converter is capable of changing from a PWM to a linear mode by sensing the load current. For the PWM mode, a current mode is used, and in order to maintain high efficiency, the proposed converter operates in the linear mode under a light load and operates in the PWM mode under a heavy load. Furthermore, the proposed protection circuit prevents a malfunction of the product. Fig. 1 below shows the function block diagram of the proposed buck converter.

Fig. 2(a) shows the flow of current in the PWM mode.

The current is applied through the input terminal, and the current is provided to the load through the inductor. Fig. 2(b) shows the flow of the current in the linear mode. The current is applied through the input terminal and the current is provided to the load through the LDO_out terminal [3-6].
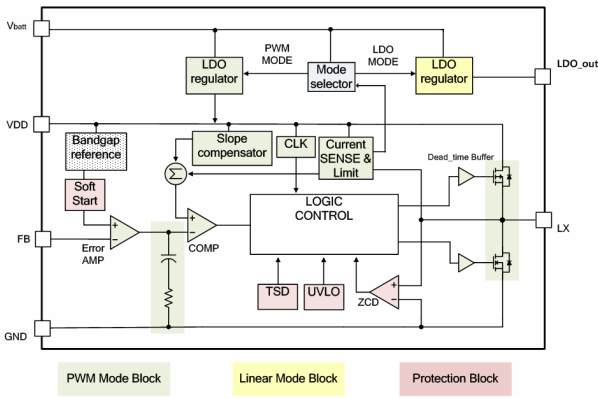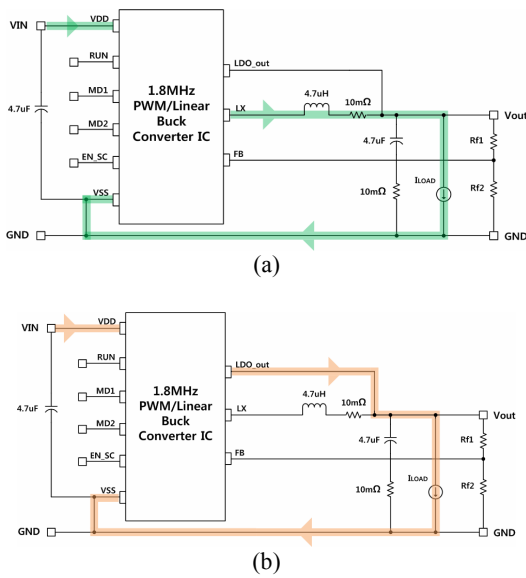

Fig. 1. Functional block diagram.

Fig. 2. Proposed buck converter (a) PWM mode block, (b) linear mode block.

2. Mode Selector

In this study, a mode selector was designed to provide mode switching according to the conditions of the load current. The method through which the mode changes are described below. When the IC is driven in the PWM mode by a heavy load, the linear regulator is blocked in order to prevent additional power consumption. When

the current is reduced to 5 mA or less, which is considered to be a light load, the device switches to the linear regulator. The method that is used to detect the load current allows for the current flowing through the inductor to be converted from a PWM mode to a linear mode [7-10], and the converter was driven through the current mode control method and was designed to enable switching the mode by sensing the current through a current-sensing circuit with no additional circuit design.

However, this method has two major outstanding issues that need to be attended. The first issue is that when the device switches from the PWM mode to the linear mode, the load current value for which the linear mode can provide a higher efficiency than the PWM mode must be known. The appropriate values must be set by performing a simulation to measure the efficiency under different load currents of each mode and then comparing the values thereof. The second issue is that the current-sensing circuit may not be stable due to the influence of noise or other errors that can occur during design. Therefore, in this paper, the values that were detected in the current-sensing circuit were amplified in order to prevent malfunction due to noise and error and
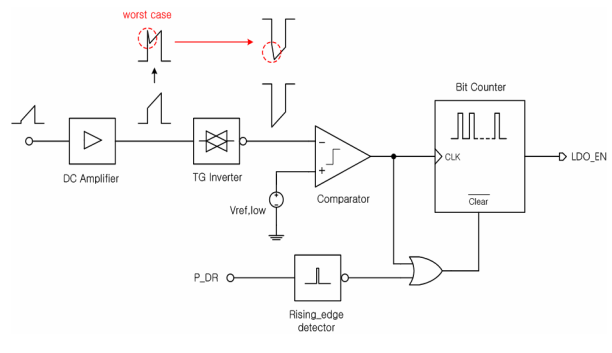

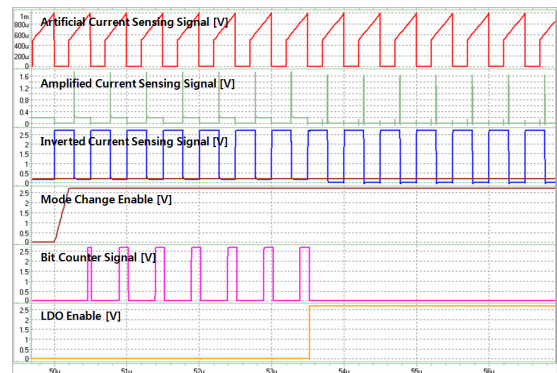**Fig. 3.** Conversion from PWM to linear.

Fig. 4. Simulation of conversion from PWM to linear.

to enable stable switching. Furthermore, the circuit was designed in such a manner that the number of final output signals for mode switching could be counted through a counter block so that no malfunction would occur due to noise or delay time.

Fig. 3 shows the block diagram for the conversion from the PWM mode to the linear mode. P_DR pin is input of a high side switch. The voltage that was detected through the current-sensing circuit was amplified to 100 mV through a DC amplifier. The current-sensing circuit in the mode selector causes a spike because it detects the inductor current when switching. This phenomenon achieves more consistent behavior when under a light load. The high spike leads to the comparator consuming additional power, which can then cause a malfunction as a result of the noise. In order to prevent this, the amplified sensing voltage is reversed with the use of a Transmission Gate inverter(TG inverter) in order to convert to a stable voltage. TG inverter passes the signal only when a PMOS and NMOS connected in parallel is turned on at the same time. This method can therefore suppress the additional power consumption from the comparator. Spike phenomenon can be removed by reversing the phase by using a TG inverter. The current-sensing signal that is converted for mode switching is formed through the reference voltage at the comparator, and the generated signal is converted into the linear mode after a certain pulse is applied by the bit counter block. This method prevents a malfunction that can occur due to noise or time delay and it restores the initial condition through the clear terminal if the current is not low [11-15]. As a result, generated LDO_EN signal operate linear mode and stop PWM mode simultaneously.

Fig. 4 shows the results of the simulation of the mode conversion of the circuit presented in Fig. 3. The spike occurs in the current-sensing voltage that was amplified via switching, and the spike is removed by reversing the phase with the TG inverter. The removed signal and the reference voltage are compared and a clock is created for the mode conversion. When a total of seven clocks is applied through the 3-bit structure of the bit counter, the signals converted to the linear mode are formed, and the LDO_EN signal blocks the PWM controller block in order to reduce the additional current consumption.

On the other hand, if the regulator in the linear mode operates under a light load, mode switching must therefore be performed by detecting the low current. When switching to the PWM mode by detecting a heavy load, the PWM controller must begin operation before the linear regulator is blocked. Mode switching in the PWM mode is easy as a result of the current-sensing circuit, but the LDO regulator requires an additional circuit in order to detect the load current because the current sensing circuit is blocked. In this paper, therefore, the device uses the structure of the over current limit circuit that detects the gate voltage of the pass transistor and copies the current in order to detect the load current.

Switches S1 and S2 in Fig. 5 select the manual mode or the automatic mode. If you only want to drive the
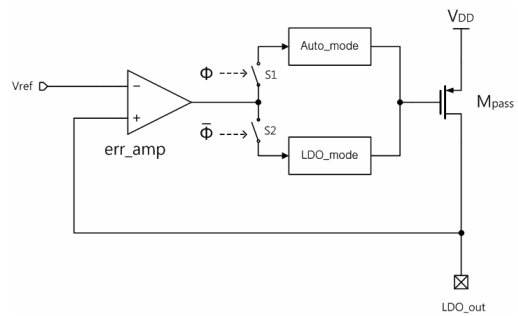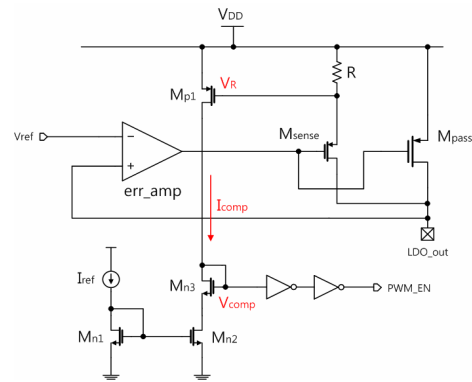

Fig. 5. LDO regulator of linear mode.

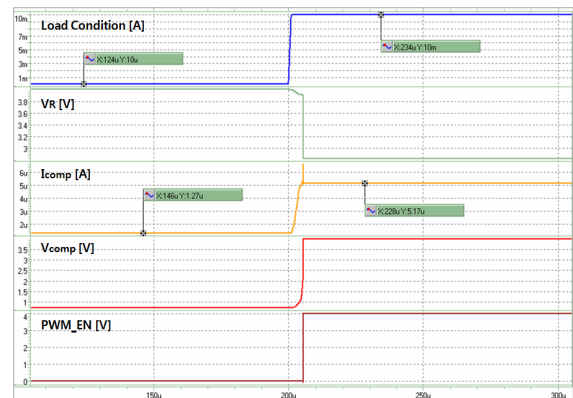**Fig. 6.** Conversion from linear to PWM.

Fig. 7. Simulation of conversion from linear to PWM.

LDO regulator according to input values of the external pin, IC does not operate in the PWM operating mode and LDO regulators were designed to operate only through the LDO_mode block.

Switch1(S1) and Switch2(S2) serves to determine the condition of the LDO regulator operation according to the external pin. If you only want the PWM drive method, S1 and S2 are both open states. So LDO regulators no longer operate.

Automatic mode according to load current achieved in switch1(S1) is close state and switch2(S2) is open state.

Fig. 6 shows a schematic diagram of the conversion from the linear mode to PWM mode. With respect to the circuit structure, a circuit is used to limit the over current in the LDO regulator. The mode change from the linear mode to PWM mode through the use of a pass transistor gate voltage-sensing circuit in Fig. 6. Since the gate and the drain terminals of the pass transistor and the detection transistor are common, it is easy to copy the current by the size ratio. The copied current forms a voltage across the resistance R, which then forms a signal in Mn3 through a comparison with the reference current source. To ensure stable operation and to prevent malfunction, the device was designed so that the logic threshold voltage of the inverter can be adjusted. As a result, generated PWM_EN signal operate PWM mode and stop linear mode simultaneously.

Fig. 7 shows the results of the simulated mode conversion in the circuit shown in Fig. 6. The gate voltage at Mp1 decrease as the load current increases, and the reason for this is that when the load current increases, more current flows through Msense. So, the gate voltage at Mp1 decreases as the potential difference between the two ends of resistance R increases. If the contact VR gradually decreases, the Vgs of Mp1 increases, and this in turn increases the current passing through the corresponding branch. The limit of this increase is determined by the reference current source, and as a result, the change in Vgs for Mp1 simultaneously changes the current of the branch and the operation range of Mp1. Thus, a rapid change in the voltage can be verified through the gate voltage of Mn3.

The Vcomp changes to a clear digital signal through the inverter and the signals that are created play a role in switching from the linear mode to the PWM mode through the PWM_EN terminal.

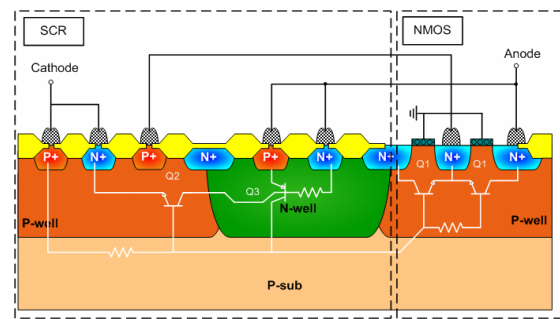## 3. Proposed PTSCR(P-substrate Triggered SCR)

Fig. 8. PTSCR structure (P-substrate Triggered SCR).

Fig. 8 shows the structure of the PTSCR, which acts as the ESD protection circuit. This device consists of 2-Finger Gate Grounded NMOS structures at the right-hand side and an SCR that contains additional bridge N+ and P+ diffusion areas (P+ Tab). This structure enables the following characteristics of the proposed device. First, the parallel arrangement of the 2-Finger GGNMOS structures comprises two drain areas (bridge N+, N+ anode) which lowers the avalanche breakdown voltage with P-Well and enables a lower trigger voltage. Second, when the ESD current flows in, this device works separately between the first operation by the GGNMOS and the second operation by the SCR. As a result of the first operation process by the GGNMOS, this device generally has a high trigger current and a high holding current. Third, the bridge N+ and P+ diffusion areas (P+ Tab) on the discharge path of the SCR decrease the current gain of the parasitic NPN and PNP of the SCR, increasing the general holding voltage of SCR. In particular, the P+ diffusion area (P+ Tab) is connected to the source of the GGNMOS and supply the trigger current from the GGNMOS to the SCR.

ESD coming from anode causes avalanche breakdown between N+ and P- well junction, which in turn creates EHP. And the parasitic NPN BJT(Q1) is turned on by the created EHP. The hole current flows into P-well through P+ of SCR via parasitic NPN BJT(Q1). When the electrical potential of P-well becomes larger than the potential barrier at P-well and N+ cathode junction, the parasitic NPN BJT(Q2) of SCR is turned on, and the operation of NPN BJT(Q2) turns on the parasitic PNP BJT(Q3) of SCR. As the positive feedback operation of parasitic NPN/PNP BJT turns on SCR, most of ESD current is discharged via the path of SCR.
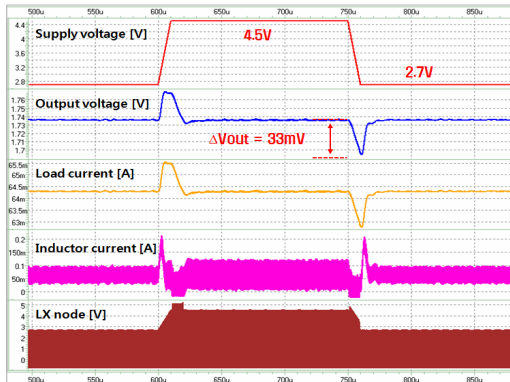
III. SIMULATION RESULTS

1. PWM mode

Fig. 9. Line transient response in PWM mode.
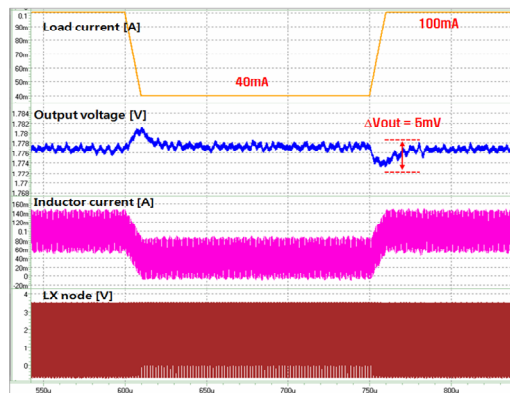

Fig. 10. Load transient response in PWM mode.

Fig. 9 shows the waveforms observed through the simulation that verify the output voltage through a change of the input voltage when the IC operates in the PWM mode. When the input voltage suddenly changed, the waveform of the output voltage increased along with the input voltage, but the output voltage returned to its original value through negative feedback provided by the error amplifier. The same characteristic can be found when the input voltage decreases, i.e., the output voltage decreases and then returns to its original value. A change of about 33 mV in the output voltage can be verified.

Fig. 10 shows the simulation waveform that shows a change in the output voltage when the load current changes from 100 mA to 40 mA for 10 µs at a fixed input voltage in the PWM mode. As the load current decreases, the output voltage shows a rising and falling pattern, but returns to its original value through negative feedback, and a 5 mV change in the output voltage can be verified.
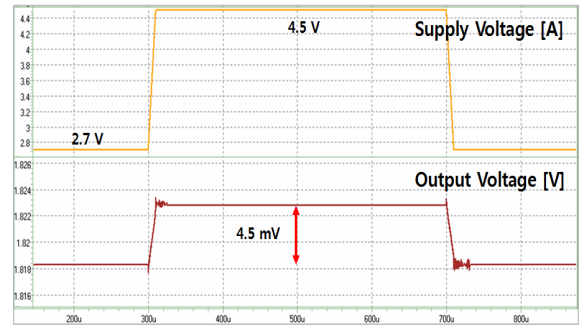
2. Linear mode

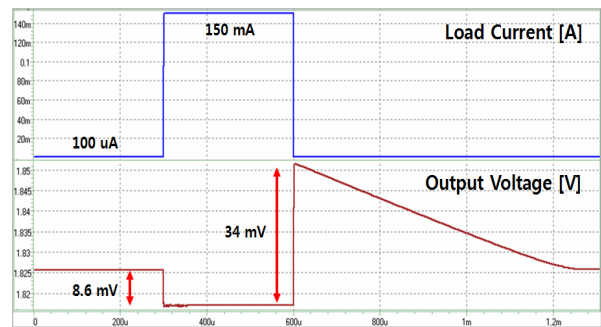**Fig. 11.** Line transient response in linear mode.

Fig. 12. Load transient response in linear mode.

Fig. 11 shows the simulation waveform that verified the output voltage that was achieved through a change in the input voltage when the IC was operating in the linear mode. When the input voltage suddenly changed, the waveform of the output voltage increased along with the input voltage, but the output voltage returned to its original value through negative feedback provided by the error amplifier. A 4.5 mV change in the output voltage was verified. Fig. 12 shows the simulation waveform that shows a change in the output voltage when the load current changes from 100 uA to 150 mA for 10 µs at a fixed input voltage in the linear mode. As the load current decreases, the output voltage shows a rising and falling pattern, but returns to its original value through negative feedback. The change in the output voltage shows a different pattern obtained through a change in the load value.

3. Auto mode

Fig. 13 shows the final results of the simulation in the auto mode. When the first enabling signal was applied, the soft start circuit began operation, and the output

voltage slowly increased. After a transient flow at the inductor, a value in the mA range was maintained.

In addition, the reverse current protection circuit allowed for the initial current of the inductor to not flow to the ground, and after the soft start circuit was blocked, the load variation indicated that the mode switching and the voltage maintenance were operating as intended.

When the load current was reduced to 5 mA or lower, the switching operation between the inductor and the ground stopped, and the device changed from the PWM mode to the linear mode. In order to verify the possibility of re-switching from the linear mode to the PWM mode, the load current was increased.

As a result, switching occurs at the switching contact, and the output voltage decreased due to the transient reduction of the load resistor. Then, a constant output voltage was again supplied.
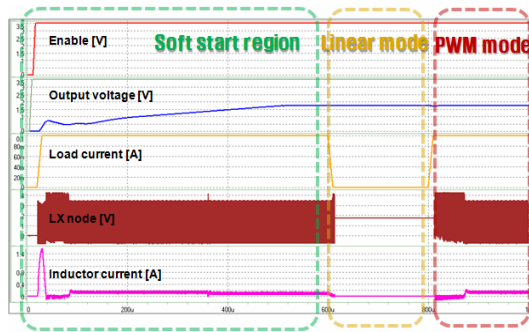

Fig. 13. Auto mode simulation.

IV. MEASUREMENT RESULTS

Figs. 14 and 15 show the results measured in order to verify the mode switching in the auto mode, resulting from a variation in the load between a heavy load and a light load. Fig. 14 shows the waveform that switches from the PWN mode to the linear mode, which is enabled through the PWM_EN signal that was created by detecting the load current.

Fig. 14(a) shows the switching operation that occurred at the switching node when the PWM_EN signal was high, and the switching operation in the switching node halted when the PWM_EN signal changed to a low signal. Fig. 14(b) shows the results of the output voltage measured when the mode switched. The output voltage showed a 5 mV change during mode switching. Fig. 15 shows the waveform that switches from the linear mode

to the PWM mode. As shown in Fig. 15(a), switching occurred in the switching node when the PWM_EN signal changed from a low to a high signal due to the increase in the load current. Fig. 15(b) shows the results of the output voltage measured when the mode switched from the linear mode to the PWM mode. The output voltage showed a 5 mV change during mode switching.

Fig. 16 shows the results measured in order to verify the mode change and output voltage according to load current in auto mode.
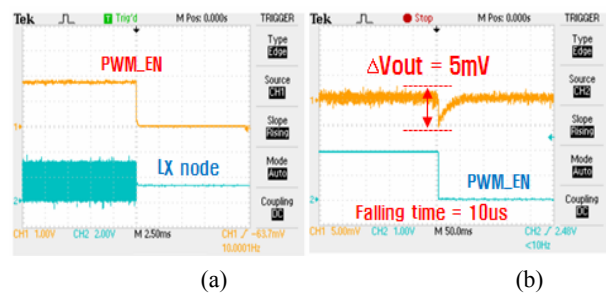

(a)   (b)

Fig. 14. PWM mode to linear mode.

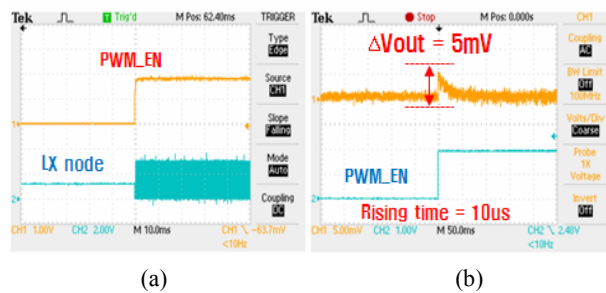(a)   (b)

Fig. 15. Linear mode to PWM mode.
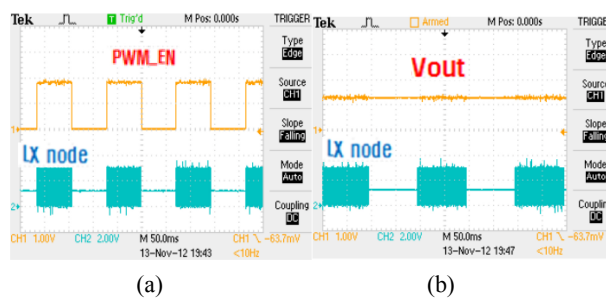

(a)   (b)

Fig. 16. Mode change in auto mode.

Figs. 17 and 18 show the changes in the rate of the output voltage according to the variation of the input in the PWM and linear modes.

Figs. 19 and 20 show the results of the output voltage indicating a rate of change due to the load variation in the PWM mode and in the linear mode. Line regulation and

load regulation were measured in a condition for which the mode could operate independently and the results of the measurement are shown in Table 1.

Fig. 21 show the results of the output voltage indicating a rate of change due to the load variation in the auto mode.
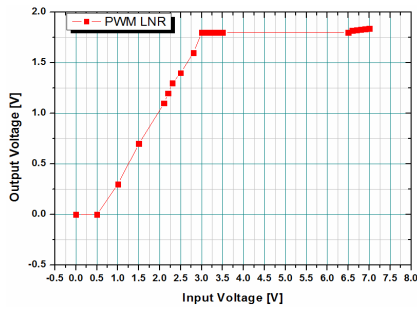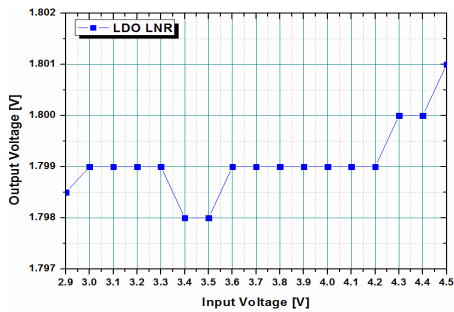

Fig. 17. PWM mode line regulation(@Vin=0~7 V).

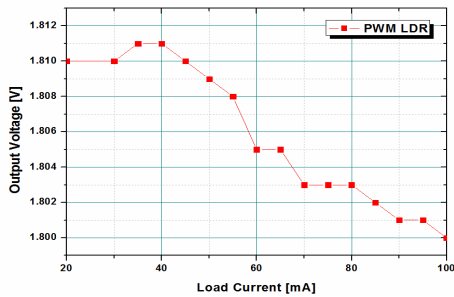**Fig. 18.** Linear mode line regulation(@Vin=2.9~4.5 V).
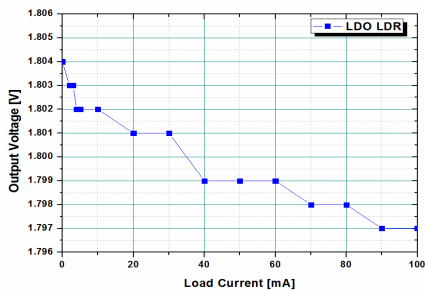

Fig. 19. PWM mode load regulation(@Iload=1~100 mA).
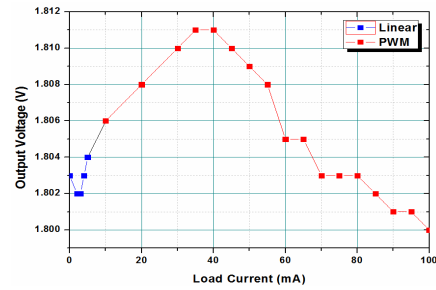

Fig. 20. Linear mode load regulation(@Iload=1~100 mA).
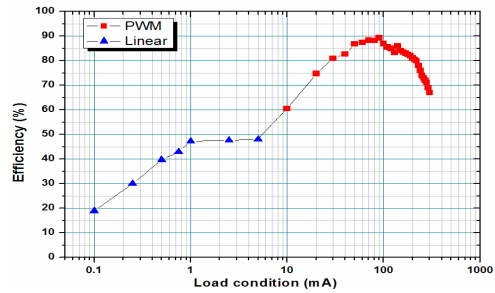

Fig. 21. Auto mode load regulation(@Iload=1~100 mA).

Fig. 22. Efficiency.

Table 1. Summary

Parameter	Condition	Min	Typical	Max
Supply Voltage	Vout=1.8 V	2.7 V	3.6 V	6.5 V
Quiescent current PWM mode			600 uA	800 uA
Quiescent current Linear mode			70 uA	
Line Regulation (PWM mode)	Vin=3.1~6.5 V Vout=1.8 V Iout = 60 mA		≤5 mV	
Line Regulation (Linear mode)	Vin=2.7~4.5 V Vout=1.8 V Iout = 60 mA		≤5 mV	
Load Regulation (PWM mode)	Vin=3.6 V Vout=1.8 V Iout=1~100 mA	0.8%	1.3%	1.8%
Load Regulation (Linear mode)	Vin=3.6 V Vout=1.8 V Iout=1~100 mA	0.1%	0.2%	0.35%
PWM switch ON-resistance	Vin=3.6 V Idrain=100 mA	0.18Ω	0.22 Ω	0.3 Ω
Oscillator frequency			1.8 MHz	
LDO dropout voltage			78 mV	
Output voltage noise			2.5 mV	5 mV
Over-temperature shutdown			130 ℃	
Over-temperature hysteresis			20 ℃	

Fig. 22 shows a graph of the results of the measured efficiency. To specify the efficiency measurement, the load current was changed from 100 μA to 300 mA at Vin=3.6 V and Vout=1.8 V.

Under a light load, the LDO regulator shows a higher efficiency than the switching regulator with PWM. Under a heavy load, on the contrary, the switching regulator shows a higher efficiency than the LDO regulator.
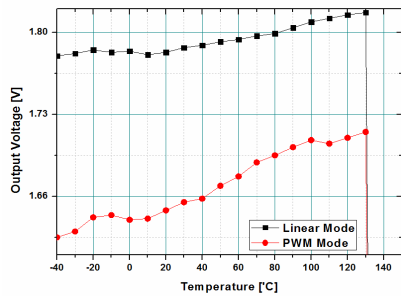
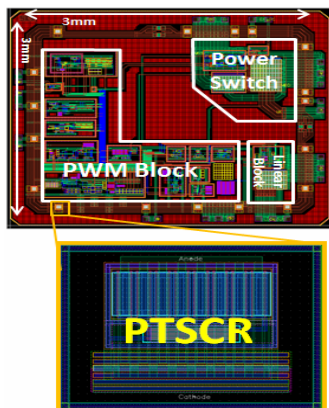**Fig. 23.** Temperature measurement of output voltage.

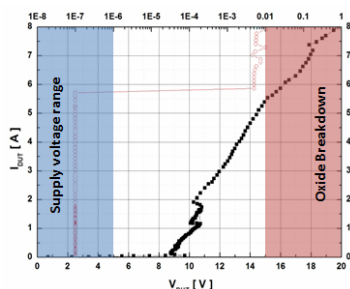**Fig. 24.** Layout of proposed DC-DC converter.

Fig. 25. Chip level TLP I-V curve.

A higher efficiency can be achieved by increasing the output voltage against the input voltage and the maximum efficiency is obtained at Vin=3.6 V and Vout=1.8 V of about 90%.

Fig. 23 shows the results of measurement of the temperature produced on the chip in the range from -40 °C to 140 °C. The measurement indicated that in the PWM mode, a change of 88 mV was observed between -40 °C and 140 °C at a rate of change of 0.5 mV/°C. Furthermore, in the linear mode a change of 44 mV was observed at a rate of change of 0.24 mV/°C. In addition, the circuit switches off at 130 °C due to the thermal shutdown block inside of the circuit that is meant to protect the circuit from high temperatures. Fig. 24 shows

the layout of the proposed converter and the total area that contains the seal-ring is about 3 mm $\times$ 3 mm.

Fig. 25 shows the chip-level TLP I-V curve of the ESD protection circuit that was produced by embedding in the proposed regulator. The PTSCR has a holding voltage of 8.3 V and a trigger voltage of 9.69 V, which are both higher than the supply voltage of the proposed LDO. Furthermore, it had a 5.4 A current drive capacity and showed an 8 kV tolerance in the HBM test on the PCB board. Table 2 shows the specification of designed ESD protection circuit.

Table 2. Specification of ESD protection circuit

Trigger Voltage	9.69 V
Holding Voltage	8.3 V
It2	5.4 A
Robustness (I_{load}0~100 mA)	HBM 8 kV

V. Conclusions

This paper proposes a high-efficiency dual-mode PWM / linear buck converter with a wide-input range. The reason for using the auto-mode is to change the mode automatically according to the load current in order to achieve high efficiency. In 5 mA or more, the efficiency of the PWM relatively high and the efficiency of the LDO relatively high in less than 5 mA. So, the mode is converted when 5 mA by sensing the load current.

Also, the input voltage is supplied from the LDO regulator during PWM operation to guarantee stability for a variation of the input voltage and over a wide-input range. As a result, the line regulation characteristics are improved. The proposed buck converter was fabricated using a Dongbu Hitek 0.18 µm CMOS process. Also, the proposed buck converter is used in the current-mode and has a switching frequency of 1.8 MHz, inductance of 4.7 µH and capacitance of 4.7 µF. In addition, an 8kV(chip level) ESD protection circuit of a P-substrate triggered SCR structure was designed and embedded to improve the latch-up the problem due to the low holding voltage of the conventional SCR structure.

Finally, measurement is performed separately in order to obtain a more accurate experimental data for a change. In order to see the line regulation in auto mode, for example, voltage and current have to be changed together. If the two elements are changed together, changing of the two elements are same to perform the LNR and LDR together. Changing of the two elements may occur in an

unexpected malfunction due to the increase of the elements involved in the characteristic. So, this paper is proceeded with several measurements in each mode.

REFERENCES

[1] Chi Yat Leung, "An Intergrated CMOS Current-Sensing Circuit for Low-Voltage Current-Mode Buck Regulator." IEEE Transactions on, Vol.52, pp. 394-397, July.2005

[2] Cheung Fai Lee, "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique." IEEE, Vol.39, pp. 3-14, Jan.2004

[3] Feng-Fei Ma, Wei-Zen Chen, "A Monolithic Current-Mode Buck Converter With Advanced Control and Protection Circuits" Power Electronics, IEEE,Vol.22 pp. 1836-1846, Sept. 2007

[4] Zhang Bin, "A novel thermal-shutdown protection circuit" ASID 2009, pp. 535-538, Aug.2009

[5] Chao Zhang, Zhijia Yang, "A CMOS hysteresis undervoltage lockout with current source inverter structure" ASICON 2011, pp. 918-921, Oct.2011

[6] Zhao Fangla, "An undervoltage lockout of hysteretic threshold of zero temperature coefficients" APMC 2005, Vol.2, Dec.2005

[7] Angkititrakul. S, "Design and analysis of buck converter with pulse-skipping modulation" PESC 2008. IEEE, pp. 1151-1156, June.2008

[8] Ahmed Emira, "DC-DC Converter with ON-Time Control in Pulse-Skipping Modulation" Circuits and Systems (ISCAS), pp. 2746-2749, June.2010

[9] J.B. Jia and K.N. Leung, "Integrated ramp generator with auto-set hysteretic comparator for PWM voltage regulators" Electronics Letters ,Vol.43, pp. 1384-1385, Nov.2007

[10] Junsoo Park, "A Design of Peak Current-mode DC-DC Buck Converter with ESD Protection Devices" IKEEE, Vol.17, pp. 77-82, Mar.2013

[11] Sao-Hunh Lu, "A Fast-Recovery Low Dropout Linear Regulator for Any-Type Output Capacitors" ASSCC 2005, pp. 497-500, Nov.2005

[12] Yangkook Ahn, Hyunseok Nam, "A 93.5% Efficiency, 400-mA Current-Mode DC-DC Buck Converter with Watchdog Functions" ISOCC 2009 , pp. 428-431, Nov.2009

[13] Wan-Rone Liou, Mei-Ling Yeh, "A High Efficiency Dual-Mode Buck Converter IC For Portable Application" Power Electronics, IEEE, Vol.23, pp.667-677, Mar.2008

[14] Hora, J.A., Jiun-Chang Zeng, "Asynchronous dual-mode buck converter design with protection circuits in 0.18um CMOS process for battery applications" ASIC 2009, ASICON '09, pp. 1314-1317, Oct.2009

[15] Bi, Zhuo, Xia, Wenbin, "A PWM/PFM switch technique of dual-mode buck converter" CCWMC2009, IET International Communication Conference, pp. 357-360, Dec.2009

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