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D-band Stacked Amplifiers based on SiGe BiCMOS Technology

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***Abstract*—This paper presents two 3-stage D-band stacked amplifiers developed in a 0.13-μm SiGe BiCMOS technology, employed to compare the conventional cascode topology and the common-base (CB)/CB stacked topology. AMP1 employs two cascode stages followed by a CB/CB stacked stage, while AMP2 is composed of three CB/CB stacked stages. AMP1 showed a 17.1 dB peak gain at 143.8 GHz and a saturation output power of -4.2 dBm, while AMP2 showed a 20.4 dB peak gain at 150.6 GHz and a saturation output power of -1.3 dBm. The respective power dissipation was 42.9 mW and 59.4 mW for the two amplifiers. The results show that CB/CB stacked topology is favored over cascode topology in terms of gain near 140 GHz.**

***Index Terms*—Cascode, stacked, common emitter, common-base, D-band, SiGe HBT**

I. INTRODUCTION

The increasing interests towards frequency bands beyond 100 GHz boost motivations for various applications including broadband communication and imaging. Typically, the increased frequency provides improved performance and enables new functionalities. Amplifiers are a key component for the systems operating at such raised frequency bands. Owing to recent advances in the operation speed of Si-based semiconductor devices, there have been growing reports on amplifiers operating beyond 100 GHz based on Si CMOS or SiGe HBT technologies. For the amplifiers operating at this band based on SiGe HBT technology, cascode topology has been a popular choice [1, 2]. On the other hand, recent reports on common-base (CB) topology reveals that it exhibits larger power gain than common-emitter (CE) topology particularly at higher frequency bands [3, 4]. Based on these results, it can be naturally envisioned that CB/CB stacked topology may outperform cascode (i.e. CB/CE stacked) topology with a similar bias level if properly optimized, while maintaining the advantages of the stacked topologies. This study is intended to experimentally compare the performance of CB/CB stacked topology and cascode topology for D-band amplifiers based on SiGe BiCMOS technology.

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II. CIRCUIT DESIGN

Fig. 1 compares the MSG (Maximum Stable Gain) and MAG (Maximum Available Gain) for the CB and CE topology, which are obtained from the device model of the actual device used for the circuits in this work. It indicates that the CB topology shows higher gain for $f>$ ~50 GHz for this particular device, leading to expectation of higher performance for the CB/CB stacked topology compared to the conventional cascode topology.

In this work, two 3-stage amplifiers were developed for comparison of cascode and CB/CB stacked topologies. The schematics of the amplifiers, respectively denoted as AMP1 and AMP2, are shown in Fig. 2. For AMP1, the first two stages are based on cascode

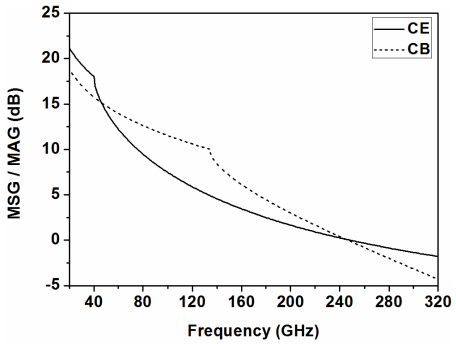
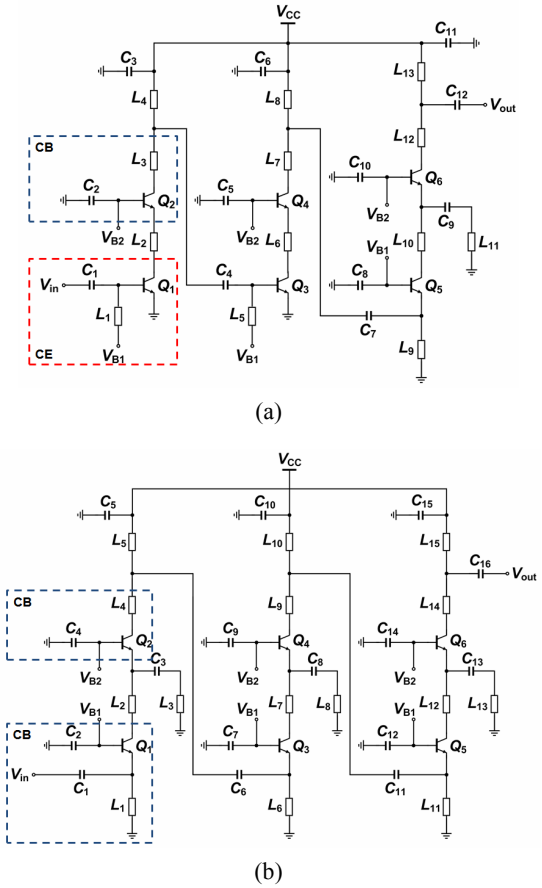


Fig. 1. Simulated MSG/MAG of the CB and CE topology.

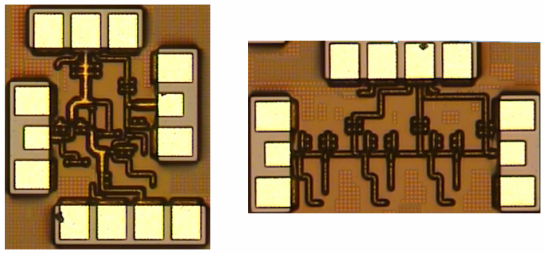


(a)

(b)

Fig. 2. Circuit schematics (a) AMP1, (b) AMP2.

topology while the last buffer stage is based on CB/CB stacked topology. AMP2 employs CB/CB stacked topology for all three stages. For the actual implementation of the CB/CB topology, an additional matching network was inserted between the top and bottom devices in order to further increase the total gain, which is composed of a series transmission line and a short stub connected in series with a capacitor. Also for the cascode stage, a series transmission line was inserted between the top and bottom devices for improved gain, which will lead to a fair comparison. Interstage matching between the individual stages as well as the input and output matchings were carried out for conjugate matching based on series transmission lines and stubs. 50 ohm microstrip lines were employed for the transmission lines and stubs. Blocking and bypass capacitors were realized with metal-insulator-metal (MIM) capacitors provided from the foundry.



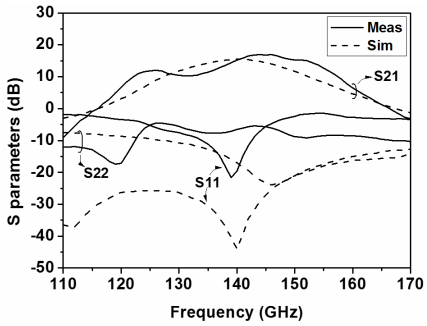
(a) (b)

Fig. 3. Die photographs of the fabricated amplifiers (a) AMP1, (b) AMP2.

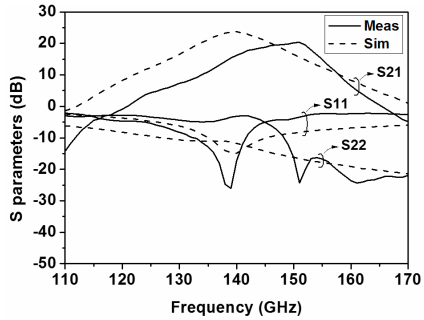
III. MEASUREMENT RESULTS

The two amplifiers were fabricated in a 0.13 μm SiGe BiCMOS technology that shows an f_{max} of ~245 GHz from the device model. The die photographs of the fabricated circuits are shown in Fig. 3. The chip sizes of AMP1 and AMP 2 are 475 × 610 μm^2 and 736 × 425 μm^2, respectively, including the DC and RF pads.

The measured and simulated S-parameters of the amplifiers are shown in Fig. 4. The measured data were obtained by an Agilent E8361A PNA network analyzer through OML D-band extender modules. As indicated by the measured S_{11} and S_{22}, the inputs are nicely matched near the target frequency of 140 GHz, but the output matchings were shifted for both amplifiers, leading to overall shifts of the gain profiles. The peak gain of AMP1 was measured as 16.9 dB at 143.8 GHz, while that of AMP2 was 20.3 dB at 150.6 GHz. The higher peak gain achieved with AMP2 indicates that CB/CB stacked topology shows higher gain than cascode stage as expected. The measured 3-dB bandwidth was larger for AMP1, which showed 16 GHz, slightly wider than 12 GHz for AMP2. The simulated results show some differences compared to the measured data, which can be expected due to the lack of model accuracy at high

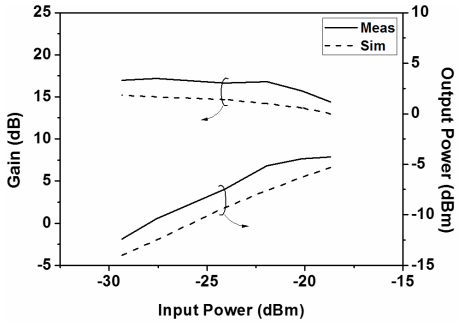


(a)

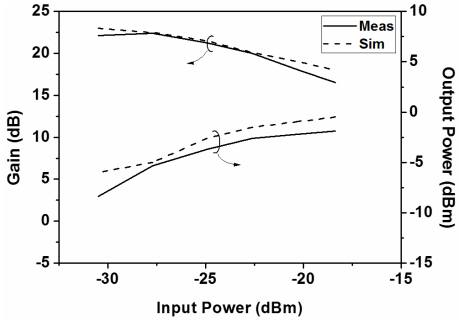


(b)

Fig. 4. Measured and simulated S-parameters (a) AMP1, (b) AMP2.



(a)



(b)

Fig. 5. Measured and simulated linearity properties (a) AMP1, (b) AMP2.

frequencies. Still, the overall trend of the simulation agrees to the measurement.

Linearity measurements were also carried out based on a D-band signal source, composed of a Quinstar tripler driven by an Agilent E8257D signal generator. An Erickson PM4 power calorimeter was used for output signal readout. An extra attenuator was attached to the tripler for input power level adjustment. The measured results are shown in Fig. 5. Simulation is also shown for comparison, which reasonably agrees with the measurement. A peak power gain of 17.2 dB and saturation output power of -4.2 dBm were achieved for AMP1, while 22. 4 dB and -1.3 dBm were measured for AMP2. All measurements were conducted under a bias condition of V_{CC} = 3.3 V, leading to power consumptions of 42.9 mW and 59.4 mW for AMP1 and AMP2, respectively.

IV. CONCLUSION

In this work, two 3-stage SiGe HBT amplifiers have been developed for comparison of CB/CB stacked topology and cascode topology near 140 GHz. From the measurement, the amplifier with three CB/CB stacked stages showed higher peak gain than the amplifier with two cascode stages followed by a CB/CB buffer. The results indicate that CB/CB stacked topology is favored over cascode topology in terms of the gain, which can be successfully applied to stacked amplifiers operating beyond 100 GHz.

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