JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.2, APRIL, 2015
http://dx.doi.org/10.5573/JSTS.2015.15.2.202
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

High-Robust Relaxation Oscillator with Frequency Synthesis Feature for FM-UWB Transmitters

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***Abstract*—A CMOS relaxation oscillator, with high robustness over process, voltage and temperature (PVT) variations, is designed in 0.18 µm CMOS. The proposed oscillator, consisting of full-differential charge-discharge timing circuit and switched-capacitor based voltage-to-current conversion, could be expanded to a simple open-loop frequency synthesizer (FS) with output frequency digitally tuned. Experimental results show that the proposed oscillator conducts subcarrier generation for frequency-modulated ultra-wideband (FM-UWB) transmitters with triangular amplitude distortion less than 1%, and achieves frequency deviation less than 8% under PVT and phase noise of –112 dBc/Hz at 1 MHz offset frequency. Under oscillation frequency of 10.5 MHz, the presented design has the relative FS error less than 2% for subcarrier generation and the power dissipation of 0.6 mW from a 1.8 V supply.**

***Index Terms*—Relaxation oscillator, high robustness, frequency synthesis, switched-capacitor, FM-UWB, subcarrier generation**

I. INTRODUCTION

Frequency-modulated ultra-wideband (FM-UWB) transmitters employ dual frequency modulation technique: FSK-modulated triangular subcarrier generation where triangular frequency f_1 represents data "0" and f_2 represents data "1"; followed by RF frequency modulation (FM) where the triangular amplitude voltage converted to UWB FM signal by using an RF voltage-controlled oscillator (VCO) with carrier frequency f_C calibrated [1, 2]. Hence, an oscillator having 2-FSK modulated triangular waveform output is indispensable.

The relaxation oscillators [3, 4] based on a slew-rate control by a timing capacitor and a charge-discharge current are good configurations to generate triangular waveform, with low complexity, power, noise and high linearity. However, oscillation frequency f_{OSC} encounters poor robustness over process, voltage and temperature (PVT) variations. Thus these oscillators need to work in a closed loop to conduct FSK-modulated subcarrier generation, which complicates the system design. Fig. 1 shows the block diagram of FM-UWB transmitters employing fractional-N phase-locked loop (PLL) with relaxation VCO for subcarrier generation [5, 6].

The existing oscillators [7-10] with temperature immunity lack enough consideration of, or are sensitive to process deviations. The existing oscillators [11-13] with good PVT robustness have large power dissipation in comparison to low oscillation frequency, which causes poor figure of merit (FOM) values. The existing

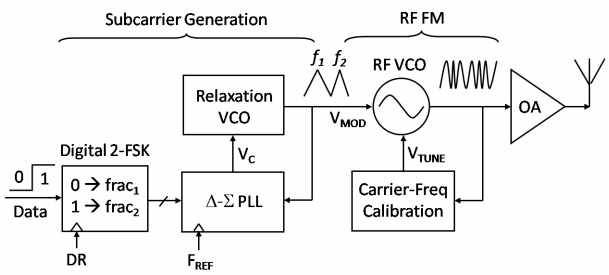

Fig. 1. Block diagram of FM-UWB transmitters.

Manuscript received Sep. 7, 2014; accepted Jan. 21, 2015
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oscillator [14] encounters slight f_{OSC} shift under power supply variations. Although these oscillators have better PVT feature than those [3-6], they either could not generate the desired triangular waveforms, or have no the frequency synthesis (FS) function, namely, f_{OSC} is not linearly tuned by a digital control signal. Hence, they are not perfect for 2-FSK triangular subcarrier generation.

In this paper, a relaxation oscillator consisting of full-differential charge-discharge timing circuit and switched-capacitor (SC) based voltage-to-current (V-to-I) conversion is proposed, which generates both triangular and square waveforms with high frequency robustness, low triangular distortion and low phase noise. The proposed architecture could be expanded to a simple open-loop frequency synthesizer with output frequency digitally tuned, which greatly simplifies the 2-FSK subcarrier generation for FM-UWB transmitters.

II. ARCHITECTURE AND IMPLEMENTATION

Fig. 2 shows the proposed high-robust relaxation oscillator with FS feature. The SC array C_{OSC} is charged and discharged by the current mirrors M11-14 and the switches M1-2, all these together with M4-5 form the oscillation cell. The replica cell comprised of M3, M6, M10, M15 and an operational amplifier Y2, controls the effective load resistances of M4-5 to have the constant voltage swing between 0 and V_{SW} at nodes A and B. This inversely sets the fixed voltage swing between $V_T+\Delta$ and $V_{SW}+V_T$ at nodes Y and X. Here V_T and Δ are the threshold voltage and the minimum saturation voltage of M1-2, respectively. Strict match design between the oscillation and replica cells is required with the operation principle referred in [3].

The charge-discharge current I_{M11} (I_{M12}) is generated by a V-to-I converter consisting of M7, an equivalent resistor and an operational amplifier Y1. The equivalent resistor is implemented by a SC module comprised of a capacitor C_{REF} and switch transistors S_{1-2}, controlled by a two-phase non-overlapping clock with the frequency F_{REF}. Large bypass capacitor C_{F3} and low-passed filters (LPFs) consisting of R_{F1-2} and C_{F1-2} with low cut-off frequencies are employed to suppress the switching ripple caused by the clock.

To get the triangular waveform output from the differential constant-current charge-discharge nodes X and Y across C_{OSC}, an operational amplifier Y3 with class-AB output stage and shunt-shunt feedback configuration is designed in the oscillator buffer. To get the rail-to-rail square waveform output from the nodes A and B, a simple comparator is employed in the buffer. Both Y1 and Y2 use fold-cascode architecture with the capacitors C_{C1-2} for frequency compensation within respective loops.

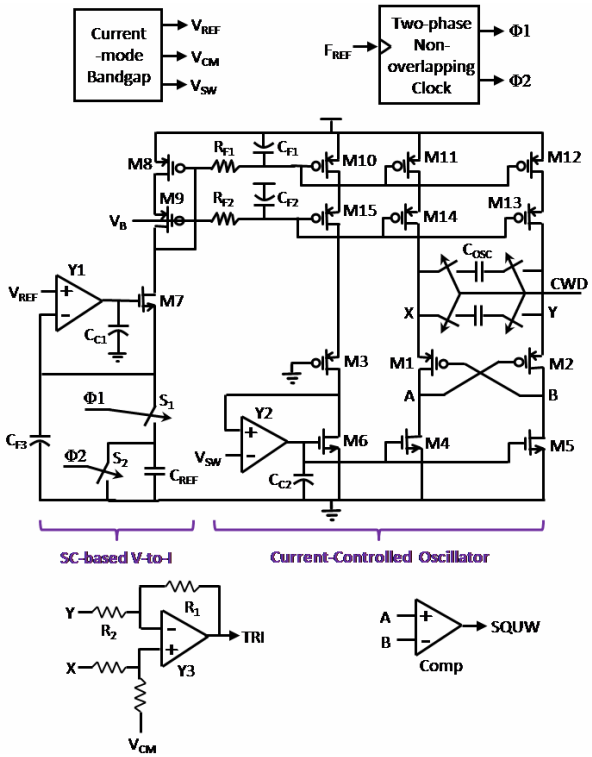

Fig. 2. Proposed FS-embedded high-robust relaxation oscillator.

Given the parasitic capacitor C_P in the node X (Y) and the size ratio K between M11-12 and M8, the oscillation frequency f_{OSC} is depicted in Eq. (1). Under PVT variations, f_{OSC} is set by K, V_{REF}/V_{SW}, C_{REF}/C_{OSC} and F_{REF}. Considering the strict match design among the cascode current mirrors and MIM capacitors (which means both K and C_{REF}/C_{OSC} constant), with V_{REF} and V_{SW} provided by a current-mode bandgap reference (which makes V_{REF} and V_{SW} robust over PVT to keep V_{REF}/V_{SW} constant) and F_{REF} generated by an external crystal oscillator (namely, F_{REF} is fixed), f_{OSC} thus has high robustness over PVT variations, when Δ and C_P are enough small in comparison to V_{SW} and C_{OSC}, respectively.

$$f_{OSC}=\frac{I_{M11}/(C_{OSC}+0.5C_p)}{2\left|(V_{SW}+V_T)-(V_T+\Delta)\right|}=\frac{KV_{REF}C_{REF}F_{REF}}{2(V_{SW}-\Delta)(C_{OSC}+0.5C_p)}$$
$$=\frac{K}{2}\frac{V_{REF}}{V_{SW}-\Delta}\frac{C_{REF}}{C_{OSC}+0.5C_P}F_{REF}\approx\frac{K}{2}\frac{V_{REF}}{V_{SW}}\frac{C_{REF}}{C_{OSC}}F_{REF}$$
$$\approx\frac{K}{2}\frac{V_{REF}}{V_{SW}}\frac{C_{unit}\times M}{C_{unit}\times N_{CWD}}F_{REF}\approx\frac{K}{2}\frac{V_{REF}}{V_{SW}}\frac{M}{N_{CWD}}F_{REF} \quad (1)$$

Considering the match design between the resistors R_1 and R_2, the oscillator buffer, which adjusts the amplitude rather than frequency of the triangular and square waveforms, has less effect on the robustness of f_{OSC} over PVT variations.

When C_{OSC} is digitally tuned by a control word (CWD) of N_{CWD}, f_{OSC} is digitally reconfigured and the proposed architecture thus performs open-loop FS function with low complexity. That is, different N_{CWD} produces different f_{OSC} with high robustness. When the CWD is single-bit representing the transmitted data, FSK-modulated triangular subcarrier is generated.

In this design with 180 nm CMOS, V_{REF}, V_{SW} and V_{CM} are respectively set to 0.6 V, 0.6 V and 0.9 V by the current-mode bandgap reference. The external reference clock F_{REF} is 3.2 MHz and the current-mirror ratio K is fixed to 25/4. Both C_{REF} and C_{OSC} are 8 pF under typical case and have 20~30% deviation under PVT. Δ is designed to 50 mV under typical case and varies with PVT. C_P has a typical value of 0.6 pF and varies with PVT and C_{OSC}. As a result, f_{OSC}=10.5 MHz is achieved under typical case.

Considering the inverse and minor effect of Δ and C_P, the frequency synthesis feature is depicted in Eq. (2). To ensure the linearity relationship between f_{OSC} and N_{CWD}, or to make the product of N_{CWD} and f_{OSC} constant, both Δ and C_P should be very small to reduce the FS error. Since Δ and C_P have poor robustness over PVT, the only method to ensure the FS feature is to decrease Δ and C_P simultaneously. The absolute and relative FS errors FS_{AE} and FS_{RE} are concluded.

$$f_{OSC}\approx\frac{K}{2}\frac{V_{REF}}{V_{SW}}\frac{M}{N_{CWD}}F_{REF}(1+\frac{\Delta}{V_{SW}})(1-\frac{C_p}{2N_{CWD}C_{unit}})\Rightarrow$$
$$N_{CWD}f_{OSC}(1-\frac{\Delta}{V_{SW}})(1+\frac{C_p}{2N_{CWD}C_{unit}})\approx\frac{K}{2}\frac{V_{REF}}{V_{SW}}MF_{REF}=C$$
$$\Rightarrow FS_{AE}\approx\frac{\Delta}{V_{SW}}-\frac{C_p}{2N_{CWD}C_{unit}}\qquad FS_{RE}\approx\frac{C_p}{2N_{CWD}C_{unit}} \quad (2)$$

Obviously, advanced fabrication process such as 65nm CMOS with smaller channel length and parasitic capacitor, achieves smaller Δ and C_P simultaneously, and thus better FS feature. In addition, larger C_{OSC} (N_{CWD}) contributes to smaller FS_{RE} with less C_p effect (C_p/C_{OSC}). For 2-FSK subcarrier generation, it is FS_{RE} rather than FS_{AE} that affects the effective frequency deviation between data "1" and "0". Therefore, FS_{RE} performance is more critical.

III. Experimental Results

The proposed architecture is implemented in 0.18 μm CMOS with active core area of 0.8 mm^2 and power dissipation of 0.6 mW from a 1.8 V supply, and is employed to the subcarrier generation for FM-UWB transmitters. With 10.5 MHz f_{OSC}, the FOM of 57 nW/kHz is achieved.

Fig. 3 shows the simulated transient oscillation waveforms with 10.5 MHz. The triangular waveform centered at 0.9 V (V_{CM}) with the peak-to-peak amplitude of nearly 0.55 V (V_{SW}−Δ), is generated by the voltage difference between nodes X and Y, which have voltage swings between V_T+Δ and V_{SW}+V_T. Triangular amplitude distortion less than 1% is observed and caused by the propagation delay of cross-coupled pair M1-2, which does not affect the flatten in-band property of the FM-UWB spectrum. The voltages of nodes A and B are clamped at 0 and V_{SW}, which are distinguishable for a common comparator to generate the rail-to-rail square waveform.

The simulated phase noise is –85 and –112 dBc/Hz at 100k and 1 MHz offset frequencies, respectively, greatly

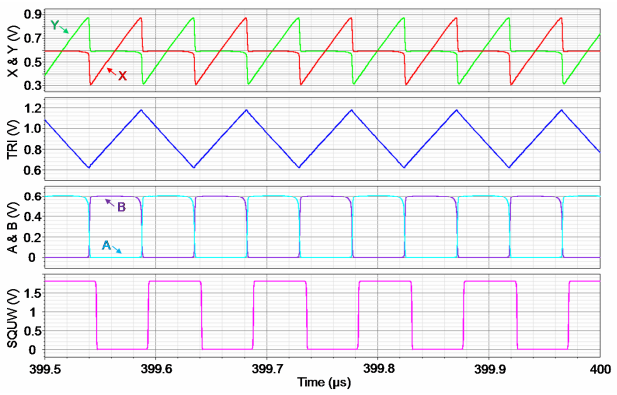

Fig. 3. Simulated transient oscillation waveforms.

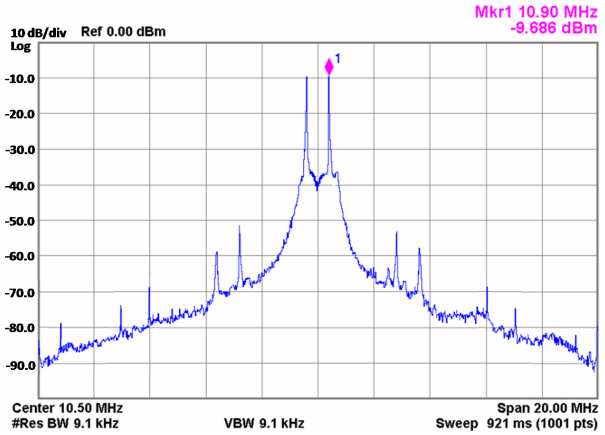

Fig. 4. Measured subcarrier spectrum for FM-UWB systems.

meeting the noise requirement (–80 dBc/Hz at 1 MHz offset frequency [1, 2]) of FM-UWB systems.

Fig. 4 gives the measured output spectrum of FSK-modulated subcarrier for FM-UWB systems. Two sidelobes at ±400 kHz offset frequency from the center frequency of 10.5 MHz are observed. Here 10.9 MHz triangular waveforms represent data "1" and 10.1 MHz ones represent data "0", with the equivalent C_{OSC} of 7.7 pF and 8.3 pF chosen by the single-bit CWD (transmitted data), respectively. The harmonics of reference clock (3.2 MHz) are introduced by the SC-based V-to-I conversion and observed with more than 44dB suppression.

Table 1 shows the simulated oscillation frequencies under PVT with various process corners (3σ), ±10% supply deviation and −40~120° temperature range. The frequency deviation of 7.6% is observed and caused by variable Δ and C_P, showing good robustness over PVT. Fig. 5 shows the measured oscillation frequencies under temperature and voltage deviations. The line sensitivity of 5%/V, the temperature coefficient (TC) of 900 ppm/℃ and the process corner accuracy of 1.9% are achieved, respectively. The proposed oscillator has high frequency robustness over process and voltage deviations, only is slightly sensitive to temperature variation. When advanced fabrication process such as 65 nm CMOS is employed, the frequency deviation will be less with better robustness.

Table 2 shows the simulated FS performance with f_{OSC} changing from 0.5 to 2 times, tuned by the CWD. The relative FS error due to C_P and absolute FS error by C_p and Δ are observed. From Eq. (2), the first item of the absolute FS error is larger than the second one, hence

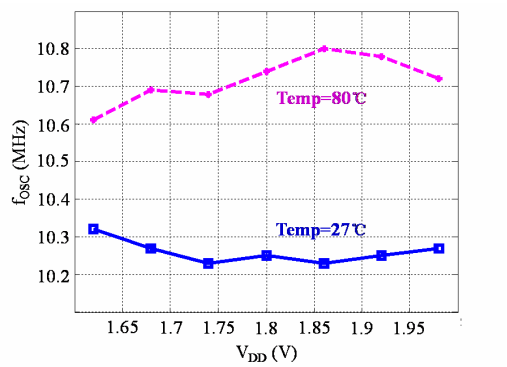

Fig. 5. Measured oscillation frequencies under temperature and voltage deviations.

Table 1. Simulated oscillation frequencies under PVT

PVT	tt/1.8V/27°	ss/1.8V/120°	ff/1.8V/120°	ss/1.8V/−40°	ff/1.8V/−40°
f_{OSC}	10.5MHz	11.3MHz	11.2MHz	9.8MHz	9.7MHz
PVT	tt/1.98V/27°	ss/1.98V/120°	ff/1.98V/120°	ss/1.98V/−40°	ff/1.98V/−40°
f_{OSC}	10.4MHz	11.1MHz	11.3MHz	9.9MHz	9.7MHz
PVT	tt/1.62V/27°	ss/1.62V/120°	ff/1.62V/120°	ss/1.62V/−40°	ff/1.62V/−40°
f_{OSC}	10.5MHz	11.2MHz	11.3MHz	10MHz	9.8MHz

Table 2. Simulated frequency synthesis performance

C_{OSC}	$0.5C_{REF}$	$0.75C_{REF}$	C_{REF}	$1.25C_{REF}$	$1.5C_{REF}$	$1.75C_{REF}$	$2C_{REF}$
Ideal f_{OSC} (MHz)	20	13.33	10**	8	6.67	5.71	5
Simulated f_{OSC} (MHz)	20.9	13.95	10.5*	8.44	7.08	6.1	5.38
FS_{AE} (%)	4.5	4.65	5	5.5	6.15	6.8	7.6
FS_{RE} (%)	4.2	3.6	3	2.3	2.1	1.5	

* Δ=0.05V, C_P=0.6pF, C_{OSC}=8pF @ typical case ** Δ=0, C_P=0, C_{OSC}=8pF @ ideal case

FS_{AE} increases with larger C_{OSC} due to smaller effect of C_p. However, the relative FS error FS_{RE} between two adjacent CWDs decreases with larger C_{OSC} due to the same smaller effect of C_p. Under 25% f_{OSC} variation, less than 4% FS_{RE} is achieved. For common subcarrier generators where smaller f_{OSC} range (≤10%) is required, the relative FS error is thus less than 2%. Such small error does not degrade 2-FSK modulation feature of the subcarrier generation. With reduced C_P and Δ under 65 nm CMOS, less FS errors will be achieved.

The performance of the proposed oscillator is summarized and compared to the existing designs in Table 3. The presented architecture achieves good trade-off between high f_{OSC}, good PVT robustness and low FOM value. With advanced process, the temperature coefficient, line sensitivity and corner accuracy could be further optimized with smaller Δ and C_P, as discussed above. In addition, the proposed design has the

Table 3. Oscillator performance summary and comparison

Ref.	Process	Supply (V)	f_{osc} (kHz)	Power (μW)	Line Sens. (%/V)	TC (ppm/℃)	Corner Acc. 3σ (%)	FOM (nW/kHz)
This work	180nm	1.8	10500	600	5	900	1.9	57
[7]	350nm	1.0	80	1.06	2.5	842	11.9	13.3
[8]	350nm	1.0	3.3	0.011	3.5	1000	20.7	1.9
[9]	65nm	1.2	12600	98.4	0.35	205	bad	7.8
[10]	180nm	1.8	1100	0.86	3.0	64.3	bad	0.8
[11]	65nm	1.05	100	41	0.1	100	1.1	410
[12]	350nm	1.2	200	84	0.14	900	0.7	420
[13]	60nm	1.6	32.8	0.005	0.125	32.4	N/A	138
[14]	90nm	0.8	100	0.28	9.7	105	N/A	2.8

embedded FS feature for subcarrier generation of FM-UWB transmitters.

IV. CONCLUSIONS

A high-robust relaxation oscillator with triangular and square waveform outputs is implemented in 0.18 μm CMOS for the subcarrier generation of FM-UWB transmitters. The proposed oscillator consists of full-differential charge-discharge timing circuit and SC-based V-to-I conversion. Experimental results verify that good frequency robustness, low triangular distortion, low phase noise, low power dissipation and embedded FS feature are achieved.

ACKNOWLEDGMENTS

This work is supported by the National Natural Science Foundation of China (61306037), Beijing Natural Science Foundation (4153063), and Basic Research Foundation of Beijing Institute of Technology (20130542009). This work is also supported by the China Scholarship Council (201406035016).

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