

80 μ W/MHz 0.68V Ultra Low-Power Variation-Tolerant Superscalar Dual-Core Application Processor

Youngsu Kwon, Jae-Jin Lee, Kyoung-Seon Shin, Jin-Ho Han, Kyung-Jin Byun, and Nak-Woong Eum

SoC Research Department, Electronics and Telecommunications Research Institute (ETRI) / Daejeon, Republic of Korea
{yskwon, ceicarus, shinks, soc, kjbyun, nweum}@etri.re.kr

* Corresponding Author: Youngsu Kwon

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Abstract: Upcoming ground-breaking applications for always-on tiny interconnected devices steadily demand two-fold features of processor cores: aggressively low power consumption and enhanced performance. We propose implementation of a novel superscalar low-power processor core with a low supply voltage. The core implements intra-core low-power microarchitecture with minimal performance degradation in instruction fetch, branch prediction, scheduling, and execution units. The inter-core lockstep not only detects malfunctions during low-voltage operation but also carries out software-based recovery. The chip incorporates a pair of cores, high-speed memory, and peripheral interfaces to be implemented with a 65nm node. The processor core consumes only 24mW at 350MHz and 0.68V, resulting in power efficiency of 80 μ W/MHz. The operating frequency of the core reaches 850MHz at 1.2V.

Keywords: Processor, Core, Low-power, Variation-tolerance, Superscalar, Application processor

1. Introduction

Emerging mobile device markets, such as the internet of things (IoT) and wearable devices, create ever-increasing demand for low-power processor cores. While the core at the heart of microcontroller units shows power consumption of several milliwatts, performance is limited to tens of millions of operations per second. Application processors in smartphones or tablets operate at several gigahertz to run heavy operating systems, such as Android, drawing several thousand milliwatts. The processor core in the era of the IoT and wearable devices is forced to provide performance of several thousand operations per second with a power budget comparable to that of microcontrollers for continuous activation over days or months.

Commercial application processor cores pursuing only performance maximization have lots of complex *fill-rate-sustaining structures* (FRS) including register renaming, reorder buffers, and instruction fetch speculation units [1]. A deeply pipelined processor core focusing on throughput enhancement necessitates implementation of a power-hungry FRS to sustain the instruction fill rate in pipeline stages of the core. However, the technology scaling wall in

nodes over 14nm puts limits on fanout-of-4 (FO4) delay reduction. The lower bound on logic delay imposes a performance limit on the FRS, as well as instruction sequencing and execution units. It indicates that a more complex FRS provides a much smaller return in terms of performance-sacrificing power efficiency. Re-architecting of the processor core is required for the upcoming era of low-power devices.

Low supply voltage to a processor core is one of the driving factors for achieving extreme low-power devices. The sub-threshold operation of application-specific logic or an Intel architecture, 32-bit (IA-32) core, operating at near-threshold voltage, shows the prospective power benefits of low-voltage operation [2, 3]. Low voltage operation of the processor core incurs two limiting factors. First, a processor core operating at a low supply voltage inherently exhibits degraded performance caused by the increased FO4 delay. The increased delay pushes the operating frequency to the lower bound, resulting in low-performance devices. Second, the static and dynamic variation in deep-submicron technology combined with reduced noise immunity in transistors causes instability in processor core operations.

The manufacturing-induced static parameter variation

in circuits of a processor core changes from die to die. A dynamic variation occurs during processor operations by changing environmental conditions, such as temperature, voltage fluctuation, irregular current induction, and various workload distributions in the time-domain. The performance monitoring circuit prevents operational failure of the processor core. Jain et al. [3] employed variation-aware pruning of standard cells for reliable low-voltage operation. Das et al. [4] proposed the shadow latch with meta-detector to identify circuit failures. A performance monitor, such as tunable replica circuits presented by Raychowdhury et al. [5] is a widely adopted technique to enable time-domain scaling of operating voltage and frequency.

In this paper, we propose a novel superscalar dual-core processor called Aldebaran for high-performance low-power applications. We designed the microarchitecture and Register-Transfer-Level (RTL) code of the Aldebaran core from the ground up to achieve high performance while minimizing power consumption. The contributions of this paper are summarized as follows. First, we designed a dual-issue superscalar processor core with an intra-core low-power architecture using a ground-up approach. Second, a novel inter-core lockstep architecture for reliable low-voltage operation is proposed. Periodic activation of an inter-core lockstep enables the Aldebaran core to sustain stable operation under dynamic variations, such as environmental and workload condition changes accompanied by low supply voltage.

This paper is organized as follows. Section 2 discusses the internal low-power microarchitecture of the Aldebaran core, and Section 3 presents the inter-core lockstep architecture. Chip implementation and measurement results of Aldebaran integrating cores, memory and peripheral interface intellectual property (IP) are presented in Section 4, with concluding remarks in Section 5.

2. Intra-Core Low-Power Architecture

Aldebaran is a 32-bit superscalar processor of which the internal microarchitecture is built for low-voltage high-performance operation. The overall microarchitecture is shown in Fig. 1 with simplified architectural details. The 13-stage pipeline is composed of three sub-cores: instruction fetch and branch prediction (IF), decode with queues (DEC), and execution (EX).

Acronyms and full names of hardware units in Fig. 1 are summarized in Table 1. The IF sub-core accesses the instruction cache to fill the instruction queue (IQ). The DEC sub-core is composed of dual-rail decode data paths, where each path reads an instruction from the IQ, decodes it, and stores the decoded signals in the execution queue. The EX sub-core fetches decoded instructions from the EQ, reads operands from the register file, and executes instruction operations in parallel with two-way integer units, the load-store unit, and the floating-point unit.

The virtual address (VA) computation in the IF sub-core produces the virtual address of instructions to be fetched. The four-way set-associative instruction cache (iS) is composed of i-Tag (tag memory), and i-Data (data

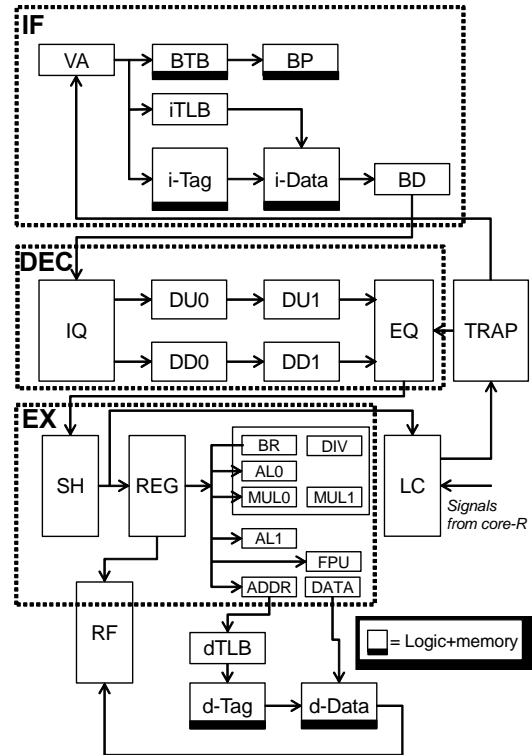


Fig. 1. Microarchitecture of Aldebaran.

Table 1. Acronyms and full names of units.

Acronym	Full name
VA	Virtual Address computation
BTB	Branch Target Buffer
BP	Branch Predictor
i/d TLB	Instruction/Data address Translation Look-aside Buffer
BD	Branch pre-Decision
IQ	Instruction Queue
DU, DD	Decoder-Up, Decoder-Down
EQ	Execution Queue
SH	Scheduler
REG	Register File
LC	Lockstep Controller
BR, DIV	BRanch unit, integer DIVider
AL, MUL	Arithmetic-Logical unit, Multiplier
TRAP	Trap (interrupt) controller

memory), which contain cache lines. The virtual address is fed to i-Tag to check if the requested cache line exists in i-Data. The instruction address translation look-aside buffer (iTTLB) translates the virtual instruction address into the physical address. The cache line where the address matches the physical address is fetched into the instruction queue if i-Tag confirms a cache hit. The sequence of iS access is repeated at every cycle in a pipelined way. iS access accounts for a large portion of the power consumption as bit line charging and discharging in memory blocks is done during every access. The branch

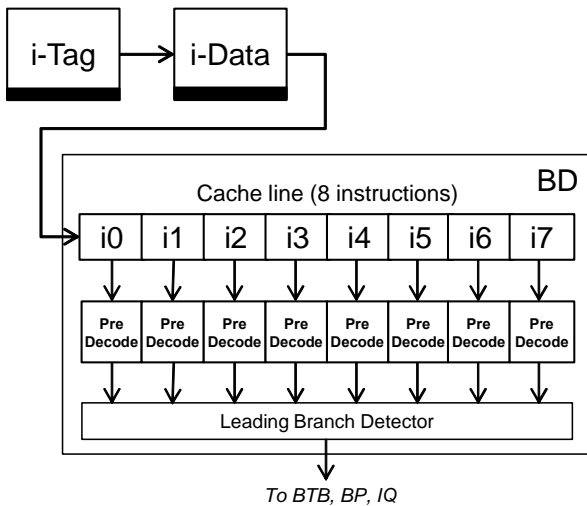


Fig. 2. Architecture of BD (Branch pre-Detector).

prediction architecture, which is composed of the branch target buffer (BTB) and the branch predictor (BP) is another source of power consumption. The BTB stores branch target addresses in two-way 58-bit 256-entry memory. The BP is implemented with a two-bit 4096-entry memory array where two bits indicate the taken history for each target address.

The branch pre-decision (BD) unit minimizes the access frequency of IS as well as that of the BTB and the BP. The internal architecture of the BD is shown in Fig. 2. The cache line read from i-Data contains eight 32-bit instructions. In Fig. 2, i0 ~ i7 are instructions read from i-Data on the same cache line. In the Aldebaran core, only three bits of instruction at a higher bit position are sufficient to identify a branch instruction. The pre-decoder unit attached to each instruction locates the branch instruction by decoding each of the higher three bits. The leading branch detector identifies where the first branch instruction is. If the branch instruction is at i5, the IQ fetches all of i0 ~ i4 into some of its 24 instruction slots. In a subsequent cycle, the branch instruction i5 and the following delayed instruction, i6, are sent to the BTB and the BP for branch prediction. These instructions are also put into the following slots in the IQ.

Simultaneous single-cycle fetching of instructions in the same cache line enables sporadic activation of IS resulting in power reduction. The leading branch detection in the BD also relieves the IQ of logic overhead, storing instruction addresses as all instructions fetched into IQ are actually executed, if branch prediction is correct. Upon branch mis-prediction found during the execution stage, the IQ is cleared. Branch instruction identification in the BD also allows sporadic activation of the BTB and the BP to save power. Memory accesses in the BTB and the BP occur only when there is a branch instruction in the cache line fetched in the previous cycle.

Decoder-up (DU) and decoder-down (DD) pop, at most, one instruction each from the IQ, decode them, and store the decoded information in the EQ, which is composed of eight slots. The scheduler (SH) schedules the dispatch timing and the sequence of decoded instructions in the EQ.

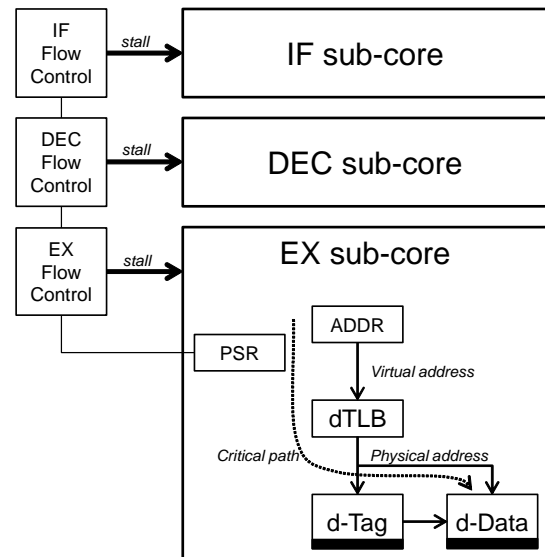


Fig. 3. Flow control under low-voltage operation.

The in-order dispatching of instructions into the EX sub-core discards introduction of complex interconnection wires required in reservation stations or register renaming units resulting in area and power savings.

An instruction flow through the pipeline is stalled by hazards caused by register dependencies among instructions. The separation of the Aldebaran core into sub-cores, IF, DEC, and EX enables independent control of instruction flow. The IQ between the IF, and the DEC and the EQ between the DEC and the EX implement this separation. Flow control independence in the Aldebaran core adjusts the performance during low-voltage operation, as shown in Fig. 3. The critical path in the Aldebaran core lies on the units composed of D cache (D\$) address computation, dTLB for physical address translation, and access to d\$. As the operating voltage decreases, the increased delay on the critical path may cause malfunction of the core. In the Aldebaran core, compensation for increased delay is done by setting up a processor state register (PSR). The specific bit in the PSR stalls the EX sub-core for a single cycle only when the load-store instruction is executed under low supply voltage. Performance degradation by single-cycle stall is negligible by virtue of in-time stall as well as flow control independence.

3. Inter-Core Lockstep for Reliability

Increased delay by lowering the supply voltage may cause incorrect operation of the processor core. A pre-constructed table denoting the frequency-voltage relation is useful in controlling voltage and frequency for a required workload performance. However, static and dynamic variation in operating conditions alters the frequency-voltage relation from the initial voltage-frequency table. Research by Bowman et al [7] and Karpuzcu et al [8] presents techniques to detect timing failures while increasing the operating frequency of the

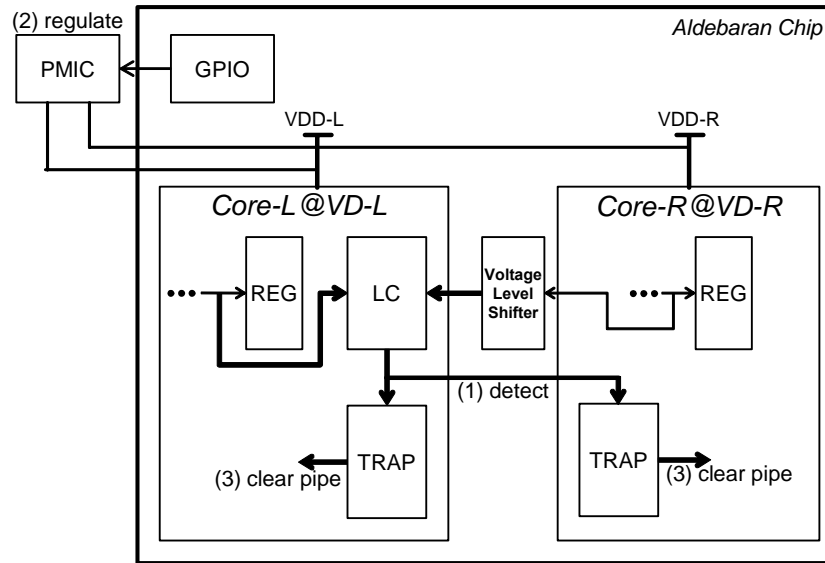


Fig. 4. Per-core voltage domain for Inter-Core lockstep.

processor. The error detection sequential circuits and tunable replica circuits report timing violation occurrences. Upon the occurrence of timing errors, the core restarts from the instruction already safely completed, and the adjustable clock distribution network sustains continuous correct functionality.

Inter-core lockstep is a technique to ensure correct operation of the Aldebaran core for a given operating voltage. The dual-core on the Aldebaran chip is for parallel workload execution. An appropriate configuration of cores enables the inter-core lockstep, with the architectural view shown in Fig. 4.

We implemented a per-core voltage domain where the power grid of the core is separated from the other core. Core-L is the ‘first’ core with supply voltage of VDD-L, and Core-R is the ‘second’ core with VDD-R. The lockstep controller (LC) compares both input and output signals of the register file (REG) from Core-L with voltage-shifted signals from Core-R. The mismatches in the signal output indicate that the behavior of Core-L deviates from that of Core-R. This acts as evidence that incorrect functionality has occurred during the operation.

The inter-core lockstep ensures reliable low-voltage operation with dynamic voltage adjustment. It exploits the actual core and workload to search for the optimal supply voltage. After power-on reset of each core, the power manager of the operating system (OS) assigns nominal operating voltage (HV), 1.1V, to each core. An OS kernel thread starts in Core-L at HV. The OS thread scheduler may assign another thread or workload to Core-R. The thread assignment to the core initiates the voltage adjustment process shown in Fig. 5.

During the operation, remember that each core is processing its own thread with the pre-assigned operating voltage. The OS then assigns a new thread to Core-R. The OS triggers a trap routine in Core-L to store the current state of Core-L in the stack. The trap routine assigns HV to Core-L while it sets lowest voltage (LV) to Core-R. It assigns the same thread to both Core-L and Core-R to

```

Core_Thread_Voltage_Assignment {
  Send Trap signal to Core-L;
  Assign HV to Core-L and Core-R;
  Assign a thread to Core-L and Core-R;
  do {
    Copy Core-L's PC to Core-R's PC;
    Detect_Failure = FALSE;
    Continue Core-L and Core-R
      for pre-determined time;
    If (LC reports 'failure detection') {
      Store PC and clear pipeline of cores;
      Increase Core-R's Voltage by  $\Delta V$ ;
    }
  } while (Detect_Failure == FALSE);
  Trap return for Core-L;
}

```

Fig. 5. Voltage adjustment.

detect a mismatch occurrence coming out of the LC if the mismatch occurs as the thread execution progresses. Low operating voltage combined with dynamic variation of operating conditions may cause incorrect operation in Core-R. The result of incorrect operation appears as ‘failure detection’ in the LC. Upon failure detection, the LC reports the failure to the Trap (interrupt) controller (TRAP). The trap routine stores the current PC (Program Counter) indicating the progress of the core, clears core pipelines to restart the cores, and increases Core-R’s operating voltage by ΔV . The amount of ΔV is in the range of 10mV. After increasing the operating voltage, the lockstep controller checks mismatches between signal outputs. If it is found out that there is no failure detected for a pre-determined time, thread execution continues in Core-R while Core-L reverts to its original thread before the voltage assignment process. The voltage assignment process is run periodically by the OS.

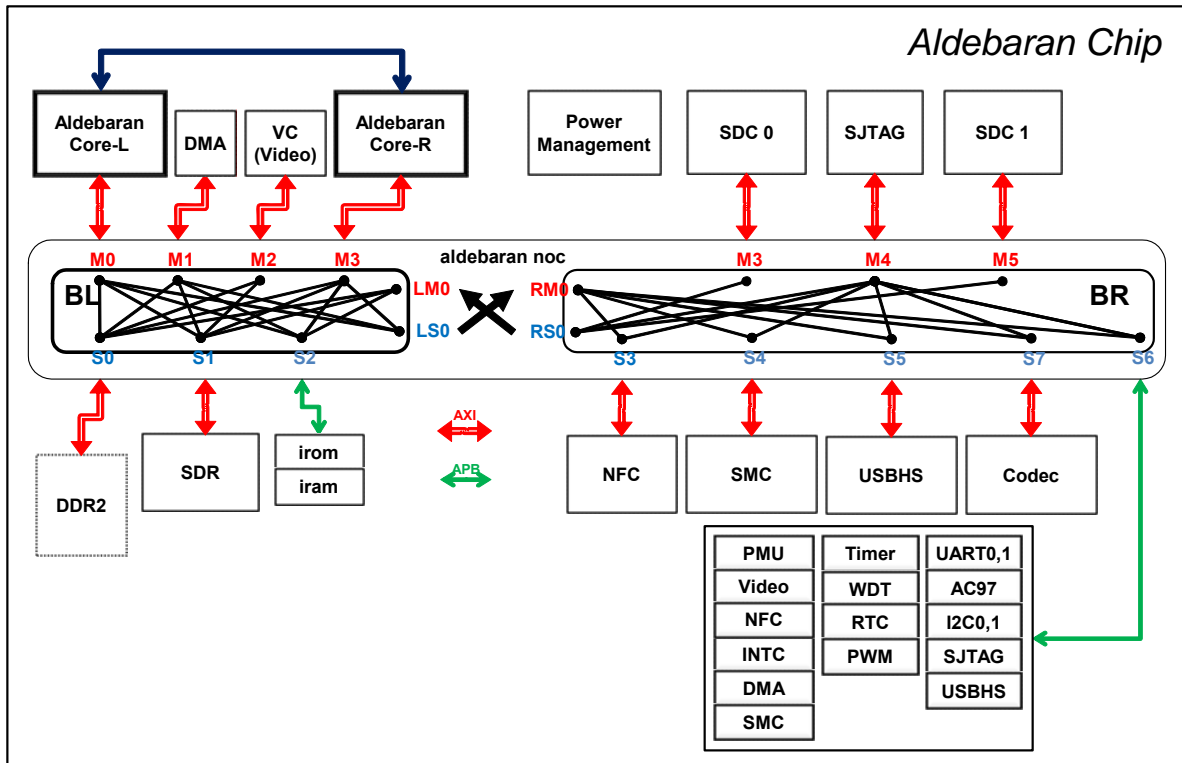


Fig. 6. Architecture of Dual-Core Aldebaran chip.

4. Implementation

The architecture of the Aldebaran chip is shown in Fig. 6. The chip incorporates dual Aldebaran cores, DMA (Direct Memory Access controller), video controller, USB (Universal Serial Bus), SDIO (Secure Digital Input/Output controller), and industry-standard peripheral IPs, and etc. required for the low-power application processor. The interconnection backbones are a 32-bit AXI on-chip bus for high-speed IPs and an APB (Advanced Peripheral Bus) for low-speed peripheral IPs. The Aldebaran Core-L operates under the voltage source separated from that of Core-R. The lockstep controller located in Core-L compares the input and output signals of Core-L with voltage-level shifted signals from Core-R.

The Aldebaran chip, fabricated with a 65nm node shown in Fig. 7, occupies an area of 2.4mm x 3.3mm, excluding pads. The area of the core is 2.65mm² including all sub-cores, 32KB I\$, 32KB D\$, iTLB (instruction Translation Lookaside Bus), and dTLB (data address Translation Lookaside Bus). The voltage level shifters around Core-R manipulates signal transfers between per-core voltage domains. The power management integrated circuit (PMIC) outside of the chip supplies the separated power grid of each core with a separate power source. The core is able to adjust the operating voltage in units of 10mV by finely controlling the PMIC through general purpose input/output (GPIO) interface. The power consumption breakdown obtained from the static power estimation tool (Synopsys PT-PX) shows that leakage power accounts for 57% of overall power consumption. It implies that the compact area of the Aldebaran core, which

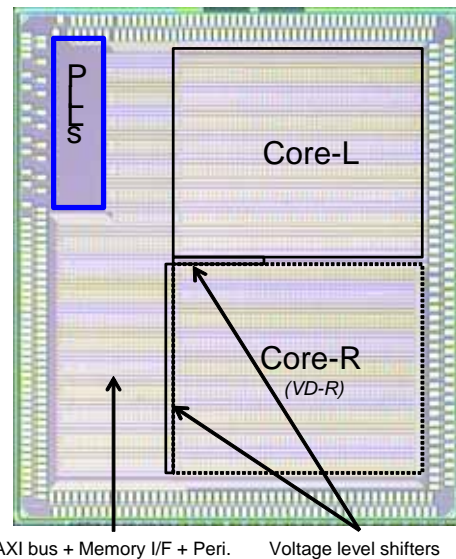


Fig. 7. Die microphotograph of Aldebaran Chip.

is about two-thirds of that of commercial cores, effectively reduces power consumption. While the architecture concentrates on saving power, it shows a normalized Coremark [6] score of 2.0, which is comparable to that of commercial cores (1.8~2.3). In summary, the Aldebaran architecture obtains comparable performance while it achieves sufficiently high power efficiency.

The actual chip measurement in terms of operating frequency and power consumption versus operating voltage of the core is shown in Fig. 8. The operating frequency rated on the left y axis in log scale linearly

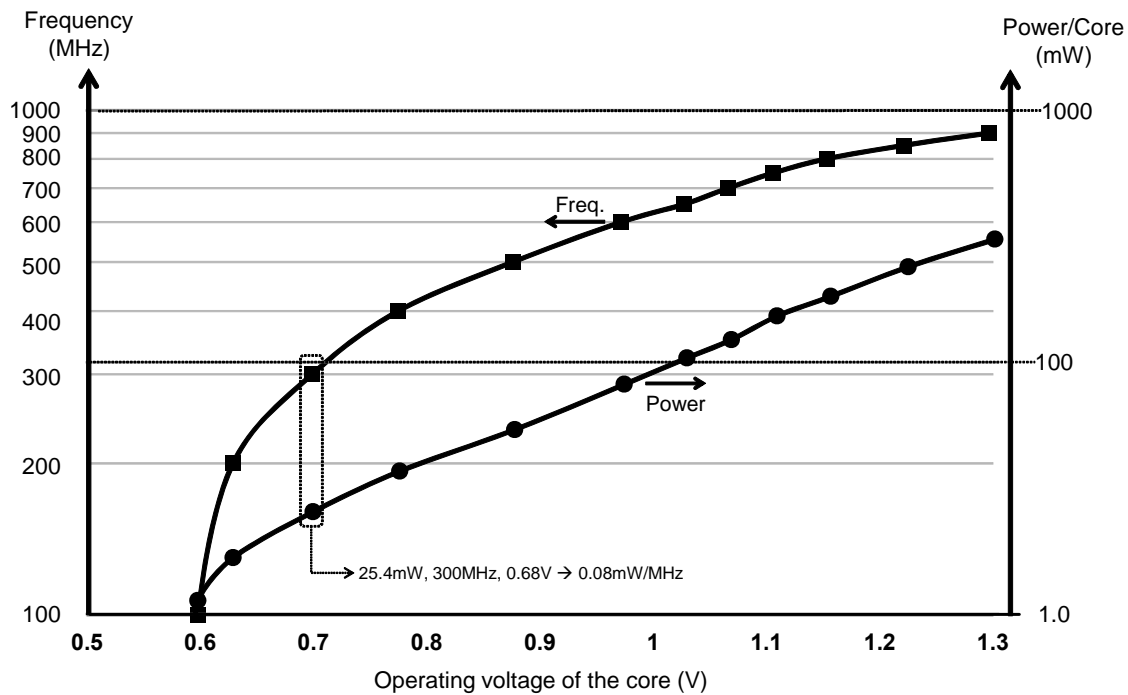


Fig. 8. Operating frequency and power vs. operating voltage.

increases in a voltage range of 0.7~1.3V. It indicates that the circuit delay decreases exponentially as the voltage increases. The rate of frequency enhancement slows down in the range of 1.0~1.3V while power consumption of the core also shows a steady linear increase. This degraded performance improvement with respect to linear power increase results in inferior power efficiency at a higher operating voltage. The power efficiency is the power that goes into unit performance. It is apparent that higher power efficiency is obtained at a lower voltage as the power decreases exponentially as the voltage scales down. The nominal frequency of Aldebaran reaches 850MHz at 1.2V, showing power efficiency of 0.24mW/MHz. The power efficiency of the proposed core is 65% better, compared to the 0.68mW/MHz nominal power efficiency of commercial embedded superscalar cores.

The Aldebaran core adjusts the operating voltage with minimum voltage offset to search for the lowest voltage satisfying current operating conditions and workload. Power consumption of the Aldebaran core at 0.68V is 25.4mW with an operating frequency of 300MHz, resulting in power efficiency of 80 μ W/MHz.

5. Conclusion

We propose the design and implementation of a 32-bit superscalar processor: the Aldebaran core. This intra-core low-power architecture achieves 0.08mW/MHz power efficiency at 0.68V. The novel inter-core lockstep with dynamic voltage adjustment ensures reliable low-voltage operation under static and dynamic variations in operating conditions.

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References

- [1] Y. Shin, et al., “28nm high-metal-gate heterogeneous quad-core CPUs for high-performance and energy-efficient mobile application processor,” Proc. of Int’l Solid-State Circuits Conference, pp. 154-155, 2013.
- [2] H. Kaul, et al., “A 320mw 56 μ W 411 GOPS/Watt ultra low voltage motion estimation accelerator in 65nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 44, no. 1, pp. 107-114, Jan. 2009.
- [3] S. Jain, et al., “A 280mV-to-1.2V wide-operating-range IA-32 processor in 32nm CMOS,” Proc. of Intl. Solid-State Circuits Conference, pp. 66-68, 2012.
- [4] S. Das, et al., “A self-tuning DVS processing using delay-error detection and correction,” IEEE J. Solid-State Circuits, vol. 41, no. 4, pp. 792-804, Apr. 2006.
- [5] A. Raychowdhury, et al., “Error detection and correction in microprocessor core and memory due to fast dynamic voltage droops,” IEEE J. on Emerging and Selected Topics in Circuits and Systems, vol. 1, no. 3, pp. 208-217, Sep. 2011
- [6] J. A. Poobey, et al., “A benchmark characterization of the EEMBC benchmark suite,” IEEE Micro, vol. 29, no. 5, pp. 18-29, 2009
- [7] K. A. Bowman et al., “Adaptive and resilient circuits for dynamic variation tolerance,” IEEE Design & Test, vol. 30, issue 6, pp. 8-13, 2013
- [8] U. R. Karpuzcu et al., “Coping with parametric

variation at near-threshold voltages,” vol. 33, issue 4, pp. 6-14, 2013



Youngsu Kwon received B.S., M.S., and Ph.D. degrees from Korea Advanced Institute of Science and Technology (KAIST), Republic of Korea at 1997, 1999, and 2004, respectively. He had been with Microsystems Technology Laboratory (MTL), Massachusetts Institute of

Technology as a Postdoctoral Associate from 2004 to 2005 for designing 3-Dimensional FPGA. He is now with System-on-Chip Research Department, Electronics and Telecommunications Research Institute (ETRI), Republic of Korea since 2005. In ETRI, he is leading the design of Korean CPU platform, Aldebaran, as a member of principal research staff. He has authored over 30 internal journal and conference papers with special interest in low-power processor core design, many-core architecture, VLSI CAD and algorithmic optimizations of circuits and systems. He received Excellent Researcher Award from Korea Research Council in 2013, Industrial Contributor Award from Korean Federation of SMEs in 2013, medals from Samsung Humantech Thesis Prize. The Aldebaran CPU core and Application processor for which he acts as a leading architect received Prime Minister’s Award from Korean Semiconductor Design Award in 2013.



Jae-Jin Lee received the B.S., M.S. and Ph.D. degrees in computer engineering from Chungbuk National University in 2000, 2003 and 2007, respectively. He is currently with the Multimedia Processor Research Section, Electronics and Telecommunications Research Institute, Daejeon,

Korea. His current research interests include the areas of application specific instruction set processor and compiler, and system-level multi-core emulation.



Kyoung-Seon Shin received his B.S. and M.S. degrees in electrical engineering from Chonbuk National University, Jeonju, Korea in 1989 and 1991, respectively. From 1991 to 1999, he worked at LG semiconductor Co.,Ltd, Korea. He has been with System-on-Chip Research Department,

Electronics and Telecommunications Research Institute (ETRI), Daejeon, Korea since 1999. His current research interests include the development of multimedia processor, multi-cores, low-power embedded processor.



Jin-Ho Han received the B.S. and M.S. degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Dae-jeon, Korea, in 1998 and 2001, respectively. From 2000 to 2001, he had worked at Korean System Integration and IP Authoring Research Center (SIPAC), Dae-jeon, Korea. Since 2001, he has been on the senior researcher of the System-on-Chip Research Department at Electronics and Telecommunications Research Institute (ETRI), Dae-jeon, Korea. His current research interests include energy scalable vector processor, multi-processor system-on-chip, low-power and resilient VLSI, and hardware acceleration for multimedia and recognition applications for humanistic intelligence systems.



Kyungjin Byun is the director of multimedia processor research section of Electronics and Telecommunications Research Institute (ETRI). He received his B.S. degree in electronics engineering from Kookmin University, Seoul, Korea in 1987 and his M.S. and Ph.D. degrees in information and telecommunications from Korea Advanced Institute of

Science and Technology (KAIST), Daejeon, Korea in 2000 and 2006, respectively. He was a visiting scholar at Purdue University, W. Lafayette, USA in 2007. Since 1987, he has been with ETRI as a principal member of research engineering staff, and involved in several projects including the development of various SoCs (System-on-Chip), an embedded DSP and speech codecs. His current research interests are in multimedia SoC, embedded processor, multimedia codecs and its applications.



Nak-Woong Eum received B.S. degree in Electronic Engineering from Kyungbook National University, Korea, in 1984 and M.S. and Ph.D. degrees in Electrical Engineering from Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1987 and 2001, respectively. Since 1987, he

has been working with ETRI, Daejeon, Republic of Korea, as a principal member of engineering staff, where he is currently the director of the System-on-Chip Research Department. From 1987 to the present, he has participated in several projects including the development of the electronic design automation system, an embedded DSP core, multimedia encoders, decoders, and receiver chips for digital multimedia broadcasting system. His current research interests include energy-scalable embedded processor, and System-on-Chip design methodology on deep-submicron technology.