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Negative Group Delay Circuit with Improved Signal Attenuation and Multiple Pole Characteristics

Girdhari Chaudhary · Junhyung Jeong · Phirun Kim · Yongchae Jeong*

Abstract

This paper presents a design of a transmission line negative group delay (NGD) circuit with multiple pole characteristics. By inserting an additional transmission line into a conventional NGD circuit, the proposed circuit provides further design parameters to obtain wideband group delay (GD) and to help reduce signal attenuation. As a result, the number of gain compensating amplifiers can be reduced, which can contribute to stable operation when integrated into RF systems. The multiple pole characteristics can provide wider NGD bandwidth and can be obtained by connecting resonators with slightly different center frequencies separated by quarter-wavelength transmission lines. For experimental validation, an NGD circuit with two poles GD characteristic is designed, simulated, and measured.

Key Words: Distributed Transmission Line, Low Signal Attenuation, Multiple Pole, Negative Group Delay.

I. INTRODUCTION

Electromagnetic wave propagation in any medium obeys the fundamental physical laws described by Maxwell's equation [1]. Most media exhibit normal propagation called subluminal, where the speed of propagation of individual time-harmonic components is slower than the speed of light, *c*, in a vacuum at all frequencies. However, in a specific and narrow frequency band of signal attenuation (SA) or in an anomalous dispersion frequency, the group velocity is observed to be greater than the *c*. This abnormal wave propagation is called superluminal group velocity or even negative group velocity [1, 2].

The wave propagation in any medium can be characterized by group velocity and group delay (GD), which are same. The GD in a circuit can be investigated by examining transmission phase variation with respect to frequency and can be defined as a negative derivative of the signal transmission phase according to frequency, as shown in (1).

$$\tau_g = -\frac{1}{2\pi}\frac{d\varphi}{df} \tag{1}$$

As seen from (1), when quantity τ_g is positive, the peak of the output pulse suffers a positive delay with respect to input pulse. On the other hand, if τ_g is negative, the peak of the output pulse emerges prior to the peak of the input pulse entering the medium, and the medium is said to exhibit a negative GD [3]. However, this does not violate the causality because the initial transient pulse is still limited to the front velocity, which will never exceed the speed of light [4].

The negative group delay (NGD) occurs at a certain range of frequency where the absorption or SA is maximum [1]. Therefore, band-stop structures are used to realize NGD circuits. Based on either series or shunt *RLC* resonators, various kinds of microwave NGD circuits have been presented and demonstrated in the literature [5−13]. To overcome the

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Division of Electronics and Information Engineering, IT Convergence Research Center, Chonbuk National University, Jeonju, Korea.
*Corresponding Author: Yongchae Jeong (e-mail: ycjeong@jbnu.ac.kr)

limited feasibility problem of lumped elements in microwave frequencies, the NGD circuits using distributed elements are also presented [5−7, 12]. However, the conventional NGD circuits presented in previous works exhibited excess SA up to 35 dB for a −8 ns GD, which can cause serious stability issues when an NGD circuit is integrated with RF/microwave systems. Therefore, for the same GD, the passband SA must be as small as possible.

A few studies have been conducted about NGD networks with small SA. In [13], a composite NGD network with smaller SA was presented. However, this circuit requires parallel lumped elements (such as capacitors and inductors) between two transmission lines, making implementation difficult at microwave frequencies.

In this paper, a design of the transmission line NGD circuit with reduced SA and multiple pole GD characteristics is presented.

II. Design Theory

Fig. 1 shows the structure of the conventional and proposed 1-pole NGD circuits that consist of resistor R and transmission lines with characteristic impedances of Z_1 and Z_2 and electrical lengths of λ/4. Total ABCD-parameters of the proposed circuit shown in Fig. 1(b) can be found as (2)

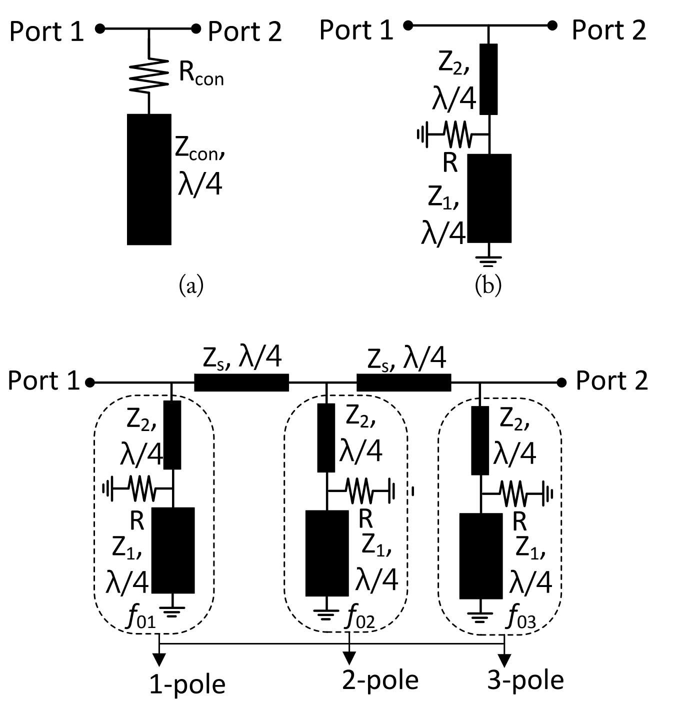


Fig. 1. Structure of transmission line negative group delay circuits: (a) conventional, (b) proposed 1-pole circuit, and (c) proposed multiple pole circuit.

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \dfrac{Z_1 Z_2 + jR\left(Z_1 \tan\dfrac{\pi f}{2f_0} - Z_2 \cot\dfrac{\pi f}{2f_0}\right)}{(Z_1+Z_2)Z_2 R + jZ_1 Z_2^2 \tan\dfrac{\pi f}{2f_0}} & 1 \end{bmatrix}, \tag{2}$$

where f and f_0 are operating and design center frequencies, respectively. The S-parameters of the proposed circuit can be found by using ABCD- to S-parameters conversion relationship [14], which is given as (3):

$$S_{11} = S_{22} = \frac{-Z_0\left[Z_1 Z_2 + jR\left(Z_1 \tan\dfrac{\pi f}{2f_0} - Z_2 \cot\dfrac{\pi f}{2f_0}\right)\right]}{\left[\begin{array}{l} 2(Z_1+Z_2)Z_2 R + j2Z_1 Z_2^2 \tan\dfrac{\pi f}{2f_0} + Z_1 Z_2 Z_0 \\ +jRZ_0\left(Z_1 \tan\dfrac{\pi f}{2f_0} - Z_2 \cot\dfrac{\pi f}{2f_0}\right) \end{array}\right]} \tag{3a}$$

$$S_{21} = \frac{2(Z_1+Z_2)Z_2 R + j2Z_1 Z_2^2 \tan\dfrac{\pi f}{2f_0}}{\left[\begin{array}{l} 2(Z_1+Z_2)Z_2 R + j2Z_1 Z_2^2 \tan\dfrac{\pi f}{2f_0} + Z_1 Z_2 Z_0 \\ +jRZ_0\left(Z_1 \tan\dfrac{\pi f}{2f_0} - Z_2 \cot\dfrac{\pi f}{2f_0}\right) \end{array}\right]}, \tag{3b}$$

where Z_0 is reference port impedance. Furthermore, S-parameters and GD at the f_0 can be obtained as (4).

$$S_{11}\big|_{f=f_0} = S_{22}\big|_{f=f_0} = \frac{Z_0 R}{Z_0 R + 2Z_2^2} \tag{4a}$$

$$\left|S_{21}\right|_{f=f_0} = \frac{2Z_2^2}{Z_0 R + 2Z_2^2} \tag{4b}$$

$$\tau_g\big|_{f=f_0} = -\frac{d\angle S_{21}}{d\omega}\bigg|_{f=f_0} = -\frac{Z_0}{4f_0}\left\{\frac{(Z_1+Z_2)R^2 - Z_1 Z_2^2}{Z_1 Z_2\left(Z_0 R + 2Z_2^2\right)}\right\} \tag{4c}$$

As seen from (4c), the maximum achievable GD depends on Z_1, Z_2, and R. To better understand (4b) and (4c), the calculated maximum achievable GD and SA at f_0 = 1.96 GHz according to Z_1 and R are shown in Fig. 2. As seen from this figure, the SA is improved as Z_2 increases. Therefore, high Z_2 and low Z_1 are necessary for reduced SA.

Fig. 3 shows the simulation results of the 1-pole NGD circuit. In this simulation, the maximum achievable GD at f_0 = 1.96 GHz is assumed to be −5 ns. As seen from this figure, the proposed circuit provides reduced SA as compared to the conventional circuit [6]. The SA of the proposed circuit is further reduced by making the value Z_2 is high. However,

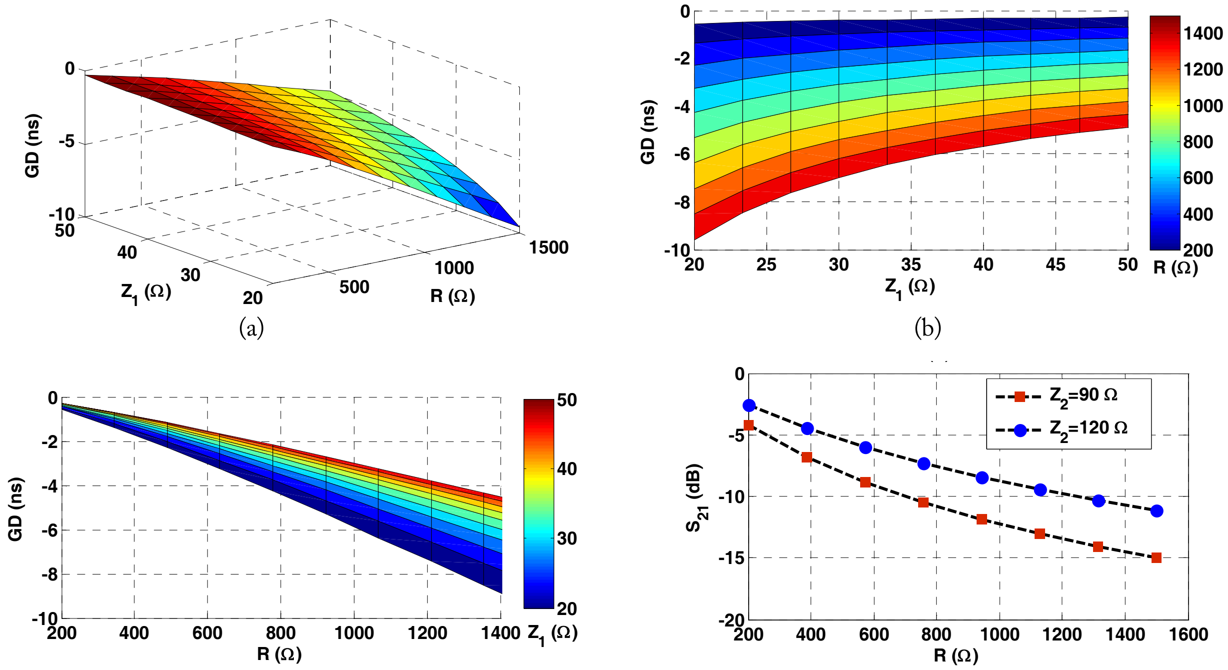


Fig. 2. Calculated group delay and signal attenuation (S_{21}) of a 1-pole negative group delay circuit according to R and Z_1 with Z_2=90 Ω and f_0=1.96 GHz: (a) 3-D plot, (b) group delay (GD) with respect to Z_1 where the color bar represents R, (c) GD according to R with the color bar denoting Z_1 and (d) signal attenuation (S_{21}) with respect to R.

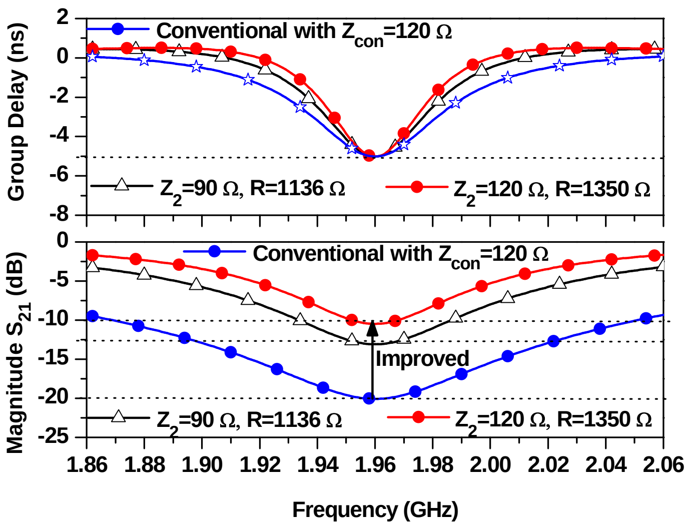


Fig. 3. Simulated results of 1-pole negative group delay circuit with different values of Z_2.

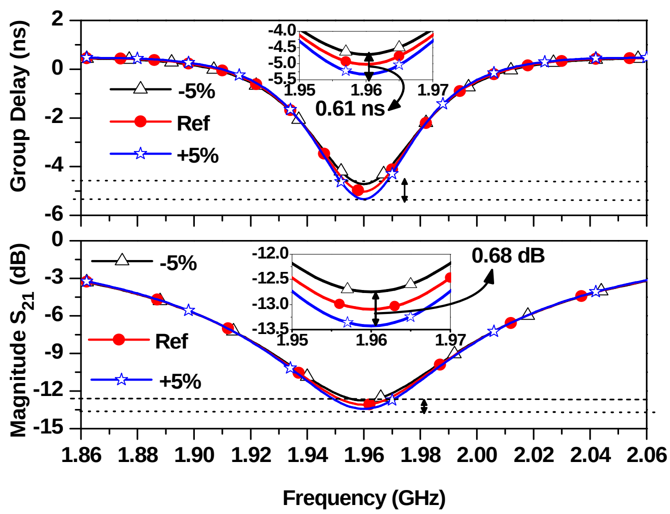


Fig. 4. Performance degradation of the proposed 1-pole negative group delay circuit assuming ±5% resistance variation from the reference value.

the NGD bandwidth is reduced.

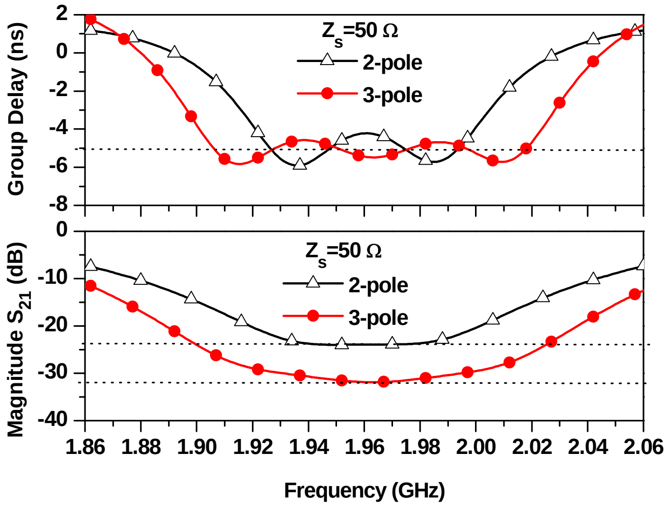
The temperature dependence of R is represented by the following relationship:

$$\frac{\Delta R}{R_0} = \delta \Delta T, \tag{5}$$

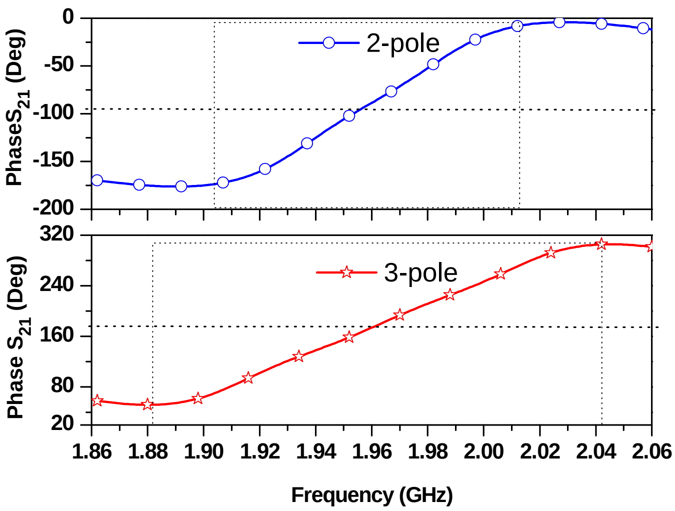
where δ, R_0, ΔR, and ΔT are temperature coefficient, initial resistance, resistance variation, and temperature variation, respectively.

Fig. 4 shows the performance degradation of the proposed 1-pole NGD circuit, assuming the resistance variation of ±5%. As seen from this figure, the GD and SA (magnitude of S_{21}) variations are approximately ±0.61 ns and ±0.68 dB from the reference values. These results indicate that the proposed NGD circuit is considerably less sensitive to the temperature-dependent resistance variation.

The NGD bandwidth can be enhanced by connecting 1-



(a)



(b)

Fig. 5. Simulated results of 2-pole and 3-pole negative group delay circuits: (a) group delay/magnitude and (b) phase characteristics.

pole NGD circuits with the slightly different center frequencies (f_{0i}, $i = 1, 2, 3, \ldots$) separated by λ/4 transmission lines with characteristic impedance of $Z_s = 50$ Ω, as shown in Fig. 1(c). Due to the different f_0 of 1-pole NGD circuits, multiple pole GD characteristics can be obtained.

Fig. 5(a) shows the simulated GD and S_{21} magnitude results of 2-pole and 3-pole NGD circuits. In the case of a 2-pole NGD circuit, two NGD circuits with $f_{01} = 1.935$ GHz and $f_{02} = 1.984$ GHz are cascaded. Similarly, for the 3-pole NGD circuit, the f_{0i} are given as $f_{01} = 1.912$ GHz, $f_{02} = 1.963$ GHz, and $f_{03} = 2.03$ GHz. In both cases, the circuit element values of 1-pole NGD circuits are given as $Z_1 = 30$ Ω, $Z_2 = 90$ Ω, and $R = 1139$ Ω. As seen from these figures, the NGD bandwidth is enhanced due to 2-pole and 3-pole characteristics. The phase characteristics of 2-pole and 3-pole NGD circuits are shown in Fig. 5(b). As seen from this figure, the phase slope of S_{21} is positive over a certain range of frequency, which signifies the presence of NGD characteristics.

III. Simulation and Experimental Results

For experimental validation of the proposed circuit, the design goal was to obtain a GD of −6 ns at $f_0 = 1.96$ GHz. For this purpose, a 2-pole NGD circuit was designed and fabricated. For given specifications, the calculated circuit element values of a 2-pole NGD circuit are given as $Z_1 = 30$ Ω, $Z_2 = 90$ Ω, $Z_s = 50$ Ω, and $R = 1{,}140$ Ω. The f_0s are the same as presented in Section II. The circuit was fabricated using RT/Duroid 5880 of Rogers Inc. with a dielectric constant (ε_r) of 2.2 and the thickness (h) of 31 mils. The simulation was performed using ANSYS HFSS 2014. The layout of the fabricated circuit is shown in Fig. 6. The physical dimensions of the fabricated circuit are shown in Table 1 after the optimization.

Fig. 7 shows the simulated and measured GD and magnitude results of the 2-pole NGD circuit. From the measurement, the GD was determined as −5.80±0.45 ns over a bandwidth of 80 MHz. The maximum SA at $f_0 = 1.962$ GHz was 24.67 dB. The SA can be easily compensated using general purpose gain amplifiers [5]. A photograph of the fabricated circuit is also shown in Fig. 7. The simulated and measured phase characteristics are shown in Fig. 8. As seen in this figure, the slope of the phase is positive over a certain region. This positive phase slope characteristic can be used to

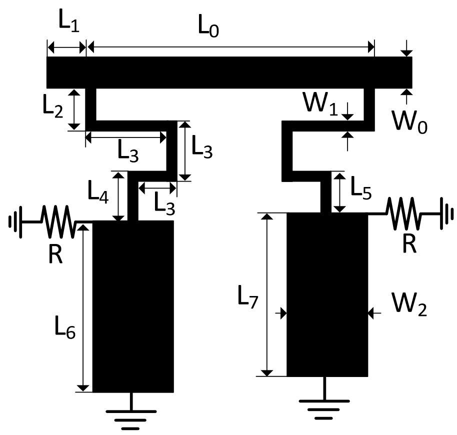


Fig. 6. Layout of the fabricated 2-pole negative group delay circuit with physical dimensions.

Table 1. Physical dimensions of the 2-pole negative group delay circuit (unit = mm)

L_0	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8	L_9	W_0	W_1	W_2
3.5	24.58	2.8	11.2	6.6	4.2	2.7	1.9	28.9	27.4	2.4	0.8	6.2

Physical dimensions refer to Fig. 6.

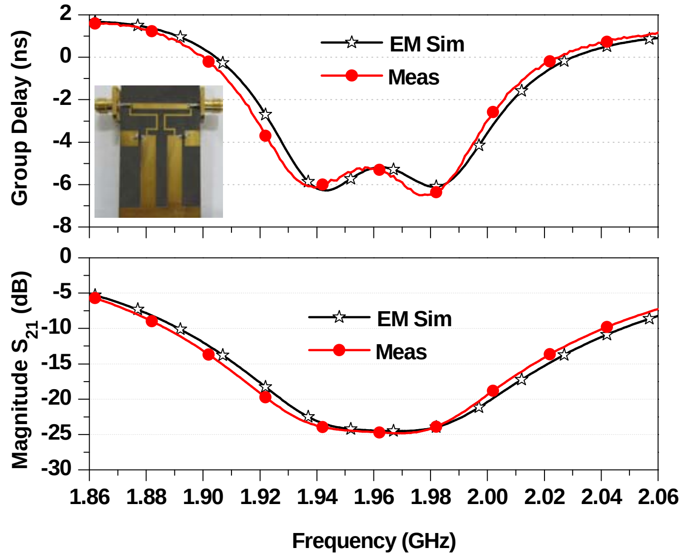


Fig. 7. Simulated and measured group delay/magnitude results of the 2-pole negative group delay circuit.

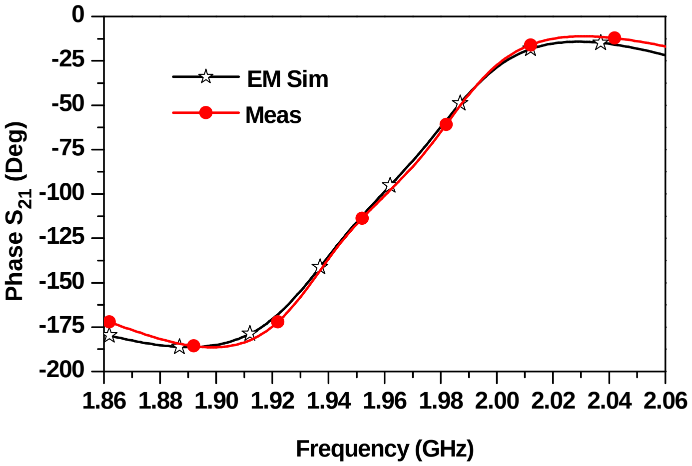


Fig. 8. Simulated and measured phase characteristics of a 2-pole negative group delay circuit.

cancel out the negative phase slope to obtain zero GD or a phase-compensated response.

IV. CONCLUSION

This paper demonstrates the design of an NGD circuit with multiple pole GD characteristics and reduced signal attenuation. The multiple pole NGD circuit is obtained by the cascade connection of several 1-pole circuits having slightly different frequencies. For the experimental verification, the 2-pole NGD circuit was designed, fabricated, and measured. The proposed topology can reduce the number of gain-compensating amplifier stages and can help improve efficiency, out-of-band noise reduction, and stable operations when integrated into RF/microwave systems.

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Girdhari Chaudhary

received the B.E. and M.Tech. degrees in Electronics and Communication Engineering from Nepal Engineering College (NEC), Kathmandu, Nepal and Malaviya National Institute of Technology (MNIT), Jaipur, India in 2004 and 2007, respectively and Ph.D. degree in Electronics Engineering from Chonbuk National University, Republic of Korea in 2013. He is currently working as Post-doctoral researcher at HOPE-IT human resource development center-BK21 PLUS, Division of Electronics Engineering, Chonbuk National University, Korea. He is receipt of Research Fellow through National Research Foundation (NRF) of Korea funded by the Ministry of Education. Dr. Chaudhary is also receipt of BK21 PLUS Research Excellence Award 2015 from Ministry of Education, Republic of Korea. He has authored and co-authored over 35 papers in international journals and conference proceedings. His research interests include multi-band tunable passive circuits, negative group delay circuits and its applications, and high efficiency power amplifiers.

Phirun Kim

received the B.E. degree in electronic engineering from National Polytechnic Institute of Cambodia (NPIC), Phnom Penh, Cambodia in 2010, the M.E. degree in electronics engineering from the Chonbuk National University, Jeonju, Republic of Korea, in 2013. He is currently working toward the Ph.D. degree at Division of Electronics Engineering, Chonbuk National University, Republic of Korea. His research interests include RF filter, power divider, impedance transformer, balun, and high-efficiency power amplifiers.

Junhyung Jeong

received the B.E. and M.E. degree in electronics & information engineering from the Chonbuk National University, Jeonju, Republic of Korea, in 2012, and 2014. He is currently working toward the Ph.D. degree at Division of Electronics Engineering, Chonbuk National University, Republic of Korea. His research interests include RF filter, high-efficiency power amplifiers and RF transmitter.

Yongchae Jeong

received B.S.E.E., M.S.E.E., and Ph.D. degrees in electronics engineering from Sogang University, Seoul, Republic of Korea in 1989, 1991, and 1996, respectively. From 1991 to 1998, he worked as a senior engineer with Samsung Electronics. From 1998, he joined Division of Electronics Engineering, Chonbuk National University, Jeonju, Republic of Korea. From July 2006 to December 2007, he joined at Georgia Institute of Technology as a visiting Professor. Now, he is a professor, member of IT Convergence Research Center, and director of HOPE-IT Human Resource Development Center of BK21 PLUS in Chonbuk National University. He is currently teaching and conducting research in the area of microwave passive and active circuits, mobile and satellite base-station RF system, design of periodic defected transmission line, and RFIC design. Dr. Jeong is a senior member of IEEE and member of the Korea Institute of Electromagnetic Engineering and Science (KIEES). He has authored and co-authored over 100 papers in international journals and conference proceedings.