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A D-Band Integrated Signal Source Based on SiGe 0.18 μm BiCMOS Technology

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Abstract

This work describes the development of a D-band (110–170 GHz) signal source based on a SiGe BiCMOS technology. This D-band signal source consists of a V-band (50–75 GHz) oscillator, a V-band amplifier, and a D-band frequency doubler. The V-band signal from the oscillator is amplified for power boost, and then the frequency is doubled for D-band signal generation. The V-band oscillator showed an output power of 2.7 dBm at 67.3 GHz. Including a buffer stage, it had a DC power consumption of 145 mW. The peak gain of the V-band amplifier was 10.9 dB, which was achieved at 64.0 GHz and consumed 110 mW of DC power. The active frequency doubler consumed 60 mW for D-band signal generation. The integrated D-band source exhibited a measured output oscillation frequency of 133.2 GHz with an output power of 3.1 dBm and a phase noise of −107.2 dBc/Hz at 10 MHz offset. The chip size is 900 × 1,890 μm^2, including RF and DC pads.

Key Words: Amplifier, D-Band, Frequency Doubler, Oscillator, Signal Source.

I. INTRODUCTION

The rapidly increasing demand for high-speed communication has spurred the development of new information and communication technologies aimed at satisfying growing high-speed needs. Numerous research groups are now actively reporting promising results for enhancements in high-speed wireless communications [1]. This technical trend supports the prediction that applications for frequency ranges beyond 100 GHz will be in the spotlight in the not so distant future. This frequency band has many advantages, such as wide bandwidth and compact size, which arise from its high frequency and small wavelength, respectively.

One of the key blocks in the high frequency wireless communication systems is the transmitter, which generally lacks sufficient output power at the high operation frequency. The currently available transistors are limited in their f_{max}, so designing a high power signal source that can operate beyond 100 GHz is very challenging. One useful way to overcome this frequency limitation is to add a frequency multiplier to the source to provide a frequency boost. This higher output power can be further enhanced by inserting an amplifier prior to the input of the frequency multiplier, to boost the signal before multiplication. There have been efforts to implement high frequency signal sources based on this approach [2]. However, few have included an integrated on-chip oscillator, which is critical for compact realization of signal sources.

This work introduces a D-band integrated signal source, which consists of a V-band oscillator, a V-band amplifier, and a D-band frequency doubler based on a SiGe BiCMOS technology.

II. CIRCUIT DESIGN

Several different methods are available for the design of a signal source that operates at high frequencies, as shown in Fig.

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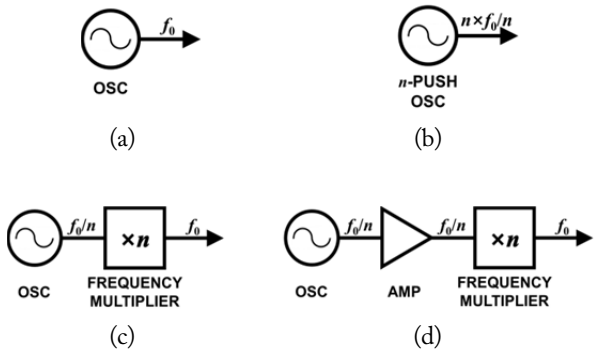

Fig. 1. Block diagrams of various topologies for signal sources to generate f_0.

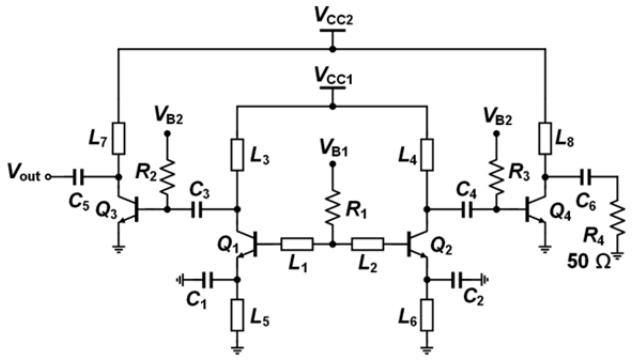

Fig. 2. Schematic of the V-band oscillator developed in this work. R_4 is added only for the individual test circuit and absent for the integrated signal source.

1. The simplest method is to use a fundamental-mode oscillator as a source, as shown in Fig. 1(a). However, designing a fundamental-mode oscillator that operates near f_{max} can be very challenging. For example, according to the model, the f_{max} of the transistors adopted in this work is 139 GHz, which complicates efforts to design a signal source operating beyond 100 GHz based on these devices. An oscillation frequency near or even higher than f_{max} can be obtained by adopting topologies that use the extraction of harmonic signals as an alternative [3−5]. This type of harmonic generation can be achieved inside the oscillator or with an external frequency multiplier. Fig. 1(b) presents a block diagram of an n-push oscillator, which achieves the n-th harmonic internally, while Fig. 1(c) shows a fundamental-mode oscillator integrated with a frequency multiplier.

It is reported that a fundamental-mode oscillator integrated with a n× frequency multiplier has a better output power and DC-to-RF efficiency than the n-push oscillator [6]. One issue with using a frequency multiplier, however, is that the input power needs to be high enough to obtain a reasonable power level at the output. The input power of the frequency multiplier can be boosted by adding an amplifier between the oscillator and the frequency multiplier, as shown in Fig. 1(d). This generates a high power output signal near or beyond the f_{max} of a given device technology. This is the topology adopted in the present work for the implementation of the D-band signal source. The design details of the individual components developed in this work for the integrated source are provided below.

1. Oscillator

Fig. 2 shows the schematic of the V-band fundamental-mode oscillator developed in this work. The oscillator adopts the Colpitts topology, which is favored over the *LC* cross-coupled topology for high frequency generation. The oscillator is also designed to have differential outputs that take into consideration the differential inputs of the amplifier and the frequency multiplier that follow. The core transistors Q_1 and Q_2 generate the V-band signal, while transistors Q_3 and Q_4 function as output buffers.

Generally, the output power of an oscillator will increase with the size of the transistors, but the oscillation frequency will decrease. In this work, large size transistors were adopted in favor of the stable oscillation, given the rather sufficient margin for frequency budget. All sizes of the transistors Q_1–Q_4 have been chosen as 10.16 μm, which is the longest emitter length available in the technology used. L_1–L_8 are the transmission lines, where L_1–L_6 are the core elements that determine the oscillation frequency, and L_7–L_8 are the loads of the output buffers. A single-ended output signal is measured by terminating one output node by a 50-Ω resistor.

2. Amplifier

The output power of a source composed of an oscillator and a frequency multiplier can be boosted by adding an amplifier, either after the oscillator or after the frequency multiplier. The latter is more challenging because of the difficulty in achieving sufficient gain at higher frequency, due to the limitations in f_{max} of the technology. Therefore, in this work, a V-band amplifier was inserted after the oscillator. Its schematic is shown in Fig. 3, which employs a cascode topology.

The transistors Q_1–Q_4 have the longest available emitter

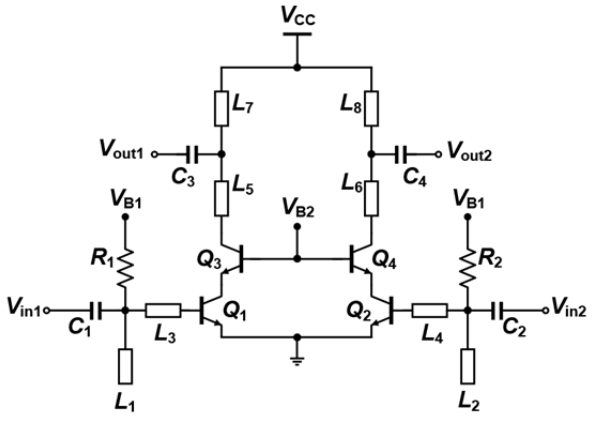

Fig. 3. Schematic of the V-band amplifier developed in this work.

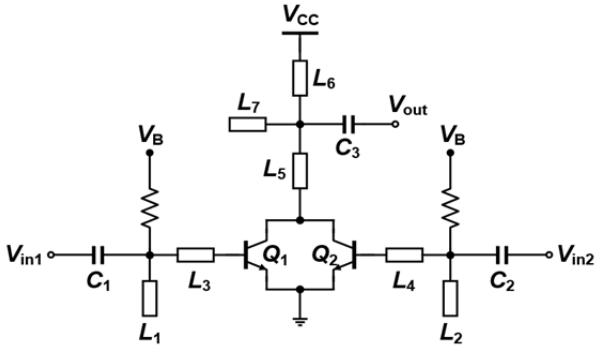

Fig. 4. Schematic of the D-band frequency doubler developed in this work.

length of 10.16 μm. The input and output matchings were achieved with transmission lines L_1–L_8. Note that the metal lines attached at the base of Q_3–Q_4 were kept as short as possible, as inductance at the base is known to have significant effects on the stability of common-base amplifiers [7]. The test amplifier, which was separately fabricated for individual characterization, included a balun added at the input and output ports (not shown in Fig. 3) to allow single-ended measurement.

3. Frequency Multiplier

The schematic of the frequency doubler is shown in Fig. 4. It is based on a common-emitter differential pair, the output being taken at the collector common node. At this node, all the odd harmonics, which have opposite phases for the left and right branches of the pair, are canceled out. On the other hand, the even harmonics have the same phases at the two branches and they are added at this common node. Hence, only the even harmonics will appear at this node, with the second harmonic being the strongest in its signal power level.

The emitter lengths of Q_1–Q_2 were chosen as 10.16 μm, which showed a good balance between output power and conversion loss characteristics in simulation. Open stubs L_1–L_2 and series transmission lines L_3–L_4 were used to match the input at the fundamental target frequency. The output node incorporated a series transmission line L_5, a short stub L_6, and an open stub L_7 for matching, which helps to maximize the output power of the doubled frequency. The test circuit fabricated for individual testing contained a balun, which was inserted at the input port for single-ended measurement.

III. Measurement Results

The D-band integrated signal source, combining the three circuits described above, was fabricated based on TowerJazz 0.18-μm BiCMOS technology. Individual circuits of each block were also fabricated for characterization of the individual circuit performance. A photograph of the integrated source is shown in Fig. 5. The total chip size, including RF and DC pads, is 900 × 1,890 μm^2.

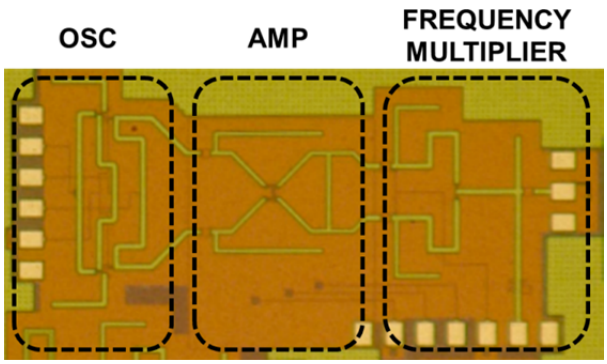

Fig. 5. Chip photograph of the integrated signal source.

The fabricated individual oscillator was measured with an Agilent E4407B spectrum analyzer and Agilent E4419B power meter. Fig. 6 shows the measured spectrum, indicating an oscillation frequency of 67.3 GHz. The inset shows the measured output power, which is –4.5 dBm before loss calibration, which corresponds to a calibrated power of 2.7 dBm after loss compensation. The DC power consumption is 145 mW, leading to a DC-to-RF efficiency of 1.3%.

The small signal characteristics of the V-band amplifier were measured using an Agilent E8361A network analyzer through *S*-parameters, as depicted in Fig. 7. The V-band amplifier has a peak gain of 10.9 dB at 64 GHz and a 3-dB bandwidth of 8 GHz (61–69 GHz). The DC power consumption was 110 mW.

The amplifier was also characterized for the linearity, using the measurement setup shown in Fig. 8(a). The signal from a V-band source module powered by an Agilent E83650B signal generator was injected into the amplifier, and the output was determined by an Agilent E4419B power meter. An additional

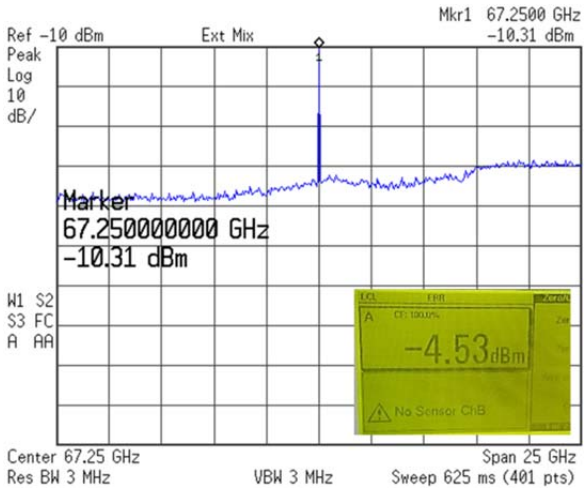

Fig. 6. Measured spectrum of the oscillator. Inset is the output power measured with a power meter (before loss calibration). The power after calibration is 2.7 dBm.

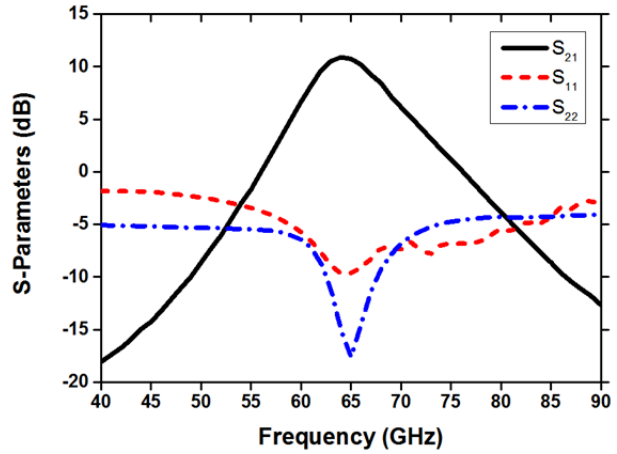

Fig. 7. Measured *S*-parameters of the V-band amplifier.

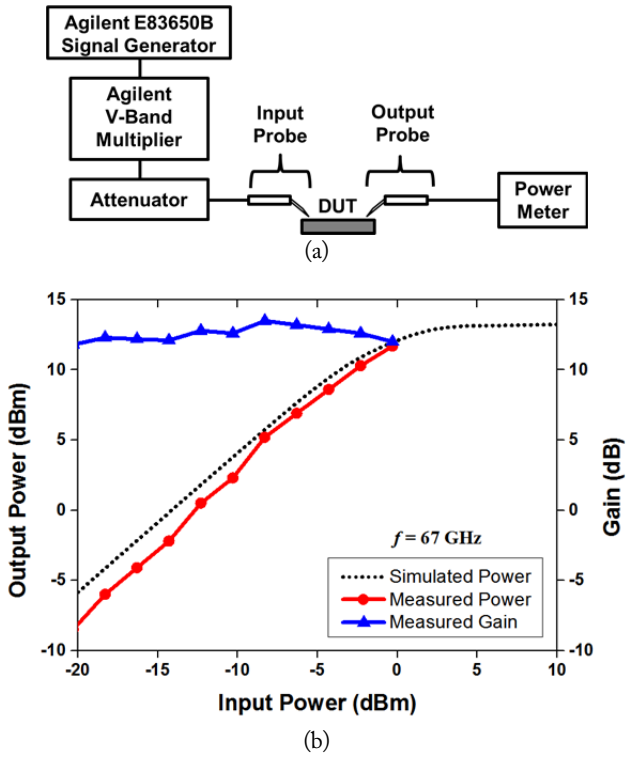

Fig. 8. (a) Setup for linearity measurement. (b) Measured linearity of the amplifier.

QuinStar QDA-V0000 attenuator was attached to the source module for input power control.

The measured linearity is shown in Fig. 8(b). Due to the limitations of the output power of the source module, measurements were only made up to an input power of around 0 dBm. However, a comparison with a simulation, which is also shown in the plot, indicates that the saturation power of the amplifier is expected to reach around 13 dBm. Together with the output power of the oscillator, 2.7 dBm, the output from the amplifier should be sufficient to drive the following frequency doubler.

The measurement setup of the frequency doubler is identical to that for the amplifier linearity measurement, except that an Erickson PM4 power meter was used for the D-band power measurement. As already mentioned, due to the limited output power of the signal source, the measurements were made only up to an input power of around 0 dBm. The lower limit was also imposed by the noise floor level of the measurement (around –40 dBm), resulting in a few data points available from the measurement as shown in Fig. 9. However, the measurement shows a reasonably good agreement with the simulation for the measured range, as shown in the plot. Thus, the circuit is expected to follow the performance predicted by the simulation. This was actually verified with measurements of the integrated source, as described later. This circuit consumes 60 mW of DC power.

Finally, the integrated source was characterized using the setup shown in Fig. 10, which is composed of an Agilent E-4407B spectrum analyzer and a D-band external sub-harmonic mixer (2nd order) driven by a V-band source with an Agilent E83650B signal generator. The output spectrum of the signal source, with the frequency down-converted for testing, is shown in Fig. 11. The measured 2.31 GHz indicates that the output frequency of the integrated source is 133.2 GHz, considering the LO input ($2\omega_{LO}$) of 135.5 GHz.

The inset in Fig. 11 shows the output power measured

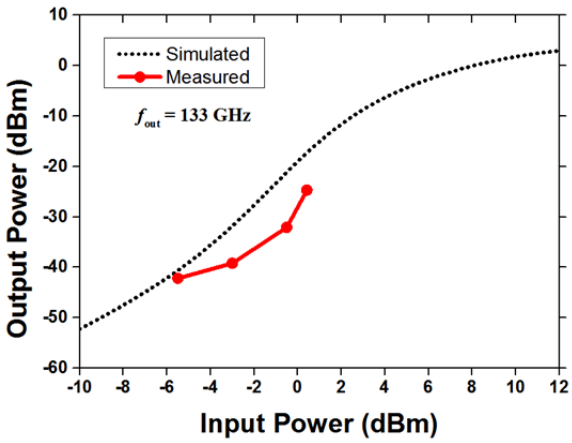

Fig. 9. Measured large signal characteristics of the frequency multiplier.

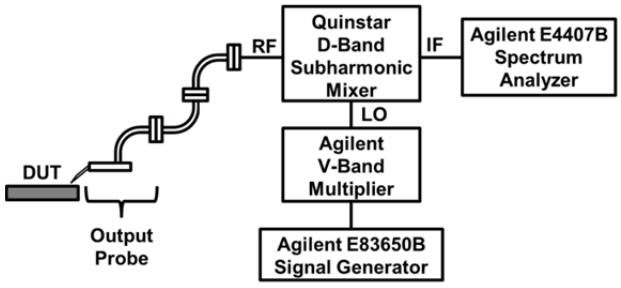

Fig. 10. Measurement setup for the integrated D-band signal source.

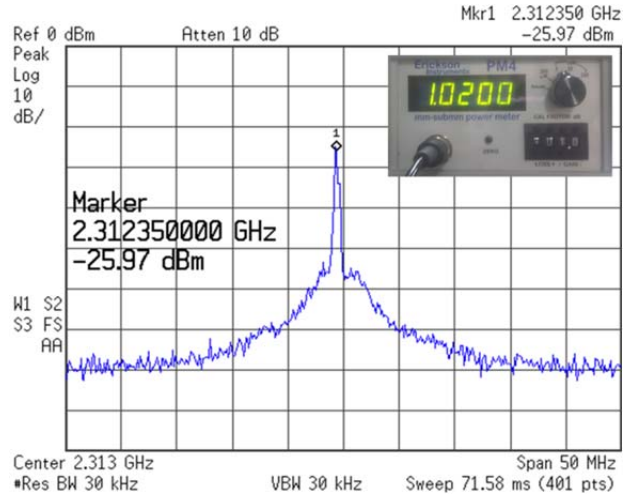

Fig. 11. Measured output spectrum of the integrated signal source (down-converted with $2\omega_{LO}$=135.5 GHz). Inset is the output power measured with a power meter (before calibration). The calibrated output power is 3.1 dBm.

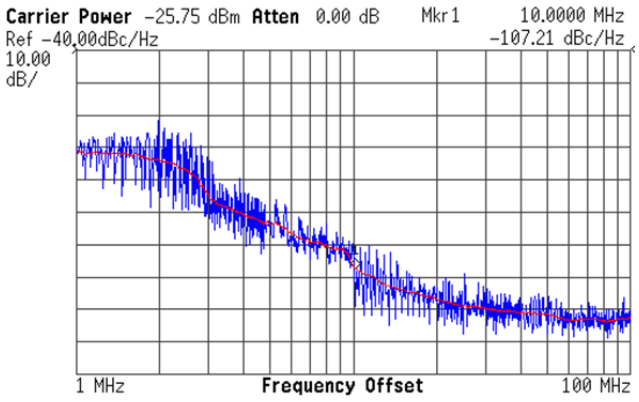

Fig. 12. Measured phase noise of the integrated signal source.

through an Erickson PM4 power meter (before calibration). With the loss of the D-band probe, known to be 3 dB, the calibrated output power is 3.1 dBm. The phase noise was measured as −107.2 dBc/Hz at a 10 MHz offset, as shown in Fig. 12. The total DC power consumption was 315 mW, leading to a DC-to-RF efficiency of 1.0%. The measured performance of the fabricated integrated source is compared with other signal sources operating around D-band in Table 1. This comparison indicates that the source developed in this work is among the best in terms of its output power level in this frequency range.

IV. Conclusion

A D-band signal source based on a 0.18-μm SiGe BiCMOS technology was developed by integrating a V-band oscillator, a V-band amplifier, and a D-band frequency multiplier. The integrated source exhibited an output power of 3.1 dBm at 133.2 GHz and the phase noise was −107.2 dBc/Hz at 10 MHz offset. The performances of the individual circuit blocks were also characterized. The employed topology for a signal source may represent an efficient solution for D-band high power signal generation.

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Table 1. Signal sources operating beyond 100 GHz based on Si-based technologies

Ref	Technology	Harmonic number	Frequency (GHz)	Peak P_{OUT} (dBm)	P_{dc} (mW)	DC-to-RF efficiency (%)	Phase noise at 1 MHz (dBc/Hz)	FoM (dBc/Hz)
[8]	0.13 μm RFCMOS	3	177	−16.6	36	0.06	−80.2	−170
[9]	65 nm CMOS	1	102	−26	7.4	0.03	−85.1	−177
[10]	120 nm SiGe HBT	1	156	−3	47	1.1	−83	−170
[11]	120 nm SiGe HBT	1	148	−11	35	0.23	−81	−169
[12]	65 nm CMOS	1	105	4.5	54	5.2	−92	−175
[13]	65 nm CMOS	3	158	−19	24	0.05	−85	−175
[14]	130 nm SiGe HBT	1	154	7	68	7.3	−87.2	−173
[15]	40 nm CMOS	3	543	−31	16.8	0.005	NA	NA
[16]	120 nm SiGe HBT	2	311	−1.7	167	0.4	−101.6*	−169
[17]	130 nm SiGe HBT	2	215	−7.1	30	0.6	−92	−184
This	0.18 μm SiGe BiCMOS	2	133	3.09	315	1.0	−107.2*	−165

* Phase noise at 10 MHz offset.

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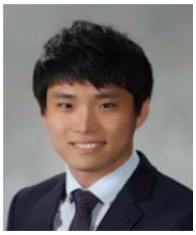

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