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A Novel Structure for the Improved Switching Time of 50V Class Vertical Power MOSFET

Doohyung Cho*,**, Kunsik Park** , Kwangsoo Kim*★

Abstract

In this paper, a novel trench power MOSFET using a Separate-W-gated technique MOSFET (SWFET) is proposed. Because the SWFET has a very low Q_{GD} compared to other forms of technology, it can be applied to high-speed power systems. The results found that the SWFET-applied Q_{GD} was decreased by 40% when compared to simply using the more conventional trench gate MOSFET. C_{ISS} (input capacitance : $C_{GS}+C_{GD}$), C_{OSS} (output capacitance : $C_{GD}+C_{DS}$) and C_{RSS} (reverse recovery capacitance : C_{GD}) were improved by 24%, 40%, and 50%, respectively. The switching characteristics of the inverter circuit shows a 24.9% enhancement of reverse recovery time, and the power efficiency of the DC-DC buck converter increased by 14.2%. In addition, the proposed SWFET does not require additional process steps and There was no degradation in the electrical performance of the current-voltage and on-resistance.

Key words: trench MOSFET, Q_{GD}, gate charge, DC-DC buck converter, switching time.

I. Introduction

In recent decades, power semiconductor devices have seen drastic improvements. The high-speed power MOSFET in particular is used for a wide variety of applications such as vehicles, mobile communication devices, and PMIC (Power Management IC) [1]. The recent global economic crisis and drastically fluctuant price of energy have resulted in an increased demand for green IT (Information Technology) technology to reduce overall energy consumption. Research on device structures, which have low-power loss, have seen significant progress in the power semiconductor field [2]-[3]. If the power loss in power MOSFET used in PMIC is reduced, the power loss in the entire IC will be reduced accordingly. Therefore, the demand for power MOSFETs which have low-power loss can be increased. The power loss of a MOSFET occurs primarily due to conduction loss and switching loss. The conduction loss is proportional to the on-resistance. However, it is difficult to reduce conduction loss since the decrease in on-resistance of silicon devices reaches a limit.

The switching loss is determined by the gate charge (Q_G) [4]-[6]. Therefore, decreasing the charge of a gate region is an effective way to reduce the switching loss in a power MOSFET. The W-gated MOSFET is an example of a method which reduces the Q_G [7]-[8]. The W-gated

*Dept. of Electronics Engineering, Sogang University,
**Convergence Component & Materials Research Laboratory,
Electonics and Telecommunications Research Institute (ETRI)
doohyung@sogang.ac.kr, 070-8816-0032
★ Corresponding author
kimks@sogang.ac.kr, 070-8816-0032
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MOSFET can easily make a thick bottom oxide region by using a LOCOS process. The thick gate bottom oxide decreases the switching loss due to its low Q_{GD} [10]-[11]. Fig. 1(a) shows the conventional trench gate MOSFET, and Fig. 1(b) shows the proposed SWFET. The SWFET reduces the region which overlaps the gate-drain region and the Q_{GD} by forming a thick gate bottom oxide [10]-[11]. Consequently, the SWFET achieves low power loss in accordance with current green IT technology principles. Furthermore, the SWFET can be fabricated without additional fabrication processes due to its similarity to the W-gated MOSFET processes [7]-[8]. A Silvaco T-CAD tool was used for the simulation to analyze the characteristics of the proposed device [9].

Table 1 List of parameters of the trench gate MOSFET and proposed SWFET

Parameter	Trench MOSFET	SWFET
Cell pitch	2.4μm	2.4μm
Trench width	1μm	1μm
Trench depth	1.3μm	1.3μm
Poly gate thickness	0.9μm	50nm
Epitaxial thickness	4μm	4μm
Source doping	$1x10^{20}cm^{-3}$	$1x10^{20}cm^{-3}$
P-body doping	$1x10^{17}cm^{-3}$	$1x10^{17}cm^{-3}$
Gate oxide thickness	50nm	50nm
Bottom oxide thickness	50nm	150nm
Device size	$2.4mm^2$	$2.4mm^2$

II. SIMULATION RESULTS AND DISCUSSIONS

2.1 The proposed structure of the SWFET

Fig. 1(b) shows the new SWFET structure. Each parameter was optimized in a previous study [12]. This structure forms a thick trench bottom oxide using a sidewall thin gate and a LOCOS process. A low Q_{GD} and capacitance are obtained due to the reductive effects of the bottom oxide and the overlapped gate-drain region. As a result, the switching loss is decreased [5]-[6]. Table.1 presents the parameters of the SW and the trench gate MOSFET.

2.2 The fabrication process of the SWFET

Fig. 2 shows the process flow of the proposed SWFET using the conventional processing sequence of a trench MOSFET [13]-[14]. First, the Si-epi layer doped by phosphorus ($1e16/cm^3$) is grown by a thickness of 4μm on the highly doped N+ substrate. After the deposition of the Si-nitride, the

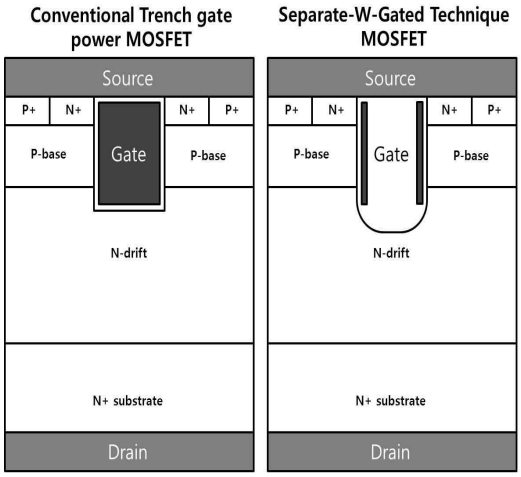

Fig. 1 Schematic cross-section of trench MOSFET (a) Trench gate MOSFET, (b) Separate-W-gated MOSFET (SWFET)

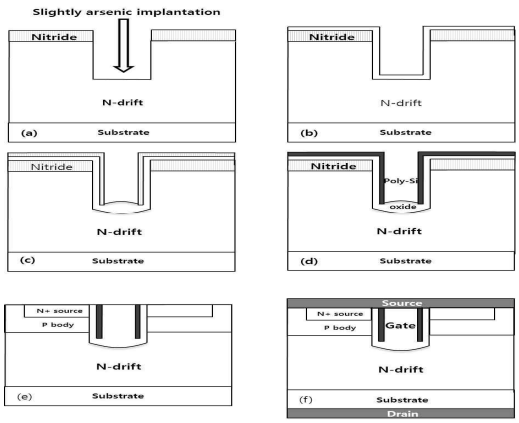

Fig. 2 Process flow of SWFET (a) trench etching and slightly arsenic implantation, (b) oxidation, (c) Si nitride deposition and LOCOS process, (d) Si nitride strip and Poly-Si deposition after Gate bottom Poly-Si etching, (e) formation of P-body and N+ source (f) electrode naming

trench gate region is opened. After the trench is etched by a width of 1μm and a depth of 1.3μm using the RIE (Reactive Ion Etching) process, arsenic is lightly implanted. Oxidation is processed by a thickness of 50nm as shown in Fig. 2(b).

In Fig. 2(c), the Si-nitride is deposited 50nm below the surface, and the etching and oxidation is then processed. Oxidation in the vertical direction is faster than that in the lateral direction since the gate bottom region is slightly doped by arsenic. After the Silicon nitride used as a spacer is removed, as shown in Fig 2(d), Poly silicon is used as a gate and is deposited 50nm below the surface. The gate bottom region is etched after the deposition. Oxide deposition is used in the rest of the gate region. After planarization of the surface via CMP process, a N+/P-body region is formed. Finally, the fabrication process is completed after the formation of electrodes on the finished device.

2.3 Voltage-Current Characteristics of the SWFET

The SWFET consists of two structures separated by the deposition of two thin poly-gates in the sidewall. The oxide region is filled between each sidewall poly-gates. This does not affect the operation characteristics of the MOSFET. Thus, SWFET does not cause any degradation in the electrical characteristics when compared to the trench gate MOSFET [15]-[16].

Fig. 3 shows the I_D-V_{DS} curve of the SW and of the trench gate MOSFET. As Fig. 3 shows, there is little degradation in the noted characteristics. It is only confirmed that resistance of the SWFET is increased by 5% when compared to that of the trench gate MOSFET at less than V_{GS} of 4V. In the case of the SWFET, the electrical field is not uniformly distributed at the trench bottom region even though the gate voltage is biased compared to that of the trench gate MOSFET [11]. Therefore, the relatively small current of SWFET is able to flow because the electrons are only accumulated at the gates edges. Because the electric field does not directly reach the central area of the trench bottom, resistance is increased. This phenomenon occurs when using a voltage of 4V. A reduction of 5% in resistance can be confirmed when the gate voltage is biased over the voltage of 4V. Accumulation concentration persists in the whole trench bottom region if a relatively high gate voltage is biased to the electrons doped by arsenic in the trench bottom region. Resistance is thus decreased. The effects of the trench bottom accumulation of the two devices are verified by a comparison in their potentials.

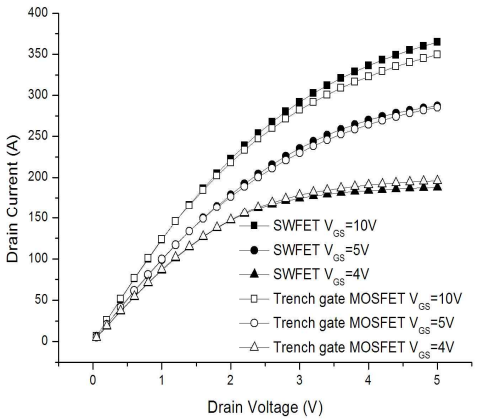

Fig. 3 The I_D-V_{DS} characteristics of SW and conventional trench gate MOSFET

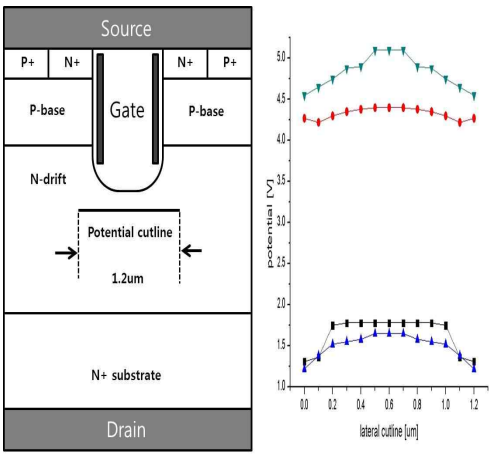

Fig. 4 Gate bottom lateral direction potential distribution of SW and conventional trench gate MOSFET

In Fig. 4, when observing the potentials in the trench bottom region of the two devices, the potential of the SWSFET at VGS of 3V is higher than that of the trench gate MOSFET alone. The

vertical voltage drop is low. On the other hand, the trench bottom potential of the SWFET is relatively lower than that of the trench gate MOSFET due to high accumulation concentration when V_{GS} is observed at a high voltage of 10V. Currents easily flow due to the higher vertical voltage drop. The effect of increasing resistance at a low gate voltage is not problematic for power devices as it is not common to use a low gate voltage. Resistance is decreased when the high gate voltage is biased. As such, high gate voltage is suitable for power devices. Fig. 5 shows the breakdown voltage graph, which is based on the simulations comparing the SWFET and the trench gate MOSFET. Although the shape of the gate region changed, the values of the fundamental parameters and doping concentrations are identical. Therefore, the depletion region width which strongly affects the breakdown voltage of the P-body/N-drift junction is also same [14]. Therefore, it is confirmed that there is no change in the breakdown of the conventional device and the proposed SWFET.

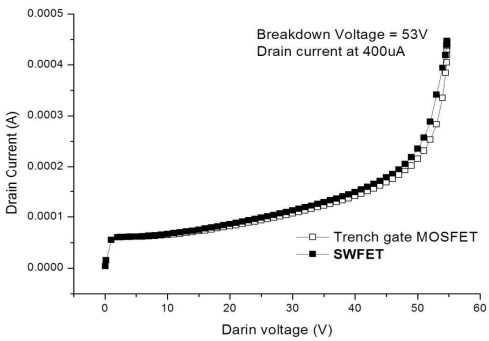

Fig. 5 The characteristics of breakdown voltage of SW and trench gate MOSFET

2.4 Charge and capacitance characteristics of the SWFET

The new proposed SWFET reduces the area overlapped by the gate-drain in order to decrease the Q_{GD}. A thick layer of gate oxide is grown in the bottom region. As a result of the thick bottom oxide, the charge which gathers at the gate bottom is decreased [10].

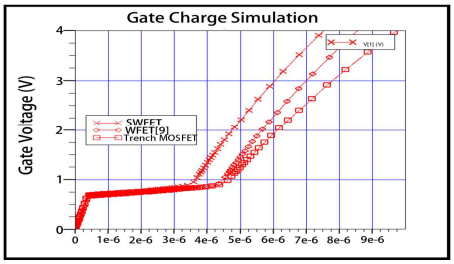

Fig. 6. The gate charge of SWFET, WFET and conventional trench gate MOSFET

Fig. 6 shows the gate voltage vs. transient time charge via a simulation graph of the SWFET, WFET [8] and the conventional trench gate MOSFET. In this figure, the flat section between 0.5V and 1V is the Q_{GD} (Miller plateau). The amount of charge charged and discharged in the gate-drain is reduced as the section is shorter. Subsequently the switching delay is decreased. Thus, the Q_{GD} of the SWFET sees greater improvement over simply using the trench gate MOSFET. In the case of the proposed SWFET, the Q_{GD} is 2.7nC. However, the Q_{GD} of the trench gate MOSFET is 4.5nC. This means there is an improvement of 40%. It is expected that the switching on/off performance of the SWFET is accordingly better than that of the trench gate MOSFET. A number of capacitance components exist in power MOSFET. Each capacitance contributes to the device during on/off switching according to their different roles. The capacitance components which are parasitic in the device are as follows [17].

Off performance of the SWFET is accordingly better than that of the trench gate MOSFET. A number of capacitance components exist in power MOSFET. Each capacitance contributes to the device during on/off switching according

$$C_{ISS} = C_{GS} + C_{GD} \quad (1)$$

$$C_{OSS} = C_{DS} + C_{GD} \quad (2)$$

$$C_{RSS} = C_{GD} \quad (3)$$

In this research, the proposed device utilizes a thick bottom oxide in order to reduce the Q_{GD} and

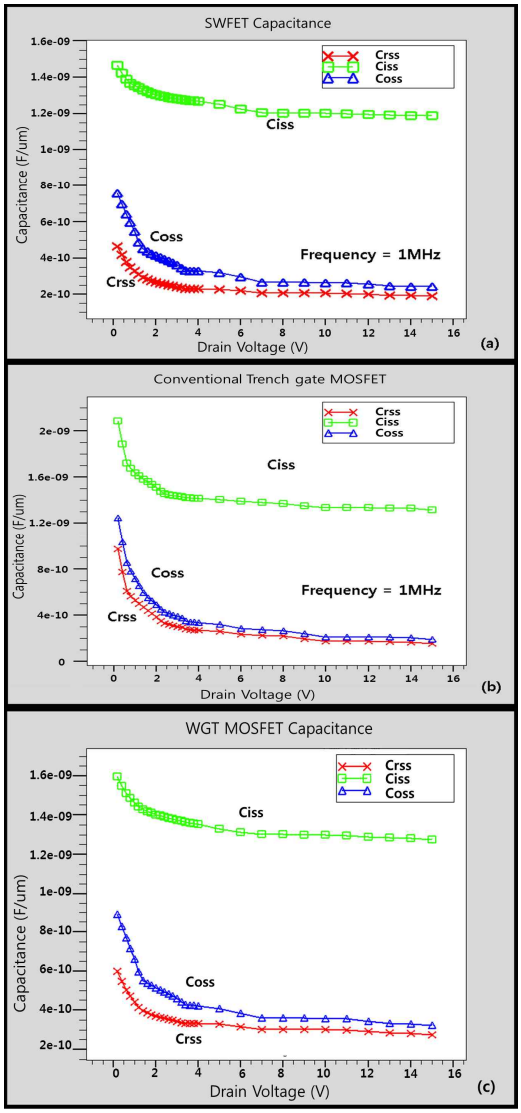

Fig. 7 The characteristics of capacitance of (a) SW and (b) conventional trench gate MOSFET (c) W-gate MOSFET

minimize the area overlapped via gate-drain. The decrease in the Q_{GD} also affects the reduction of C_{RSS} in the equation (3). The Q_{GD} determines the reverse recovery time at the point in which the device turns on and off. In this case, the reverse recover time is the switching delay. Thus switching must be turned on and off in a short period of time. The decrease in C_{RSS} reduces the switching loss occurred during the switching delay. The C_{ISS}, C_{OSS} and C_{RSS} of the proposed SWFET are respectively improved by 24%, 40%, and 50%. As Equation (1), Equation (2) and Equation (3) show, all of capacitance parameters are decreased due to the inclusion of Q_{GD} in all cases.

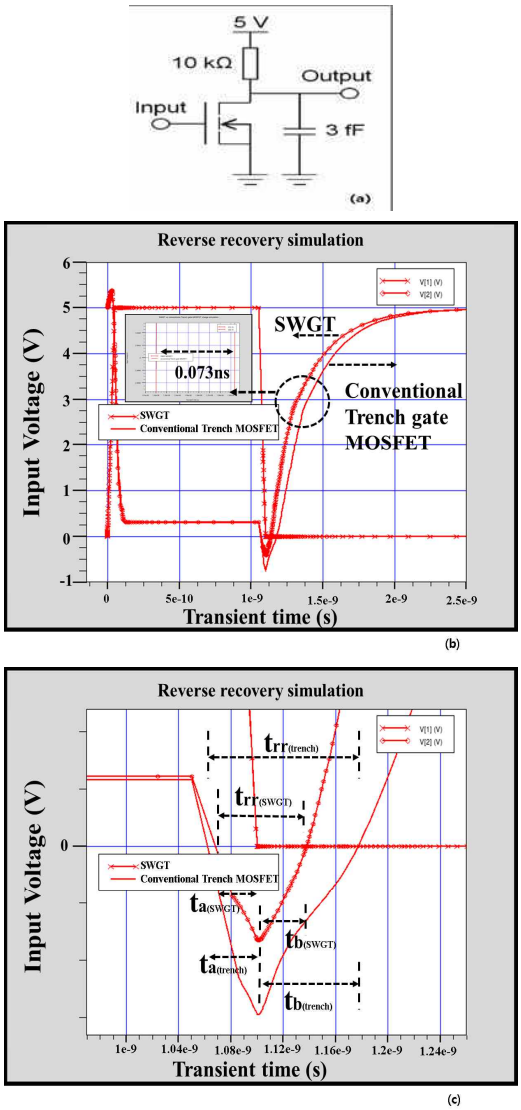

Fig. 8 SW vs. trench gate MOSFET (a) inverter circuit, (b) simulation result, (c) reverse recovery time analysis

2.5 Switching delay characteristic of the SWFET

The SWFET achieves reduced Q_{GD} and C_{GD} (C_{RSS}). When designing a circuit, switching speed is expected to be improved. Therefore, the inverter circuit is designed to confirm the switching characteristics. Fig. 8(a) shows a simple inverter circuit. The SW and trench gate MOSFET are located on the transistor in Fig. 8(a), and each switching delay is verified by the simulation. In. Fig. 8(b), the transistor is turned on during the input voltage 0~0.1ns (rising time) and is biased at 5V. The transistor is decreased by 0V during 1~1.1ns (falling time) and then turned off. Thus, the voltage which is contrary to the input is generated through the output. As Fig. 8(b) shows, the on state is switched to the off state when the input voltage is 1.1ns, so the switching characteristics seems to be efficient in recovering the 5V.
The SWFET approaches 1.320ns near the 3V point, and as the trench gate MOSFET approaches 1.393ns, the gap is shown to be 0.073.ns. The switching performance is improved by 24.9%. This result is related to the C_{RSS} (reverse recovery capacitance), which is proportional to the quantity of the Q_{GD} [18]. Fig. 8(c) shows the reverse recovery time of the SW and the trench gate MOSFET. The depletion region stored charge of the body diode is removed during the time of the ta section, and the bulk material stored charge is removed during the tb section. According to Fig. 8(C), the recovery time of the SWFET is faster than that of the trench gate MOSFET. Because the gathered charge at the gate bottom is less than that of the trench gate MOSFET, the Q_{GD} is decreased. The SWFET showed an improved switching speed because of the short trr (reverse recovery charge). Low switching loss can be achieved in the DC-DC converter because the fast switching speed of the SWFET also causes a decrease in the switching loss.

2.6 Application: DC-DC buck converter

The DC-DC buck converter shown in Fig. 9 is designed for the application of a medium voltage MOSFET in the 40V class. Fig. 9 also compares the power efficiency of the SW and the trench gate MOSFET [19]-[20]. The input and output of the DC-DC buck convert for automotives are 24V and 5.5V respectively. Thus, the DC-DC buck converter in Fig. 9(a) is also designed at an input of 24V and an output of 5.5V.

Table 2. List of power efficiency parameter of SW and conventional trench gate MOSFET in DC-DC buck converter

Parameter	Trench MOSFET	SWFET
Input Power (input current * input voltage)	7.44W	6.24W
Output Power (output current * output voltage)	5.5W	5.5W
Power efficiency (output power/input power)	73.9%	88.1%

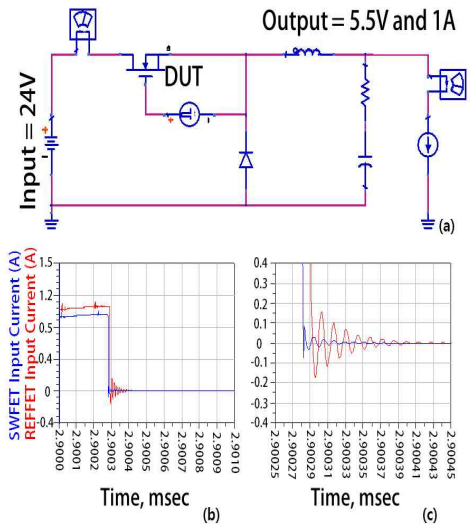

Fig. 9 Schematic circuit of (a) the DC-DC buck converter 24V input and 5.5V output, (b) input current pulse of SW and conventional trench gate MOSFET, (c) reverse recovery time of SW and conventional trench gate MOSFET

III. Conclusion

SWFET uses a thin poly-gate to reduce the overlapped gate-drain area and utilizes a thick gate bottom oxide for a reduced Q_{GD}. Consequently, the Q_{GD} and C_{RSS} are improved by 40% and 50%, respectively. Moreover, the switching performance of the inverter circuit was enhanced by 24.9%. When the SWFET was applied to a DC-DC buck converter, the power conversion shows improvements of 14.2%. As a result, the proposed SWFET is able to improve the switching performance of a DC-DC buck converter and switching circuit without any degradation in electrical performance. Furthermore, reduced energy consumption can be expected in various applications of energy conversion because the SWFET, which is a core technology in Green IT, decreases switching loss of the conventional Power MOSFET.

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BIOGRAPHY

Cho Doo-hyung (Member)

2011 : BS degree in Electrical and Electronic Engineering, Dankook University
2013 : MS degree in Electronic Engineering, Sogang University
2013 ~ present : PhD course in Electronic Engineering, Sogang University

Park Kun-sik (Member)

1991 : BS degree in Material science, KAIST
1996 : MS degree in Material science, KAIST
2011 : PhD degree in Material science, KAIST
2000 ~ present : Principle Researcher, ETRI

Kim Kwang-soo (Member)

1981 : BS degree in Electronic Engineering, Sogang University
1983 : MS degree in Electronic Engineering, Sogang University
1998 : PhD degree in Electronic Engineering, Sogang University
1983 ~ 1997 : Electronics and Telecommunications Research Institute (ETRI).
1998 ~ 2005 : Institute for Information Technology Advancement (IITA)
2005 ~ 2008 : Daegu Gyeongbuk Institute of Science and Technology (DGIST)
2008 ~ present : Professor, Electronic Engineering, Sogang University