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Control of Grid-Connected Inverters Using Adaptive Repetitive and Proportional Resonant Schemes

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Abstract

Repetitive and proportional-resonant controllers can effectively reject grid harmonics in grid-connected inverters because of their high gains at the fundamental frequency and the corresponding harmonics. However, the performances of these controllers can seriously deteriorate if the grid frequency deviates from its nominal value. Non-ideal proportional-resonant controllers provide better immunity to variations in grid frequency by widening resonant peaks at the expense of reducing the gains of the peaks, which reduces the effectiveness of the controller. This paper proposes a repetitive control scheme for grid-connected inverters that can track changes in grid frequencies and keep resonant peaks lined up with grid frequency harmonics. The proposed controller is implemented using a digital signal processor. Simulation and practical results are presented to demonstrate the controller capabilities. Results show that the performance of the proposed controller is superior to that of a proportional-resonant controller.

Key words: Adaptive frequency control, Grid-connected inverters, Proportional resonant control, Repetitive control

NOMENCLATURE

n	Number of samples in one fundamental cycle
N_{cpu}	PWM counter period
N_{cpu_o}	Nominal PWM counter period
T_{cpu}, f_{cpu}	DSP clock period and frequency
T_g, f_g	Grid voltage fundamental period and frequecny
T_{inv}, f_{inv}	Inverter modulating signal period and frequency
T_d	DSP computational time delay
T_s, f_s	Sampling period and frequency
T_{so}, f_{so}	Nominal sampling period and frequency
T_{sw}, f_{sw}	Switching period and frequency

I. INTRODUCTION

In grid-connected inverters (Fig. 1), classical proportional-integrator (PI) controllers suffer from relatively low loop gains at the fundamental frequency and the corresponding harmonics. As a result, the inverters that use these types of controllers tend to have poor grid harmonic disturbance rejections, which result in poor output current Total Harmonic Distortion (THD) if the grid voltage is heavily distorted. Different controllers and topologies have been proposed (e.g., [1]-[4]) to provide high-quality output currents that comply with national and international standards [5], [6]. Proportional-resonant (PR) controllers have also been widely used [7]-[13]. Theoretically, a PR controller has infinite gain at selected frequencies. Accurate tracking of the demanded current waveform can be achieved through having multiple PR controllers tuned at the fundamental frequency and its main harmonics. However, implementing such a controller in practice is complicated.

Repetitive control (RC) is widely used in many practical industrial systems, such as manufacturing [14], disk drives [15], and robotics [16]. RC has also been used in power electronics, such as uninterruptible power supplies [17], [18], active filters [19]-[21], DC/DC converters [22], [23], and grid-connected inverters [24], [25]. These controllers are based on the concept of iterative learning control, and error between the reference and the output over one fundamental cycle is used to generate a new reference for the next fundamental cycle. RC is mathematically equivalent to a

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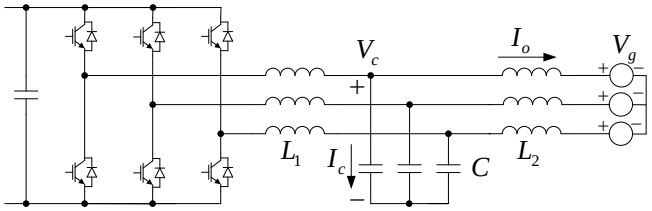

Fig. 1. Grid-connected inverter.

parallel combination of numerous resonant controllers, an integral controller, and a proportional controller [26]. Therefore, it is as effective as a PR controller at producing high-quality output currents in a grid-connected inverter, with the added advantage of being simpler and easier to implement. However, the performance of both PR and RC deteriorates significantly when the grid frequency deviates from the nominal value, because high-resonant gains will not match the fundamental frequency and the grid harmonics.

The frequency output from a phase-locked loop (PLL) can be used as input in PR controllers to have adaptive tuning with respect to the grid frequency, as suggested in [12] and [13]. However, all controller parameters must be adaptive, which makes the practical implementation of such mechanisms complicated, especially when a bank of resonant controllers is used to reject a high number of harmonics. Non-ideal PR controllers provide good immunity to variation in grid frequencies by widening resonant peaks at the expense of reducing the gains of the peaks. This phenomenon reduces the effectiveness of the controllers in tracking the demanded waveform [7].

The voltage control of grid-connected inverters with a frequency adaptive mechanism based on H∞ repetitive control was proposed in [24] and [25]. The internal model of the system consists of a delay unit $e^{-T_D s}$ that is cascaded with a low-pass filter, $W(s) = \omega_c/s + \omega_c$. The adaptive mechanisim is based on varying the cut-off frequency of the filter ω_c according to the varying grid frequency. According to the authors, this mechanism is effective for a grid frequency variation of only ±0.2 Hz. If the grid variation is higher than this limit, then the controller delay T_D must be changed. However, implementing an adaptive delay is impossible for low-sampling frequencies without further deterioration of the controller performance [24].

To overcome the deficiencies of conventional RC, this paper proposes an odd-harmonic frequency adaptive repetitive controller (ARC) for a grid-connected inverter suitable for implementation in a digital signal processor (DSP). The frequency adaptive feature is based on varying both switching and sampling frequencies according to the grid frequency, thus keeping the number of RC delay samples constant. This mechanism can precisely track changes in the grid frequency and keep the high-resonant gains lined up with the grid harmonics. The design procedure of the controller is explained in detail, and the practical DSP implementation of the proposed controller is also discussed. The performance of the proposed controller is compared to that of a PR controller and is found to be superior.

TABLE I
INVERTER PARAMETERS

Description	Symbol	Value
Inverter side filter inductor	L_1	350 µH
Filter capacitor	C	80 µF
Grid side filter inductor	L_2	50 µH
Nominal grid voltage	V_{go}	230 V (rms)
Inverter dc voltage	V_{dc}	700 Vdc
Nominal grid frequency	f_{go}	50 Hz
Nominal switching frequency	f_{swo}	8 kHz
Nominal sampling frequency	f_{so}	16 kHz
Computational time delay	T_d	10 µs

II. CONTROLLER STRUCTURE AND SYSTEM MODELING

Fig. 1 shows the circuit diagram of a conventional two-level, grid-connected inverter with an *LCL* filter. The inverter parameters used in this study are listed in Table I. Fig. 2 shows the block diagram that represents the control scheme implemented in each phase. The controller consists of an outer loop of the output current and an inner loop of the capacitor current to provide active damping. This structure increases the degree of freedom in designing the controller compared with the widely used one-feedback loop of L_1 current, because two controller gains (K_C and K) can be optimized instead of only one controller gain. A plug-in repetitive controller transfer function (G_{RC}) is implemented to reject the current harmonics that the grid voltage harmonics caused. The repetitive controller can reject the disturbance of the fundamental harmonic and its multiples. However, the convergence time of the repetitive controller is relatively long. Thus, a feedforward loop of the fundamental nominal component of the grid voltage is implemented to reduce the current error during the convergence time of the RC, which will be explained later. The controller in Fig. 2 has the form of $K + G_R(z)$ which means that it is proportional plus repetitive controller but it will be simply abbreviated as RC in this paper.

The block diagram of Fig. 2 can be simplified, as shown in Fig. 3(a). The transfer functions that appear in Fig. 3(a) are given by

$$G(s) = \frac{1}{L_1 L_2 C s^3 + (L_1 + L_2)s}, \quad (1)$$

$$H(s) = K_C L_2 C s^2, \quad (2)$$

$$B(s) = L_1 C s^2 + K_C C s + 1. \quad (3)$$

From Fig. 3a, $V_g(s)B(s)$ represents the disturbance that the grid voltage caused. Two options are available to reject this disturbance: RC and feedforward. Using RC to deal with grid

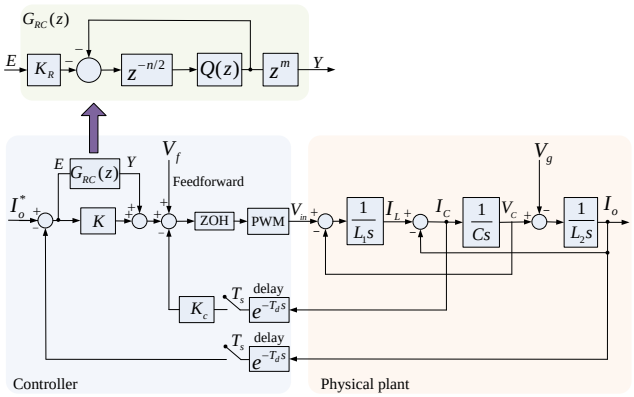

Fig. 2. Block diagram of one phase and its controller.

disturbance at the fundamental frequency means that at least one fundamental cycle (or half fundamental cycle in case of an odd-harmonic RC) delay will occur for the controller to feed the error that one fundamental cycle created back to the system for the next cycle. However, the error that the fundamental component of the grid voltage caused will be high and the inverter may generate a current several times the reference current during the first cycle. Considering the feedforward option, and to completely compensate for the grid disturbance, the feedforward loop should ideally have the form of $V_g(s)B(s)$, as seen in Fig. 3(a). The second derivative component L_1Cs^2 in Eq. (3) is small and can be neglected. Therefore, the feedforward of the component $(1+K_CCs)V_g$ should effectively reject grid disturbance. However, this action involves the differentiation of the grid voltage signal, which is undesirable in practice because of noise amplification.

To avoid differentiation in the feedforward and overcome the long delay of the RC, the proposed strategy involves using the feedforward to compensate for the disturbance that the fundamental frequency caused using a pre-known value of the nominal grid voltage and relying on the RC to compensate for the disturbance that all the other harmonics caused. Using the known nominal value of the grid rms voltage V_{go} and frequency f_{go}, the feedforward component that compensates for the fundamental component according to Eq. (3) (neglecting L_1Cs^2) is given in the following equation:

$$V_f = \frac{V_{go}}{\sqrt{2}}\sin(2\pi f_{go}t) + 2\pi f_{go}K_C C\frac{V_{go}}{\sqrt{2}}\sin(2\pi f_{go}t + \pi/2). \quad (4)$$

If the grid voltage is slightly different from its nominal value, the RC will compensate for the current error caused by this difference.

With a fully discretized system, Fig. 3(a) can be further simplified as Fig. 3(b). The disturbance $D_g(z)$ represents any grid disturbance that has not been compensated using the feedforward V_f. The physical plant discretized transfer function $G_p(z)$ can be calculated as

$$G_p(z) = \frac{G(z)}{1+GH(z)} \quad (5)$$

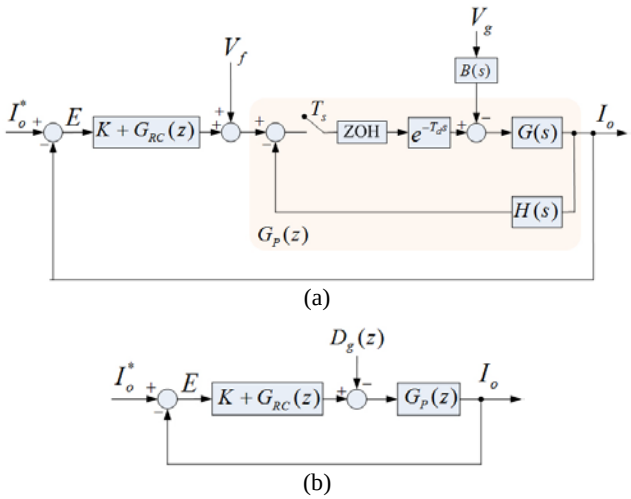

Fig. 3. Block diagram. (a) One phase and its controller. (b) Simplified block diagram.

where $G(z)$ and $GH(z)$ are the Z-transforms of $G(s)$ and $G(s)H(s)$ respectively, given the Zero-Order-Hold (ZOH) method with sampling time T_s and computational time delay T_d, such as

$$G(z) = Z\left(\frac{1-e^{-sT_s}}{s}e^{-sT_d}G(s)\right), \quad (6)$$

$$GH(z) = Z\left(\frac{1-e^{-sT_s}}{s}e^{-sT_d}G(s)H(s)\right). \quad (7)$$

The transfer function of the odd-harmonic RC is given in [27] as

$$G_{RC}(z) = -\frac{K_R z^m Q(z) z^{-n/2}}{1+Q(z)z^{-n/2}} \quad (8)$$

where $Q(z)$ is a low-pass filter, K_R is the RC gain, n is the number of samples in one fundamental cycle, and z^m is a non-causal phase lead unit.

III. System Analysis and Controller Design

The controller design involves the determination of K_C, K, $Q(z)$, K_R, and m. From Fig. 3(b), the error signal E can be expressed as

$$E(z) = \frac{I_o^*(z) + D_g(z)G_p(z)}{1+KG_p(z)+G_p(z)G_{RC}(z)}. \quad (9)$$

Substituting Eq. (8) into Eq. (9) and rearranging gives

$$\frac{E(z)}{I_o^*(z)+D_g(z)G_p(z)} = \frac{\left(1+z^{-n/2}Q(z)\right)}{\left(1+KG_p(z)\right)\left(1-z^{-n/2}R(z)\right)} \quad (10)$$

where

$$R(z) = Q(z)\left(\frac{K_R z^m G_p(z)}{1+KG_p(z)} - 1\right). \quad (11)$$

The block diagram in Fig. 4 can represent Eq. (10). This diagram consists of three cascaded transfer functions: $T_1(z)$,

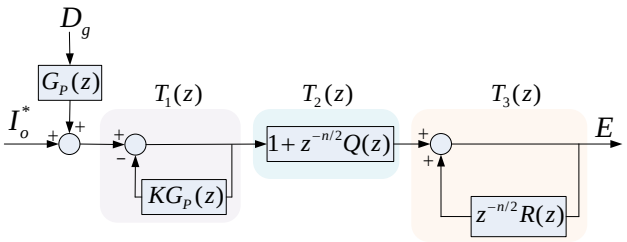

Fig. 4. Block diagram of the system error.

$T_2(z)$, and $T_3(z)$. $T_1(z)$ is the closed-loop transfer function without the repetitive controller, and stability can be guaranteed through choosing K_C and K. The stability of the second transfer function $T_2(z)$ can be guaranteed through choosing a stable low-pass filter $Q(z)$. The stability of the third transfer function $T_3(z)$, which contains a positive feedback loop, can be guaranteed using the small gain theorem, i.e., the error signal will be bounded if the magnitude of the open-loop transfer function is less than 1 for all values of frequencies. Therefore,

$$\left\|R(z)\right\|_\infty < 1. \tag{12}$$

A. Selection of K_C and K

If RC is not implemented, then the selection of the capacitor current loop gain K_C and the output current loop gain K will be a compromise between good stability margins and good harmonics rejection; increasing K_C will improve stability but will worsen harmonics rejection, whereas increasing K will worsen stability but will improve harmonics rejection [3]. In this study, the RC will handle harmonics rejection, and thus choosing K_C and K is important to maximize the stability margins. The gains K_C and K are chosen to provide good stability margins for $T_1(z)$. Typical control system design criteria are used: phase margin between 40º to 70º and damping ratio from 0.3 to 0.7. The gains K_C and K have been set to 5 and 3 respectively through analyzing $G_p(z)$ in Matlab SISO Design Tool. This selection gives the following criteria: gain margin = 5.6 dB, phase margin = 51º, damping ratio $\zeta = 0.33$, and settling time $t_s = 0.5$ ms.

B. Selection of $Q(z)$

The Bode diagram of the open-loop transfer function $(K + G_{RC}(z))G_p(z)$ with, $Q(z)$ =1 is shown in Fig. 5. The system is unstable because of the resonant peaks near the crossover frequency, which means that $Q(z)$ must be modified to attenuate the high-frequency peaks. A zero-phase low-pass filter is used, which has the following structure [28]:

$$Q(z) = \frac{\alpha_1 z + \alpha_o + \alpha_1 z^{-1}}{\alpha_o + 2\alpha_1},\ 0 < \alpha_o, \alpha_1 < 1. \tag{13}$$

Setting $z = e^{j\omega T_s}$ (T_s is the sampling period) in Eq. (13) can obtain the frequency response of $Q(z)$ as

$$Q(e^{j\omega T_s}) = \frac{1}{\alpha_o + 2\alpha_1}\left[\alpha_o + \alpha_1\left(e^{j\omega T_s} + e^{-j\omega T_s}\right)\right]. \tag{14}$$

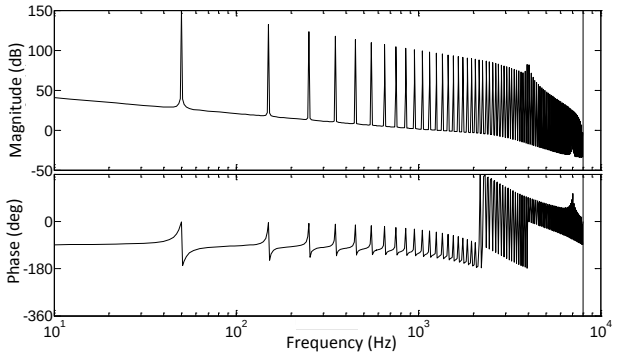

Fig. 5. Bode diagram of the open-loop transfer function $(K + G_{RC}(z))G_p(z)$, with $Q(z) = 1$, m=1, $K_R = 0.5$.

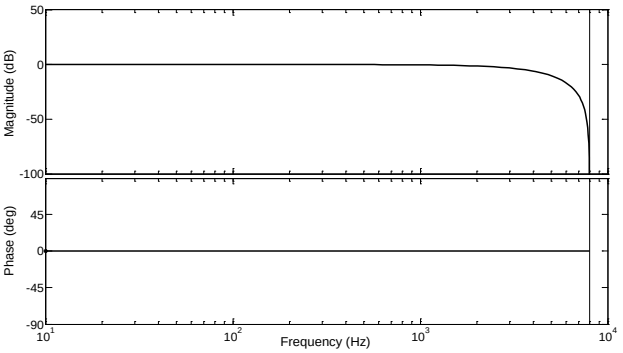

Fig. 6. Bode diagram of $Q(z) = 0.25z+0.5+0.25z^{-1}$.

Therefore,

$$Q(e^{j\omega T_s}) = \frac{1}{\alpha_o + 2\alpha_1}\left[\alpha_o + 2\alpha_1 \cos(\omega T_s)\right]. \tag{15}$$

From Eq. (15), the magnitude $\left|Q(j\omega T_s)\right|$ can be written as

$$\left|Q(e^{j\omega T_s})\right| = \frac{1}{\alpha_o + 2\alpha_1}\begin{cases}\alpha_o + 2\alpha & \omega T_s = 0\\ \alpha_o + 2\alpha_1\cos(\omega T_s) & 0 < \omega T_s < \pi\\ \alpha_o - 2\alpha_1 & \omega T_s = \pi\end{cases}. \tag{16}$$

In order to get a unity gain at zero frequency then α_o and α_1 must be chosen to satisfy $\alpha_o + 2\alpha_1 = 1$ to obtain a unity gain at zero frequency. α_o and α_1 must also be chosen to satisfy $\alpha_o - 2\alpha_1 = 0$ to obtain zero gain at high frequencies $\omega T_s > \pi$. Therefore, α_o and α_1 are set to 0.5, and 0.25, respectively. For the full frequency range, $\left|Q(e^{j\omega T_s})\right|$ is given through

$$\left|Q(e^{j\omega T_s})\right| = 0.5 + 0.5\cos\left(\omega T_s\right). \tag{17}$$

The filter is now given through

$$Q(z) = \alpha_1 z + \alpha_0 + \alpha_1 z^{-1}. \tag{18}$$

The Bode diagram of $Q(e^{j\omega T_s})$, as described in Eq. (17), is shown in Fig. 6. The Bode diagram of the open-loop transfer function $(K + G_{RC}(z))G_p(z)$ with, $Q(z)$, as described in Eq. (18), is shown in Fig. 7. This diagram confirms the stability of the system as the high gains near the crossover frequency are attenuated, and the system has positive stability margins.

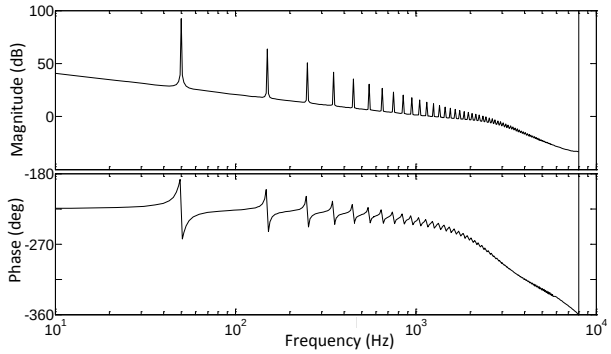

Fig. 7. Bode diagram of the open-loop transfer function $(K + G_{RC}(z))G_p(z)$, with $Q(z)$ = 0.25z+0.5+0.25z^{-1}, m=1, K_R = 0.5 (GM = 5.0dB, PM = 44.1°).

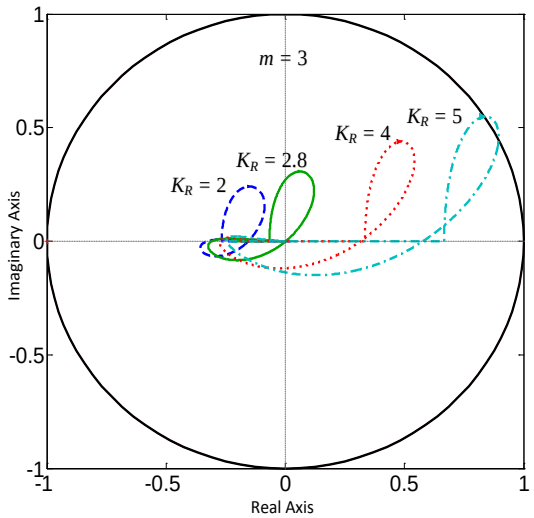

Fig. 8. Locus of the vector $|R(e^{j\omega T_s})|$.

C. Selection of K_R and m

The value of the RC gain K_R must be carefully selected because it is a key parameter for error convergence and system stability. A high RC gain K_R results in fast error convergence, but the feedback system becomes less stable. The non-causal phase lead unit of m is normally used to compensate for any delay or phase lag from the physical plant and controller transfer function. Implementing z^m is not possible in practice unless z^m is cascaded with the delay units of the RC. The design criterion used in this study maximizes K_R to reduce RC convergence time while minimizing $\|R(z)\|_\infty$ to increase stability margins. Fig. 8 shows the locus of vector $|R(e^{j\omega T_s})|$ for different values of K_R when m = 3. As K_R increases, the stability margin decreases until the system becomes unstable when K_R > 4.8 because $|R(e^{j\omega T_s})|$ becomes greater than unity. In Fig. 9, $\|R(z)\|_\infty$ is plotted against K_R and m. For m = 0, the system is only stable when K_R < 0.6 ($\|R(z)\|_\infty$ = 0.99 when K_R = 0.6). This result indicates poor stability. Increasing m improves stability, and the best value is obtained when m = 3 because this value corresponds to the lowest possible $\|R(z)\|_\infty$. The minimum

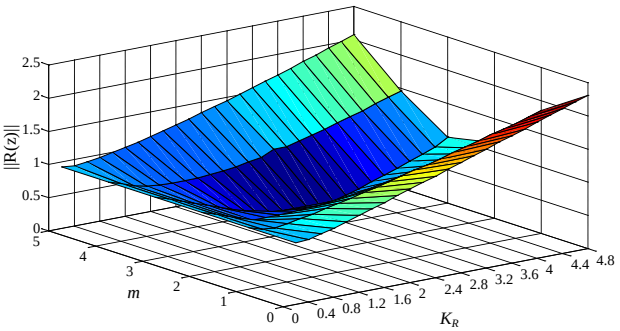

Fig. 9. $\|R(z)\|_\infty$ versus K_R and m.

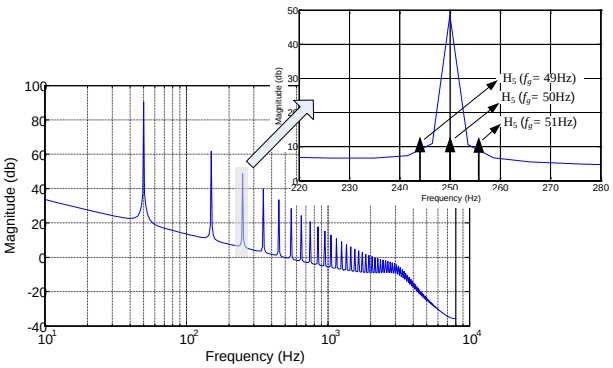

Fig. 10. Effect of grid frequency variation.

value for $\|R(z)\|_\infty$ occurs when K_R = 2.8 and m = 3. These values were thus chosen for this design.

IV. Frequency Adaptive RC

In this section, a frequency adaptive RC is proposed to track the variations in grid frequency.

A. Effect of grid frequency variation on RC performance

RC is equivalent to a parallel combination of resonant controllers with high gain at the fundamental frequency and its harmonics. It is implemented in this study to reject inverter output current harmonics that the presence of grid voltage harmonics causes. However, the grid frequency can vary with time because of the variation of loads or the connection or disconnection of large generators. Typically, grid frequency can oscillate by ±2%. Fig. 10 shows the Bode diagram of the open-loop transfer function of the system. The magnified portion of the diagram shows the resonant peak around the fifth harmonic. The benefit from this high gain occurs when the fifth harmonic is exactly 250 Hz. However, if the grid frequency changes by ±2%, the resonant peak will not align with the fifth harmonic and consequently the RC becomes ineffective. The linearized inverter model described in Fig. 2 is simulated in Matlab/Simulink with the PWM block set to unity gain. Some grid harmonics are included in the grid voltage V_g, and four causes are simulated for different grid frequencies f_g. The simulation results of the

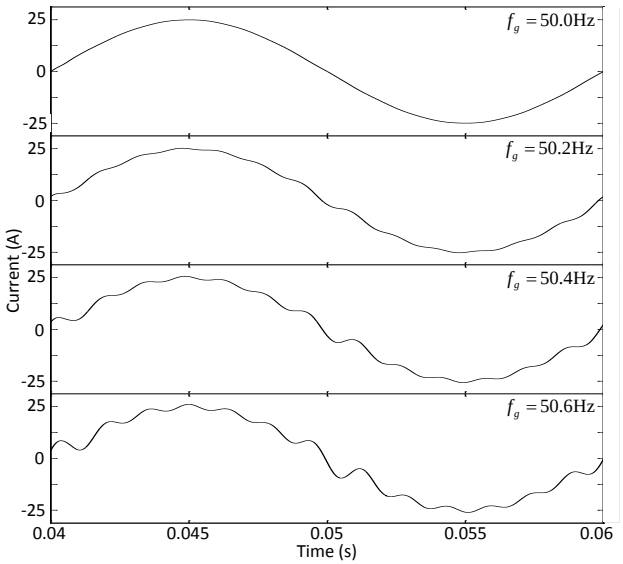

Fig. 11. Simulated output current for different grid frequencies.

output current after the RC converged are shown in Fig. 11. The performance of RC deteriorates dramatically when the grid frequency deviates from the nominal value. To remain effective, RC has to adapt to the varying grid frequency.

B. Proposed Frequency Adaptive Controller

The performance of the RC is not guaranteed unless the high-resonant gains align with the grid harmonics. Therefore, the time delay of the repetitive controller must adapt to the changes in the fundamental period of the grid voltage. The number of delay samples *n* can be changed with respect to the grid frequency. However, this mechanism will not result in a precise control of the time delay that RC used unless the switching frequency (and hence the sampling frequency) are high with respect to the fundamental frequency. For example, the number of samples per cycle is 4000/50 = 80 samples when the sampling frequency is 4 kHz, for a fundamental frequency of 50 Hz. Each sample is equivalent to 0.253 ms, which means that the minimum change in grid frequency this scheme can handle is approximately 0.63 Hz. According to the Bode diagram in Fig. 10, the RC gain at the fifth harmonic reduces by about 20% of the corresponding nominal value when the grid frequency deviates by only 0.15 Hz from the nominal value. For a 0.60 Hz deviation, the RC becomes completely ineffective. Fig. 11 also shows that the deterioration in RC performance begins to be noticeable when the grid frequency deviates by only 0.2 Hz from the nominal value. Therefore, varying the number of samples will not provide good tracking of the grid frequency without deteriorating the RC performance. The mechanism proposed in this study is to change the switching and sampling frequencies with respect to the grid frequency. The ratio of the sampling frequency to the fundamental frequency remains constant, and thus *n* does not need to change. Considering that the grid frequency can vary by up to ±2%, the sampling

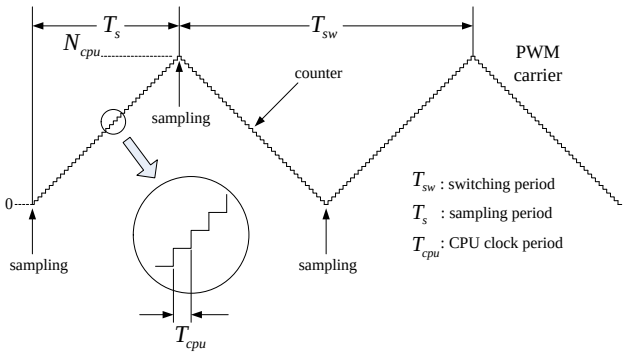

Fig. 12. PWM implementation in the DSP.

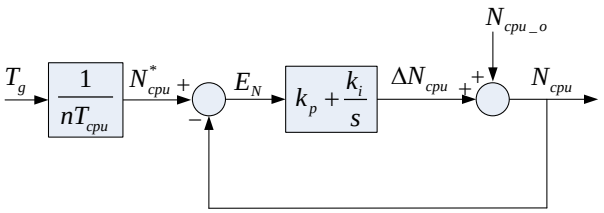

Fig. 13. PWM period control.

and switching frequencies can vary using the same ratio. Therefore, the switching frequency can vary from 7.84 kHz to 8.16 kHz. The attenuation of the *LCL* filter will change as the switching frequency varies within this range.

This mechanism benefits from the high precision of the DSP clock used to implement the controller. Fig. 12 shows the implementation of the PWM carrier in the DSP. In this study, the sampling frequency f_s is set to twice the switching frequency, such as $f_s = 2 f_{sw}$. A counter based on the central processing unit (CPU) clock is set to count up and down periodically. The PWM counter period N_{cpu} is set to determine the required sampling period. Therefore,

$$N_{cpu} = T_s / T_{cpu} \tag{19}$$

where T_s and T_{cpu} are the sampling and CPU clock periods respectively. The number of samples *n* per fundamental cycle is given through

$$n = T_g / T_s \tag{20}$$

where T_g is the grid voltage fundamental period. The inverter modulating signal period is given using

$$T_{inv} = nT_s . \tag{21}$$

Substituting Eq. (19) into Eq. (21) gives

$$T_{inv} = nN_{cpu}T_{cpu} \tag{22}$$

According to Eq. (22), in order to vary the modulating signal period T_{inv} of the inverter, and hence the frequency f_{inv}, while maintaining *n* constant, the number of counts N_{cpu} should be changed.

Fig. 13 shows the proposed controller of the PWM counter period N_{cpu}. The grid voltage fundamental period T_g is sensed (using a PLL or zero crossing detector) and divided by nT_{cpu} to calculate the demand PWM counter period N^*_{cpu}. The period error E_N is fed into a PI controller to calculate for

ΔN_{cpu}, which is added to the nominal PWM counter period N_{cpu_o} to produce N_{cpu}. The nominal PWM counter period N_{cpu_o} is calculated in Eq. (23):

$$N_{cpu\_o} = T_{so} / T_{cpu} \tag{23}$$

where T_{so} is the nominal switching period.

To highlight the advantage of this mechanism over changing n, we consider the case where the CPU frequency f_{cpu} =150 MHz, n = 320, and the nominal switching frequency f_{so} = 16 kHz. According to Eq. (23), the nominal PWM counter period N_{cpu_o} = 150 MHz/16 kHz = 9375. If the inverter modulating signal frequency f_{inv} is controlled through varying n, then when reducing n by 1 count, f_{inv} will be given by

$$f_{inv} = \frac{150\text{MHz}}{(320-1)*9375} = 50.1567 \text{ Hz}. \tag{24}$$

However, if f_{inv} is controlled through varying N_{cpu} as proposed in this study, then when reducing N_{cpu} by 1 count, f_{inv} will be

$$f_{inv} = \frac{150\text{MHz}}{320*(9375-1)} = 50.0053 \text{ Hz}. \tag{25}$$

Varying N_{cpu} gives 29 times more precision in controlling the frequency.

C. Frequency Controller Design

According to most of the grid codes of practice, the grid frequency variation has a maximum slope of 1 Hz/s [12], which is nearly equivalent to an approximate 0.4 ms/s increase or decrease of grid period. The design objective is to track this variation and maintain the error signal between the PWM counter period N_{cpu} and its demand N^*_{cpu} to the minimum of one count. The deviation in grid frequency, and hence the PWM counter period demand N^*_{cpu}, will be modeled as a ramp function:

$$N^*_{cpu} = D / s^2 \tag{26}$$

where D is the rate of change of N^*_{cpu} in count/s. From Fig. 13, the error E_N (error signal between the PWM counter period N_{cpu} and its demand N^*_{cpu}) is given through the following equation:

$$E_N(s) = \frac{N^*_{cpu} - N_{cpu\_o}}{1 + (k_p + \frac{k_i}{s})}. \tag{27}$$

The steady-state error E_{Nss} for a ramp input of N^*_{cpu} can be calculated through substituting Eq. (26) into Eq. (27) and using the final-value theorem, such as

$$E_{Nss} = \lim_{s\to 0}(sE_N) = D / k_i. \tag{28}$$

Maximum D is 184 count/s (equivalent to 0.4 ms/s). The integral gain k_i is chosen to give the minimum possible steady-state frequency error, which is one count. Therefore k_i is set to 184. The proportional gain k_p is normally set to deal with transient response to a step input, In this case, a step change in grid frequency is unlikely and the proportional gain is set to 10.

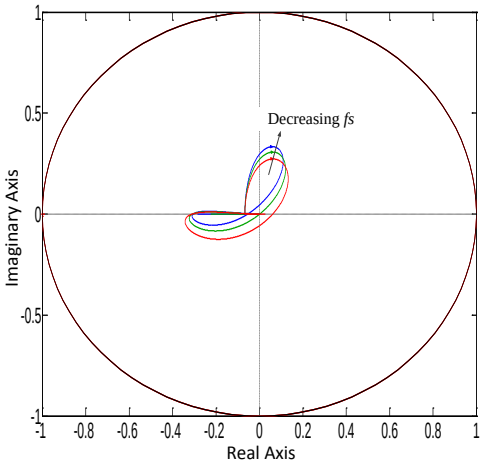

Fig. 14. Effect of different sampling frequencies on $\|R(z)\|_\infty$, f_s = 15.7, 16.0, and 16.3 kHz, K_R=2.8, m=3.

D. Effect of Varying Sampling Frequency on System Stability

Checking the effect of varying sampling frequencies on the stability of the repetitive controller is essential. Fig. 14 shows how $\|R(z)\|_\infty$ varies for three different sampling frequencies that correspond to the nominal +2%, and -2% deviation in grid frequency. The effect of changing the sampling frequency on the stability of the ARC is minimal, and $\|R(z)\|_\infty$ is inside the unit circle. The stabilities of $T_1(z)$ and $T_1(z)$ are not affected by varying the sampling frequency.

V. Design of a Proportional Resonant Controller

To compare the performance of the proposed ARC with other controllers reported in the literature, a PR controller is designed for the same inverter considered in this study. PR controller has been widely considered for its ability to reject harmonics by creating high-resonant peaks at specific frequencies. The ideal resonant controller is given in the following equation:

$$G_{Ri}(s) = \frac{2K_h s}{s^2 + \omega_h^2} \tag{29}$$

where ω_h is the selected harmonic frequency that must be compensated, and K_h is the controller gain. Eq. (29) gives infinite gain at ω_h. To avoid stability problems that may arise because of the infinite gain, a non-ideal resonant controller can be used as suggested in [7]:

$$G_R(s) = \frac{2K_h \omega_c s}{s^2 + 2\omega_c s + \omega_h^2} \tag{30}$$

where ω_c is the cut-off frequency of the non-ideal resonant controller. The insertion of ω_c reduces the resonant peaks and widens their bandwidth, causing the controller to be less sensitive to frequency variations. The use of several resonant controllers that are tuned to the desired odd-harmonic frequencies can create a resonant controller, such as

TABLE II
PROPORTIONAL RESONANT CONTROLLER GAINS

K_1	K_3	K_5	K_7	K_9	K_{11}	K_{13}	K_{15}	K_{17}	K_{19}
110	100	90	80	70	60	50	40	30	20

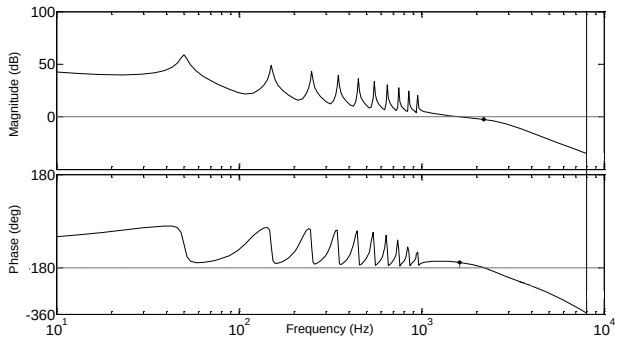

Fig. 15. Bode diagram of the open-loop transfer function $(K + G_{Rh}(z))G_p(z)$, (GM = 2.5 dB, PM = 21.0º).

$$G_{Rh}(s) = \sum_{h=1,3,5}^{H} \frac{2K_h\omega_c s}{s^2 + 2\omega_c s + \omega_h^2}. \quad (31)$$

A bank of resonant controllers that are tuned to the low-order odd-harmonics up to H=19 is used. The design involves the determination of the cut-off frequency ω_c and the controller gains K_h. A low value of ω_c will make the controller sensitive to frequency variation and difficult to implement in a fixed point DSP [7], whereas a high value of ω_c will reduce the resonant peaks and, hence, the controller performance. In practice, a ω_c value of 5–15 rad/s is found to provide a good compromise [29]. In this design, ω_c is set at 10 rad/s. The gains K_h are chosen to provide a good compromise between stability and performance. High gains will increase resonant peaks and thus improve harmonics rejection. However, the high gains will also left the open-loop Bode diagram up which will reduce the stability margins. The gains are set to reduce gradually as h increases so as to reduce the effect of the resonant peaks in the vicinity of the crossover frequency and thus reduce the effect on the stability margins. The gains K_h that were used are shown in Table II.

The resonant controller is discretized using the bilinear Tustin transformation [30], such as

$$G_{Rh}(z) = G_{Rh}(s)\big|_{s=\frac{2}{T_s}\frac{z-1}{z+1}}. \quad (32)$$

The PR controller is obtained through adding the proportional gain K to $G_{Rh}(z)$. The Bode diagram of the open-loop transfer function $(K + G_{Rh}(z))G_p(z)$ is shown in Fig. 15. The gain margin and the phase margin of this design are 2.5 dB and 21.0º respectively.

VI. SIMULATION RESULTS

A detailed simulation model of the three-phase inverter is presented in Fig. 1, which was built using the MATLAB SimPowerSystems. The inverter parameters are listed in Table I. The grid voltage harmonics were measured in the laboratory, and similar values were included in the simulation model. The total grid voltage THD was measured to be 1.9%. The controller parameters for the RC and ARC used in the simulation are listed in Table III. The simulation parameters for the resonant controller are the same as the ones listed in Table II.

TABLE III
CONTROLLER PARAMETERS

	Description	Symbol	Value
Inner Controller	Output current feedback gain	K	3
	Capacitor current feedback gain	K_C	5
RC	RC gain	K_R	2.8
	Non-causal phase lead	m	3
	Number of samples in one cycle	n	320
	Filter $Q(z)$ coefficient 1	$\propto_0$	0.5
	Filter $Q(z)$ coefficient 2	$\propto_1$	0.25
ARC	CPU frequency	f_{cpu}	150 MHz
	Nominal CPU timer period	N_{cpu_o}	9375
	Frequency control proportional gain	k_p	10
	Frequency control integral gain	k_i	184

A. Performance Comparison between P, PR, and RC at a Fixed Grid Frequency

In this section, a performance comparison is conducted between three different controllers: Proportional (P), PR, and RC. Fig. 16 shows the output current with the P controller for a 14A (rms) demand. The output current THD is 14.2%. The magnitude and phase angle of the 50 Hz fundamental component are 8.3A and -7.9º respectively. Fig. 17 shows the output current with the PR controller. The current THD is 2.6%. The magnitude and phase angle of the 50 Hz fundamental component are 13A and +8.0º respectively. Fig. 18 shows the output current with RC after the controller converged. The current THD is reduced to only 0.8%. The magnitude and phase angle of the 50 Hz fundamental component are 14A and -0.9º respectively. The effectiveness of the RC in improving the current THD and reference tracking is noticed. Fig. 19 shows the grid voltage harmonics used in the simulation model, and Fig. 20 shows the output current harmonics with P, PR, and RC.

B. Performance Comparison between PR, RC, and ARC at Varying Grid Frequencies

To test the effectiveness of the ARC, the grid frequency is set to change from 50 Hz to 50.2 Hz at the simulation time t = 0.1 s. The slope of change is 1 Hz/s. Fig. 21 shows the output current THD with PR, RC, and ARC. The THD is measured using a built-in Simulink block.

With PR, the THD increased with frequency deviation and reached 3.5% before dropping to 2.8% when the grid frequency settled at 50.2 Hz. With RC, the current THD increased as the frequency deviation increased and reached

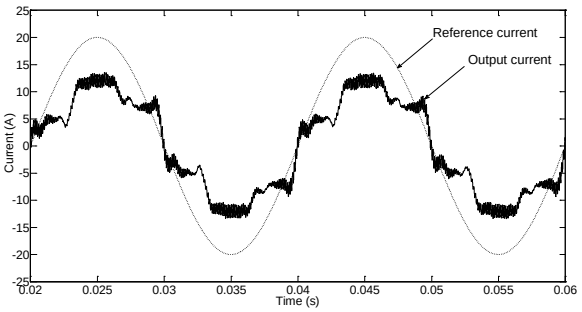

Fig. 16. Simulated steady-state output current with only a proportional controller (THD = 14.2%).

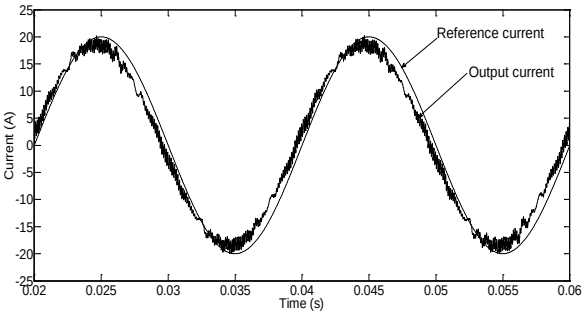

Fig. 17. Simulated steady-state output current with PR (THD = 2.6%).

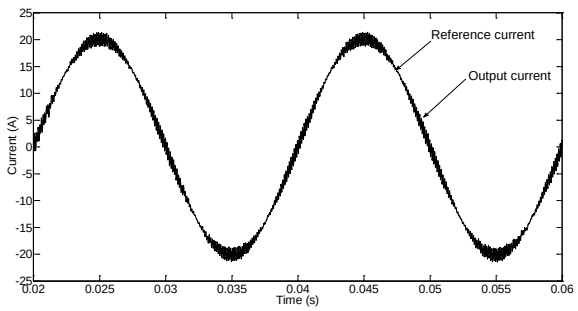

Fig. 18. Simulated steady-state output current with RC (THD = 0.8%).

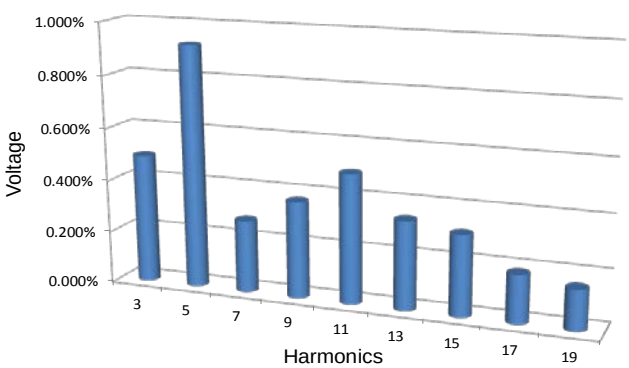

Fig. 19. Grid voltage harmonics (percentage of fundamental).

3.2%. Once the grid frequency reached 50.2 Hz and stopped deviating, the THD dropped to 1.8%. The ARC was able to keep the output current THD at 0.8% at all times.

Fig. 22 shows how the steady-state output current THD

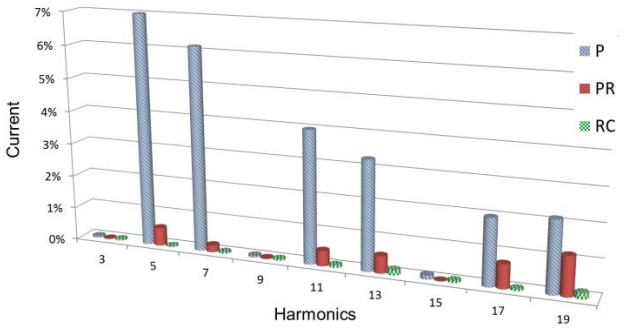

Fig. 20. Output current harmonics (percentage of fundamental).

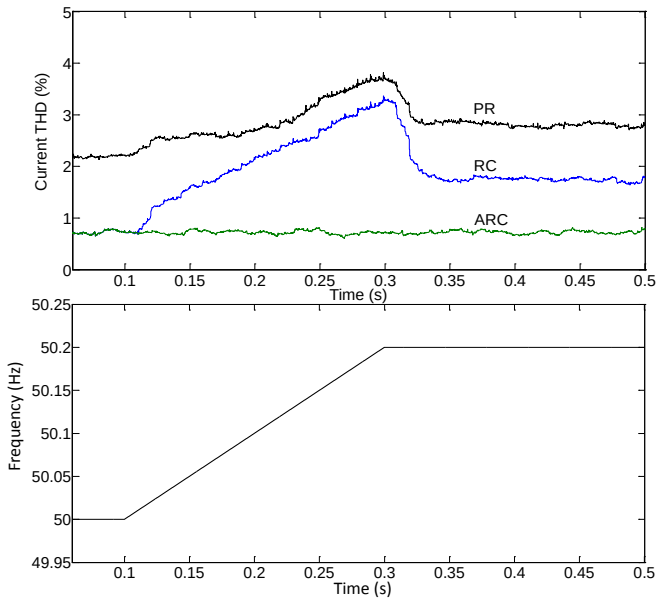

Fig. 21. Output current THD (Grid frequency started to change from 50 Hz to 50.2 Hz at t = 0.1s with a slope of 1 Hz/s).

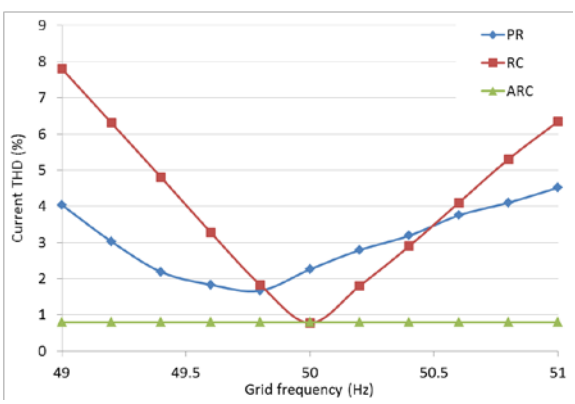

Fig. 22. Output current THD versus grid frequency.

varies as the grid frequency deviates by ±2%. The PR is less sensitive to the variation in grid frequency than RC because PR has wider resonant peaks. The lowest THD with PR occurs at 49.8 Hz, not at 50.0 Hz, because of the quantization error of the discretization process. The superiority of ARC over PR and RC is clear because ARC can always keep the

THD low regardless of the variation in grid frequency.

VII. Practical Implementation and Experimental Results

The proposed RC was tested experimentally with the grid-connected inverter described in Fig. 1 and Table I. The control parameters are listed in Table III. The controller was implemented using a Texas Instrument TMS320F2812 32-bit fixed point DSP. The three-phase reference sine waves were generated internally through the DSP using lookup tables of n = 320 samples. The sine wave amplitude was set externally (using a setting in the user interface) and sent via Controller Area Network (CAN)-bus. The input DC was regulated using an external boost circuit to 700V dc, and thus the current could be injected into the 230 Vrms grid.

The RC controller was realized through programming as follows. From Eq. (8), the discrete transfer function that relates the RC output $Y(z)$ to the RC input $E(z)$ is given in the following equation:

$$\frac{Y(z)}{E(z)} = -\frac{K_R z^m Q(z) z^{-n/2}}{1+Q(z)z^{-n/2}}. \tag{33}$$

Substituting Eq. (18) into Eq. (33) and rearranging gives

$$Y(z) = X(z)\left(\alpha_1 z^{1+m-n/2} + \alpha_0 z^{m-n/2} + \alpha_1 z^{m-n/2-1}\right) \tag{34}$$

where $X(z)$ is given in the following equation:

$$X(z) = -z^{-m}Y(z) - K_R E(z). \tag{35}$$

Eqs. (34) and (35) represent the indirect (standard) realization of digital controllers [30], which is represented in Fig. 23. The RC controller is implemented in a software through creating three arrays $x(i)$ (one per phase), in which each is 160 (320/2) entries long. At the discrete time i, the RC output $y(i)$ is calculated using the difference equation (36), and the array entry $x(i)$ is filled using the difference equation (37)

$$y(i) = \alpha_1 x(i+1+m-n/2) + \alpha_0 x(i+m-n/2) + \alpha_1 x(i-1+m-n/2) \tag{36}$$

$$x(i) = -y(i-m) - K_R e(i) \tag{37}$$

where $e(i)$ is the current error at discrete time i.

A high-precision measurement of grid voltage frequency is required to implement the proposed frequency adaptive control. The grid voltage signal is sensed, and the Positive-Going Zero Crossing (PGZC) is detected. The fundamental period of the grid voltage T_g is measured through calculating the number of samples between two consecutive PGZCs.

To increase the measurement accuracy, the PGZC is detected every 15 fundamental cycles. In this way, the measurement error is reduced to T_s/15 (compared with T_s if the PGZC is detected every cycle). For the nominal sampling frequency of 16 kHz, the measurement error is only ±62.5 μs/15 = ±4.16 μs, which is equivalent to ±0.01 Hz.

Fig. 24 shows the output current when the RC is deactivated (i.e., proportional only controller P). The demand

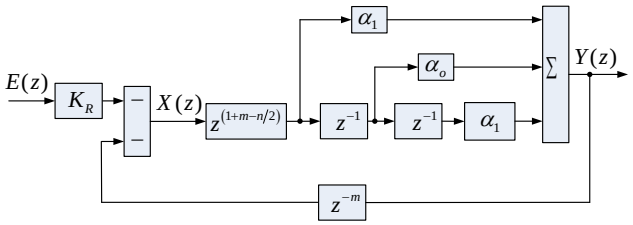

Fig. 23. RC Implementation.

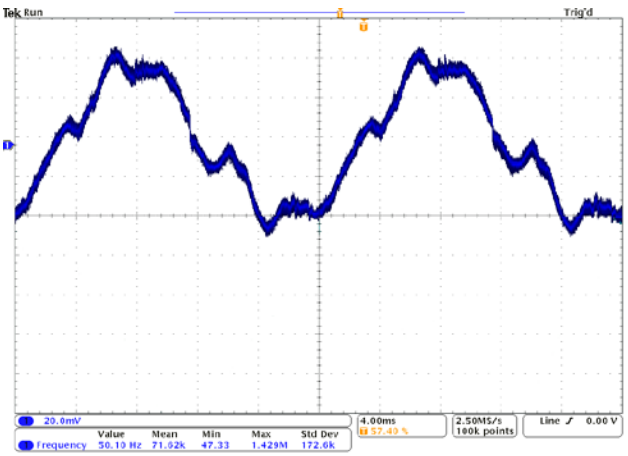

Fig. 24. Output current without RC (10 A/div).

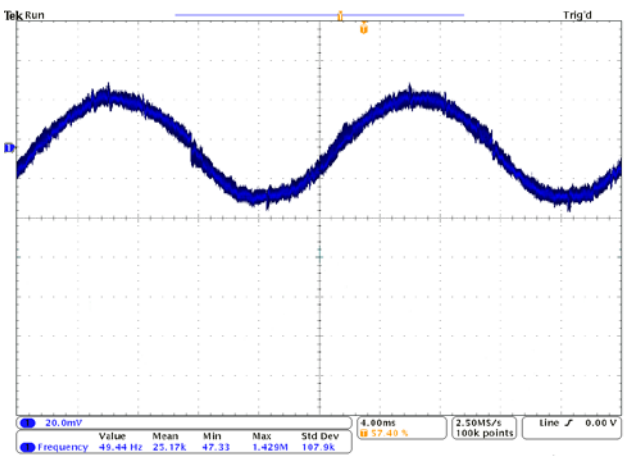

Fig. 25. Output current with RC (10 A/div).

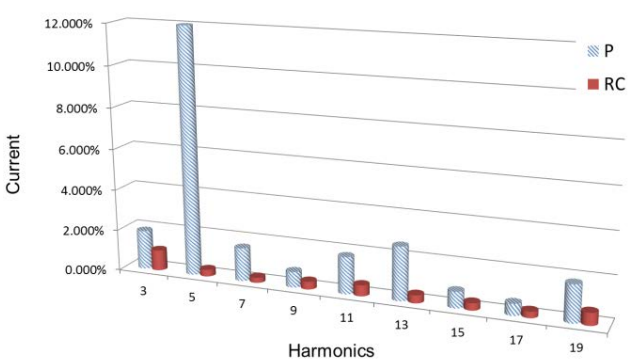

Fig. 26. Experimental output current harmonics.

current is set to 15 A (rms). The current THD is measured to be 13.0%. Fig. 25 shows the output current when the RC is activated. The current THD is measured to be only 1.1%. Fig. 26 shows the measured output current harmonics with both P and RC.

The grid frequency was monitored in the laboratory, and the maximum deviation recorded was ±0.1 Hz. The current THD was always maintained below 1.2%. To test the performance of the ARC against higher grid frequency deviation, an AC voltage source would need to be used to emulate the grid.

VIII. CONCLUSION

The design and practical implementation of a frequency adaptive and odd-harmonic RC for a grid-connected inverter was discussed. The adaptive mechanism was found to be effective in tracking the changes in grid frequency and, therefore, in maintaining the effectiveness of the RC. The performance of the proposed controller was found to be superior to that of proportional resonant controller. The proposed mechanism presents a straightforward implementation using a DSP system.

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