JPE 15-2-15

http://dx.doi.org/10.6113/JPE.2015.15.2.443
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

A Load Compensator Based on One-Cycle Control with Plug-In Repetitive Control

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Abstract

This study proposes a novel one-cycle control scheme with a plug-in repetitive controller for load compensator. The novelty of this scheme lies in the combination of high dynamics and the simplicity of a one-cycle controller and good steady-state harmonic suppression ability of the repetitive controller. In addition, the proposed scheme can reduce the effect of the harmonics in phase voltage for the existence of the repetitive controller. Finally, experimental results on a three-phase, four-wire, three-level load compensator are reported to validate the effectiveness of the proposed control scheme.

Key words: Harmonic filters, Load compensator, One-cycle control, Repetitive control

I. INTRODUCTION

Development of the power system has resulted in a huge growth in nonlinear loads, such as adjustable speed drives, electric arc welders, and switching power supplies, which usually generate large amounts of harmonic currents in both industrial and domestic fields. Consequently, line current harmonics is one of the greatest challenges in power systems because it causes voltage distortion and increases power loss [1], [2].

An easy solution to this problem is to employ a passive filter. However, such filters are often heavy, large in size, and can be easily affected when the impedance of the grid changes [3]. In contrast, a load compensator (LC) is a better solution because of its smaller size and weight compared with the passive filter, as well as its insensitiveness to the grid parameters [1]-[3].

The goal of LC is to generate a current with the same magnitude but the opposite phase to the harmonic that the nonlinear loads generated. A typical controller for LCs consists of two parts: a harmonic extractor that extracts the harmonic components of load currents to generate the reference for the current controller, and a double-loop controller that forces the output current of the LC to follow the reference and controls the DC-link voltage [4], [5]. Therefore, both current controller and harmonic extractor can affect LC performance. The harmonic extractor has already been widely employed by filters [6]-[8]; schemes based on the instantaneous reactive power theory [9] or Discrete Fourier Transformation (DFT) [10]. However, all these schemes have problems in balancing the steady-state and transient performance of its output. Thus, the harmonic extractor degrades both the accuracy and the transient behavior of LCs.

Alternatively, an indirect method is introduced in [11]-[13], where the line current is sensed and sinusoidally regulated as the same phase of the grid voltage. Without the harmonic extractor, this scheme is free from tracking errors and delays that the harmonic extractor causes and can be implemented with only one set of current sensors. However, an additional set of high-performance voltage sensors for the grid voltage is needed because the reference of the current is generated directly from the grid [12] or from the d-q reference frame that needs the information from the grid [13].

One-cycle control (OCC) based LCs [14]-[16] do not explicitly require information on the grid and load current; thus, these LCs can be implemented with only line current sensors and DC-link voltage sensors. Moreover, semiconductor devices operate at a constant switching frequency, which simplifies the design of the output filter. However, the control bandwidth of OCC based LC is limited because its bandwidth is equivalent to a proportional controller that forces the current to follow the waveform of the grid voltage. A detailed model of OCC based LC will be discussed in section II. Therefore, the OCC based LC cannot compensate high order harmonics, and can be easily

Manuscript received Jul. 16, 2014; accepted Dec. 2, 2014
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affected by distorted grid voltage.

The design of the current controller becomes a challenging task because LCs need to generate a high-order harmonics current. The bandwidth of the current loop has to be sufficiently wide. In the literature, various current controllers have been developed, such as proportional-integral (PI) control [17], [18], hysteresis control [19], [20], proportional-resonant (PR) control [21], [22], and vector PI (VPI) control [23], [24]. The bandwidth of PI control is limited, which is making it unsuitable for LCs. Although hysteresis control is simple and robust, it also has flaws—the varying switching frequency poses huge difficulty difficulties in the design of the output filter. Moreover, hysteresis control also has problems in balancing the accuracy of the current output and switching frequency. The PR controller can provide a high bandwidth for the current controller with a constant switching frequency. However, undesired frequency peaks usually appear in the closed-loop frequency response because of the delay in the digital implementation of the controller [23]. In addition, the complexity and computation burden also increase significantly when tracking high-order harmonics because each resonant controller can only regulate one harmonic component. In [23], a VPI controller based on a fundamental reference frame is introduced. This new scheme can greatly reduce the number of resonant controllers and eliminate the peaks from delay. Unfortunately, this scheme can only work under a three-phase three-wire system with a balanced load, and the performance of the controller under L-C-L filter is has not yet been reported.

Repetitive controller based on internal-mode principals is introduced in [25]. The repetitive controller can regulate all harmonics with one controller because the harmonics of line current are periodic signals, and the delay caused by the digital implementation can be easily compensated. Applying repetitive controllers to LCs under a typical structure with two parts have been attempted many times [26], [27]. However, as discussed before, LC performance is still degraded by the harmonic extractor.

In this paper, a modified one-cycle control scheme with plug-in repetitive controller is proposed. By combining the two controllers, the proposed scheme is capable of greatly increasing the harmonic rejection ability of the LC. In addition, the repetitive controller can reduce the effect of harmonics from the phase voltage. The desired features of one-cycle controller is retained because the main structure of the system is still OCC based—no phase lock loop (PLL) and harmonic extractor are needed for the LC, and the switching device works at a constant frequency.

The remaining parts of this paper are organized as follows: The configuration and design of the proposed controller is discussed in Section II. A comparison between the performance of the proposed controller and that of the existing OCC controller are given in Section III. The description of the experimental setup and the result of experiments are given and summarized in Section IV. Finally, the main conclusions are highlighted in Section V.

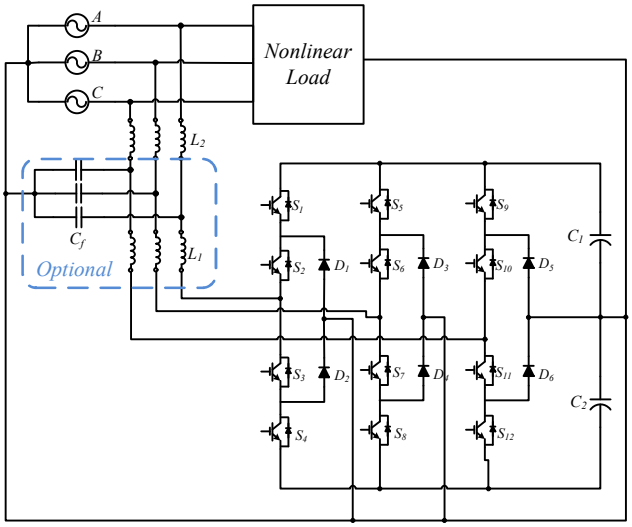


Fig. 1. Set up of the system.

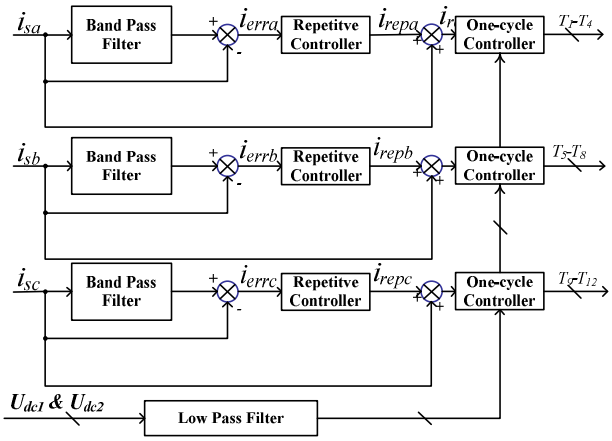


Fig. 2. Control system configuration.

II. Proposed Repetitive Controller

A. System Configuration

A typical circuit of neutral point clamp (NPC) based on a three-level three-phase four-wire load compensator with an input L-C-L or L filter is shown in Fig. 1. Repetitive control is an excellent way to eliminate all the harmonics from the system because all the harmonics in the AC system are periodic. The control system configuration is depicted in Fig. 2. A band-pass filter is used to extract the fundamental components of the line current i_{ref}, and the error signal for the repetitive controller is generated by subtracting the line current with its fundamental components. The repetitive control is separated from the OCC current loop because the repetitive controller is used as a "plug-in" structure and only deals with the error left by the one-cycle control so that fast dynamic performance can be obtained.

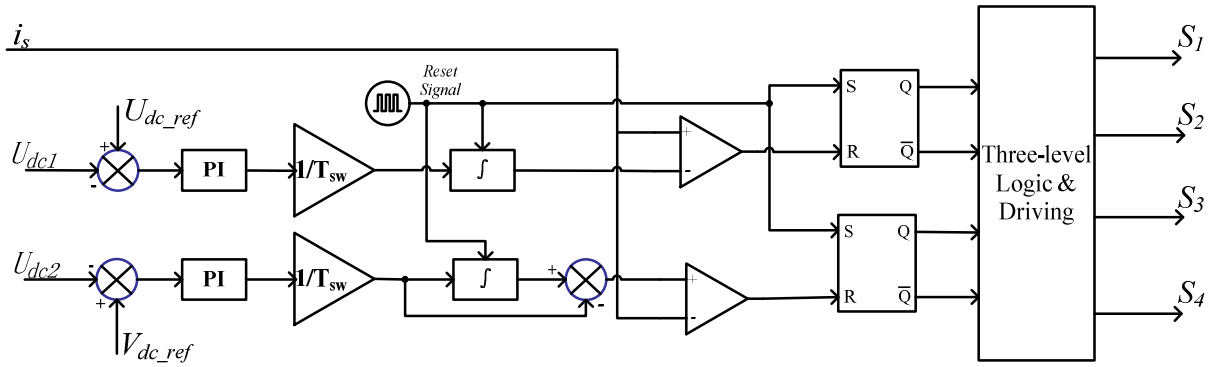


Fig. 3. Control block diagram of existing OCC scheme.

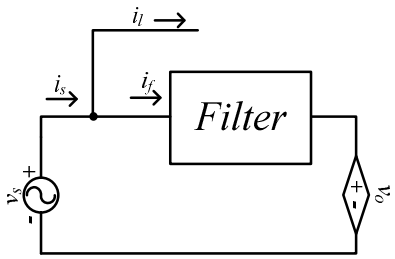
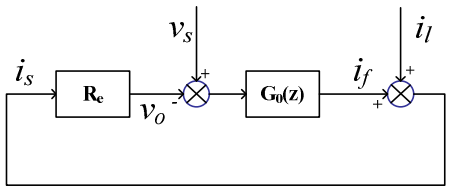
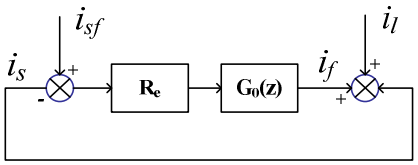


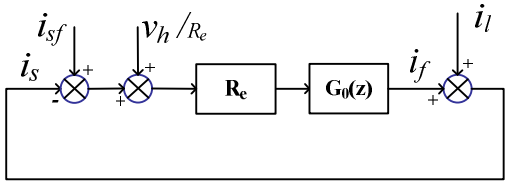
Fig. 4. Model of one phase in a three-phase four-wire load compensator.



(a) Control diagram of current loop of the existing one-cycle control.



(b) Replace v_s with i_f.



(c) Control diagram with distorted phase voltage v_s.

Fig. 5. Control diagram of the existing one-cycle control.

B. Model of Current Loop of Existing OCC Scheme

To design the repetitive controller of the proposed OCC based LC, the basic working principle of the existing OCC based LC is first explained and the model of its current loop is established.

A three-phase four-wire system can be regarded as three independent single-phase systems. Therefore, one such system is used as an example for analysis, as shown in Fig. 4.

One-cycle control is based on a double-loop structure, which is similar to other control schemes. The voltage loop regulates two DC voltages with two PI controllers, and the output of these voltages is defined as V_{m1} and V_{m2}. The two sawtooth waveforms with peaks of V_{m1} and V_{m2} are generated using an integrator with a reset and an adder (Fig. 3). Similar to the two-level case present in [28], the key control equation of the existing one-cycle controller is given in

$$V_{m1}d_1 - V_{m2}d_2 = i_s \tag{1}$$

where d_1 and d_2 represent the duty ratios of high output and low output of an inverter leg, which represents the line current. A detailed implementation of one-cycle control scheme for a three-phase, four-wire three-level LC is given in Appendix A.

Output voltage v_o of the inverter is expressed using an average model as follows:

$$v_o = U_{dc1}d_1 - U_{dc2}d_2 \tag{2}$$

where U_{dc1} and U_{dc2} represent the voltages of the upper and lower capacitors respectively.

It can be assume that the outputs of the two voltage loops are constants when analyzing the current loop because the bandwidth of the voltage loop is low compared with the current loop. Thus, as shown in Appendix A, the output of the voltage loop is given in

$$\begin{aligned} V_{m1} &= \frac{U_{dc1}}{R_e} \\ V_{m2} &= \frac{U_{dc2}}{R_e} \end{aligned} \tag{3}$$

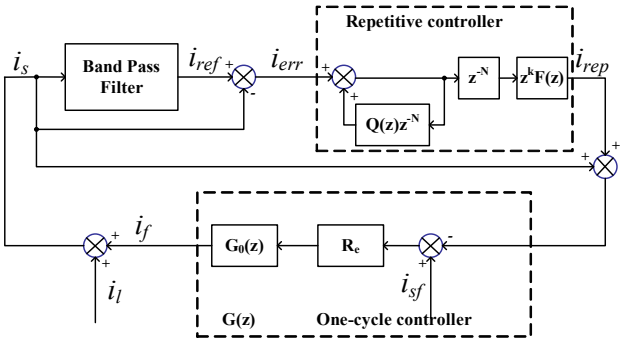
The emulated resistance R_e represents the effective per-phase load resistance seen by the AC source.

Combining Eqs. (1), (2), and (3) yields

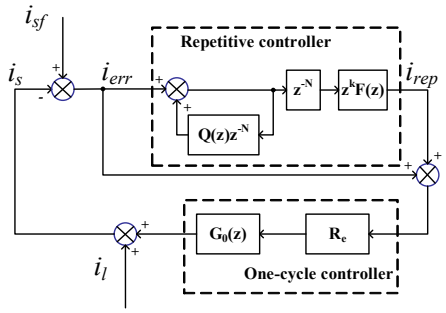
$$v_o = i_s R_e \tag{4}$$

Eq. (4) shows that the magnification of one-cycle control is R_e. Thus, the control diagram of the current loop is depicted in Fig. 5(a), where G_0 represents the transfer function of the filter.

If the grid voltage v_s has no distortion, then the active



(a) Detailed version of the proposed control.



(b) Simplified version of Fig. 6(a).

Fig. 6. Control diagram of the proposed control.

power balance of the whole system yields

$$v_s = i_{sf} R_e \tag{5}$$

where i_{sf} represents the real part of the fundamental component of i_s. Magnification of the one-cycle control is also R_e, and thus the control diagram can be transformed into Fig. 5(b) through replacing v_s with i_{sf}. Therefore, the current loop of the existing OCC is a proportional controller that lacks the ability to track high-order harmonics.

Fig. 5(b) shows that v_s works as a reference of the current system loop, and the nonlinear load current i_l is regarded as the disturbance. Thus, if the grid voltage v_s is distorted, then the performance will be greatly degraded because the control system cannot suppress the harmonic component of phase voltage v_h, which is injected from the reference as shown in Fig. 5(c). Consequently, the controller has no ability to suppress the error from the distorted phase voltage.

C. Design of Plug-in Repetitive Controller

The current loop of Fig. 2 can be redrawn in the z-domain with additional details, as shown in Fig. 6(a). The phase difference between the fundamental of the line current and phase voltage can be neglected because the one-cycle controller exhibits good performance at the fundamental frequency of the system. Thus, the output of band-pass filter i_{ref} and the real part of the fundamental component i_{sf} can be combined. The control system can be simplified through combining these two components, as shown in Fig. 6(b). The load current is treated as a disturbance. This structure is a classical plug-in repetitive control. The plant of the repetitive

TABLE I
PARAMETERS OF LOAD COMPENSATOR

Items	Values
Inverter side inductance L_1	400 μH
Filter Capacitor C_f	20 μF
Web side inductance L_2	170 μH
Damping resistance Rd	1.0 Ω
DC side capacitor Cdc	1350 μF
Grid frequency f_1	50 Hz
Switching frequency f_{sw}	10 kHz
Dead-time t_d	2.5 μs

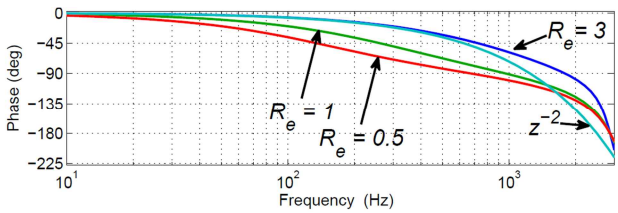


Fig. 7. Phase-frequency characteristic of $P(z)$ and z^{-2}.

controller $P(z)$ can be considered as a close-loop transfer function of one-cycle control as [29] shows:

$$P(z) = \frac{R_e G_0(z)}{1 + R_e G_0(z)}. \tag{6}$$

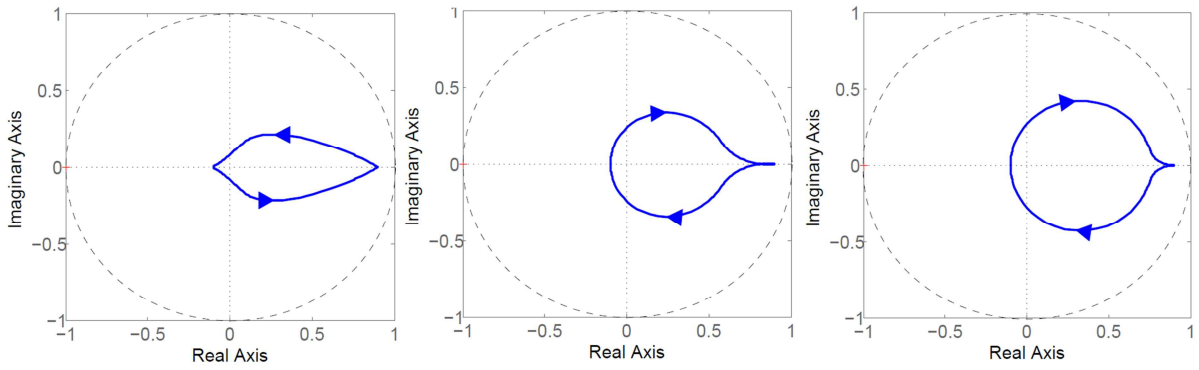
The parameters of LC is is listed in TABLE I and the design of the repetitive controller is based on them.

As the core of the repetitive controller, the modified internal model $1/(1-Q(z)z^{-N})$, which integrates the error on cycle bases, is designed first. The sampling frequency of the load compensator is 10 kHz, and the fundamental frequency of the system is 50 Hz. One repetitive control cycle contains N = 200 error sampling. The $Q(z)$ filter, which can increase the robustness of the repetitive control, is set as a low-pass filter or a constant near 1. In this case, $Q(z)$ is set as 0.9.

Repetitive control can achieve high gain under the fundamental and harmonic frequencies, but such high gain on high frequency may affect the system stability. Therefore, a filter $F(z)$ is added to eliminate the error signal from the bandwidth of the current loop and thus maintain the stability of the controller. Due to the existence of the delay stage z^{-N} which makes the control system causal, an advance stage z^k is added together with $F(z)$ to the diagram to compensate for the phase lag of $P(z)$ and $F(z)$.

Various R_e should be considered because the response of the one-cycle control is determined using R_e, which is based on the nonlinear load. Fig. 7 shows that advance stage z^2 can compensate the phase lag of $P(z)$ within the bandwidth of the current loop under various R_e. To evaluate the stability of the proposed control scheme, the transfer function from error signal i_{err} to reference signal i_{sf} can be expressed as

$$i_{err}(z) = \frac{[1 - P(z)][z^N - Q(z)]}{z^N - [Q(z) - F(z)z^k P(z)]} i_{sf}(z). \tag{7}$$



(a) R_e=3. (b) R_e=1. (c) R_e=0.5.

Fig. 8. Nyquist plot of $H(e^{j\omega t})$ under different Re.

The characteristic equation of the system is

$$z^N - [Q(z) - F(z)z^k P(z)] = 0. \quad (8)$$

To achieve system stability, all the roots of the above must be inside the unity circle that is centered at the origin of the z-plane. A sufficient condition for system stability is presented in [30]:

$$\left| Q(e^{j\omega t}) - F(e^{j\omega t}) e^{j\omega kt} P(e^{j\omega t}) \right| < 1 \quad \omega \in [0, \pi / T_s]. \quad (9)$$

Define $H(e^{j\omega t}) = Q(e^{j\omega t}) - F(e^{j\omega t}) e^{j\omega kt} P(e^{j\omega t})$. Eq. (9) means that the end of vector $H(e^{j\omega t})$ should never exceed the unity circle. The Nyquist plot of $H(e^{j\omega t})$ under various R_e are given in Fig. 8. The entire locus remains well within the unity circle, as seen in Fig. 8.

D. DC-Link Voltage Control Loop

The goal of the outer DC-link voltage loop is to keep the DC-link voltage of the LC constant through a simple PI regulator, whose output is the amplitude of the sawtooth waveforms V_{m1},V_{m2} as follows:

$$\begin{cases} v_{m1} = (K_{pdc} + \dfrac{K_{idc}}{s})(U_{dc}^* - U_{dc1}) \\ v_{m2} = (K_{pdc} + \dfrac{K_{idc}}{s})(U_{dc}^* - U_{dc2}) \end{cases} \quad (10)$$

where K_{pdc} and K_{idc} are the proportional and integrator gains of the PI controller, U_{dc}^* is the reference of the DC-link voltages, and U_{dc1} and U_{dc2} are the measured DC-link voltages. The model of the voltage loop given in Appendix B can be expressed as

$$\frac{\tilde{u}_{dc}(s)}{\tilde{v}_m(s)} = \frac{A}{1 + \dfrac{s}{\omega_0}}. \quad (11)$$

A and ω_0 can be expressed as

$$A = U_{dc} / V_m$$
$$\omega_0 = \frac{3V_s^2 V_m}{2C_{dc}U_{dc}^3} \quad (12)$$

where V_s is the root mean square (RMS) value of the phase voltage, and U_{dc} and V_m are the quiescent operation points of the voltage loop.

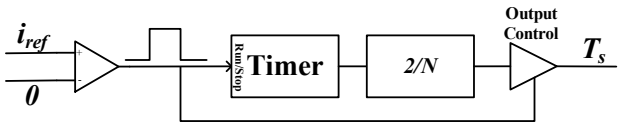


Fig. 9.Frequency adjustment block.

Based on the instructions in [31], the proportional gain of the controller K_{pdc} is derived as

$$K_{pdc} = \frac{2\pi f_c}{A\omega_0} \quad (13)$$

to transform the bandwidth voltage loop into f_c. The corner frequency of the PI controller is set as f_c/10 to achieve sufficient phase margin for the controller. Thus, the integrator gain of the controller is derived as

$$K_{idc} = \pi K_{pdc} f_c / 5. \quad (14)$$

E. Frequency Adjustment

Harmonic rejection ability of the repetitive controller can be degraded because the grid frequency varies in a narrow range. Thus, a frequency adjustment block should be added to adjust the sampling time and make the error samplings per period N a constant when the grid frequency changes.

The filtered current i_{ref} is compared with 0 to reshape the waveform into a square wave. A timer detects the high-level length of the square, which is equal to half of the grid period. The output of the timer is then divided with N/2, which is the right number of samplings per half period. After the division, the result is set as the new sampling time. Frequency adjustment block is shown in Fig. 9.

III. PERFORMANCE OF PROPOSED CONTROL

A. Harmonic Rejection Ability

The transfer function of the repetitive controller in Fig. 6(b) is

$$G_{rp}(z) = \frac{i_{rep}(z)}{i_{err}(z)} = \frac{F(z)z^k}{z^N - Q(z)}. \quad (15)$$

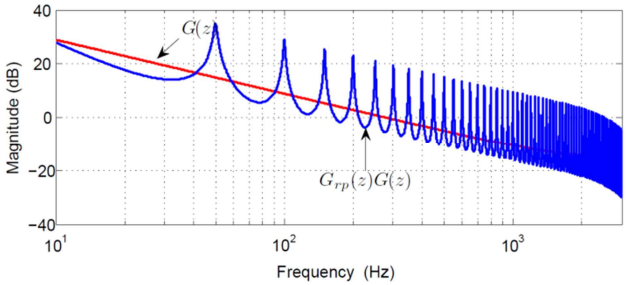


Fig. 10. Open loop gain of $|G_{rp}(z)G(z)|$ (blue) and $|G(z)|$ (red).

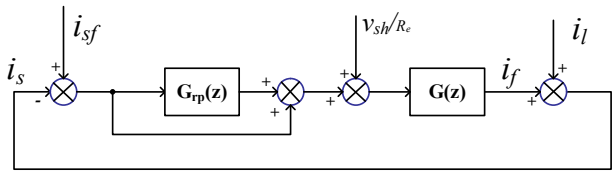


Fig. 11. Control diagram of repetitive control under distorted line voltage.

The transfer function of existing OCC in Fig. 5(b) is

$$G(z) = R_e G_0(z). \tag{16}$$

The open loop gain of $|G(z)|$ and $|G_{rp}(z)G(z)|$ are compared in Fig. 10, which indicates that the proposed controller provides higher gains at harmonic frequencies than the existing one-cycle controller. Therefore, the proposed controller has better harmonic suppressing ability than the existing one-cycle controller.

B. Sensitivity to Phase Voltage Distortion

Section II shows that the existing one-cycle controller lacks the ability to suppress distortion from the phase voltage. Investigating the effect of voltage harmonics on the proposed control is necessary. The input of the repetitive controller is from the band-pass filter, and thus contains no harmonics from the grid. To understand the suppression ability of the repetitive controller, the phase voltages are separated into two parts: fundamental component v_{sf} and harmonic component v_{sh}. The former, which contains no harmonics, is combined with the output of the band-pass filter. The diagram of the control blocks is shown in Fig. 11.

The transfer function $M(z)$ from harmonic voltage v_{sh} to error signal i_{err} can be expressed as

$$M(z) = \frac{i_{err}(z)}{v_{sh}(z)} = \frac{G(z)}{\{[1+[1+G_{rp}(z)]G(z)]\}R_e}. \tag{17}$$

The transfer function of $M(z)$ in the existing one-cycle control in Fig. 5c can be expressed as

$$M(z) = \frac{i_{err}(z)}{v_{sh}(z)} = \frac{G(z)}{[1+G(z)]R_e}. \tag{18}$$

The amplitude-frequency characteristics of M(z) is drawn in Fig. 12 (R_e=1). $M(z)$ has a smaller amplitude with the repetitive controller under harmonic frequencies. This characteristic indicates that most of the distortion from the harmonic component in phase voltage can be suppressed using repetitive control.

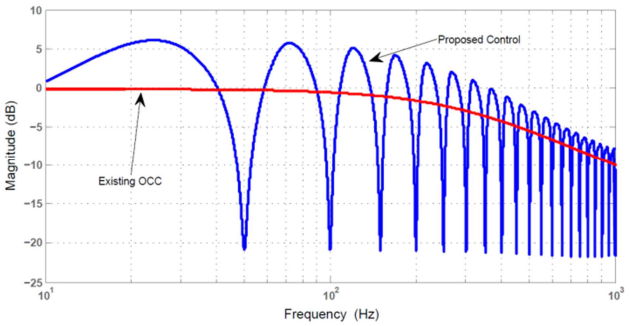


Fig. 12. Magnitude–frequency between i_{err} and v_{sh}.

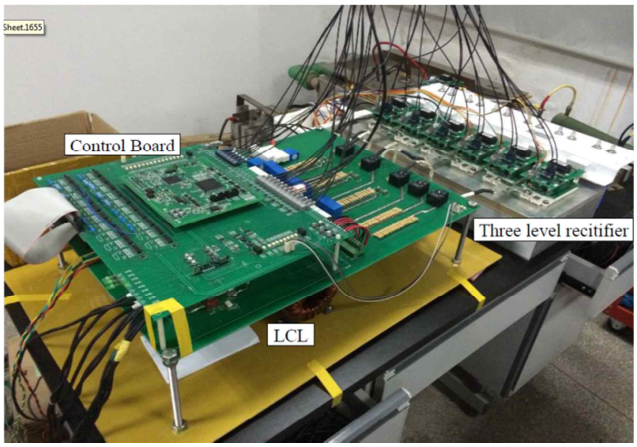


Fig. 13. Laboratory prototype.

IV. EXPERIMENTAL RESULTS

A. Experimental Setup

A scaled-down laboratory prototype of LC was built to test the performance of the proposed control. This prototype was tested on a three-phase system that had a phase voltage of 80 V. The reference voltage of both DC links is set as 160 V. To test the performance of the proposed control under a distorted voltage and its ability to suppress the effect of grid frequency variations, a Chroma programmable AC source 61512 is used as power source for the whole system. More detailed parameters used for this prototype can be found in TABLE I.

The nonlinear load of the system is a three-phase diode rectifier with two resistors on the DC-side. The neutral point of the rectifier is connected to the system, as shown in Fig. 14.

The controller is programmed with an existing one-cycle control Fig. 3 and a proposed control as Fig. 2 with the same switching frequency. The performance of both control

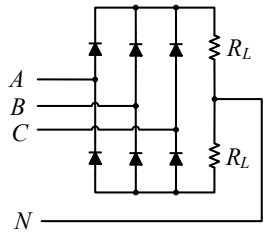
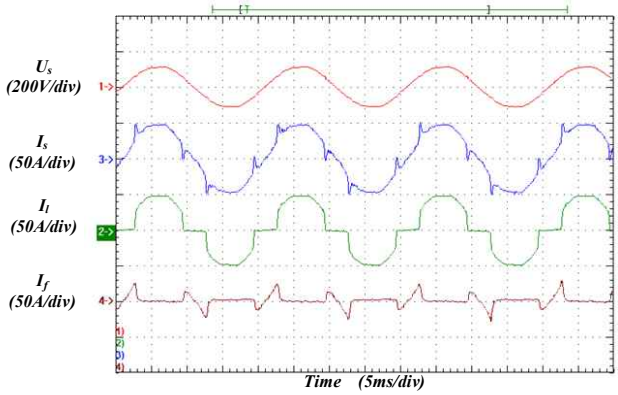
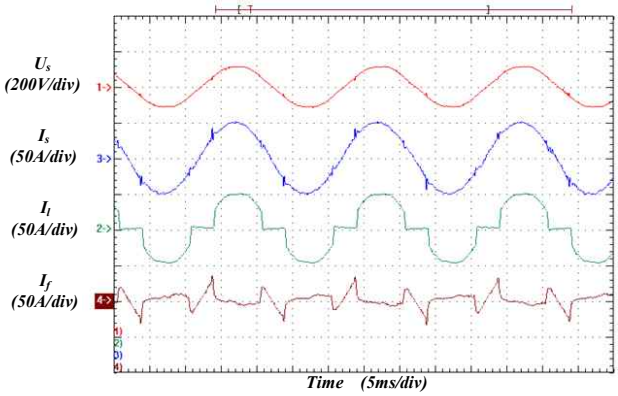


Fig. 14. Nonlinear Load.



(a) Existing one-cycle control.



(b) Proposed one-cycle control.

Fig. 15. Comparison of existing one-cycle control and proposed control.

schemes are compared under two scenarios: ideal phase voltage and distorted phase voltage.

B. Time and Spectrum Results under Ideal Phase Voltage

A set of experiments was conducted under ideal phase voltage to compare the performance of the two control schemes. Under this condition, the results are shown in Fig. 15 with voltage and currents of phase A. The existing one-cycle control cannot handle the step change of the line current because of the limited bandwidth in the current loop. Therefore, spikes appear in the waveform of line current, as shown in Fig. 15(a). The proposed control scheme has a high gain under harmonics through employing a plug-in repetitive controller. Thus, the current spikes are eliminated using the proposed control scheme, as shown in Fig. 15(b).

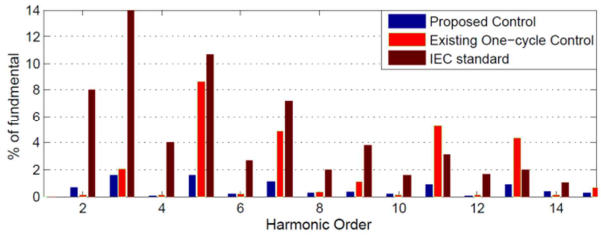


Fig. 16. Measured current spectra at ideal phase voltage.

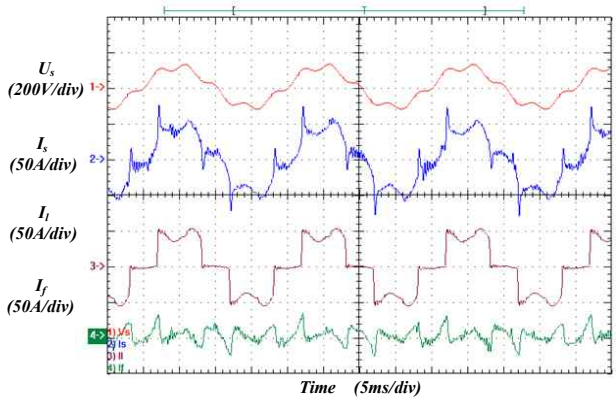
Fig. 16 compares the current spectra obtained from the two control schemes with the International Electrotechnical Commission (IEC) standard. The 11th- and 13th-order of harmonics in the existing OCC scheme exceeds the limitation of the IEC standard, whereas the current spectra of the proposed control meet the requirement of the IEC standard, as shown in Fig. 16. The line current total harmonic distortion (THD) is significantly reduced from 14.8% to 3.6% using the proposed control scheme. The proposed scheme presents better harmonic-elimination capability over the existing control and can reduce the amplitudes of low-order harmonics, which the existing control cannot do.

C. Time and Spectrum Result under Distorted Phase Voltage

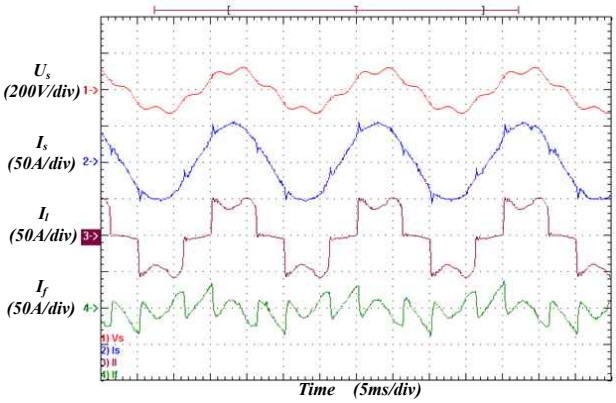
In practical circumstances, especially in low-voltage applications, phase voltage is normally distorted. Thus, a set of experiments was performed to compare the performance of the two controls under distorted phase voltage.

The experiments are from a Chroma 61612 programmable three-phase AC source. A 5th order of harmonics whose amplitude is 20% of the fundamental is then injected into the base voltage.

Fig. 17 demonstrates the results of the experiments. The existing one-cycle control almost loses the ability of harmonic suppression. In addition to the spikes, a large amount of 5th–order harmonics also appears in the current waveform. The proposed control can cancel out the effect of phase voltage harmonics using a repetitive controller that leads to good performance. Little spikes and 5th-order harmonics appear in the current waveform. Fig. 18 compares the spectra of the line current of the two controls with the IEC standard. For the existing control scheme, the amplitude of the 5th-order harmonics of the existing control is 29% and greatly exceeds the IEC standard, which is mostly from the injected voltage harmonics that the control scheme does not suppress. Under the proposed control scheme, the amplitude of the 5th-order harmonics is reduced to 3.5%, which meets the IEC standard. The THD of the line current is reduced from 36% to 7.2% through replacing the existing one-cycle control with the proposed control scheme. The proposed control shows better rejection ability of phase distortion than the existing OCC and can work effectively even with a highly distorted phase voltage.



(a) Existing one-cycle control.



(b) Proposed one-cycle control.

Fig. 17. Comparison of existing one-cycle control and proposed control under distorted phase voltage.

D. Frequency Variation

A set of experiments was conducted with different grid frequencies to test the harmonic rejection ability of the proposed control under various grid frequencies. The results of the experiments can be found in Fig. 19.

The results show that the proposed control scheme retains harmonic rejection ability when grid frequency varies. The THD of the line current is less than 3.5%, which suggests that the proposed control has the ability to adjust the variation of the grid frequency.

E. Dynamic Performance

The dynamic performance of the proposed controller is also evaluated under step load changes. Fig. 20 shows the transient response of line current i_s. A step change of the nonlinear load from 50% to 100% is performed. In the first cycle after the transient of load current, the system behaves similarly to the existing one-cycle control, and the amplitude quickly changes because the repetitive controller needs one cycle for output change. Moreover, the repetitive control does not affect the fast dynamic of the on-cycle control. Finally, the repetitive controller begins to change its output, and the line current soon becomes sinusoidal.

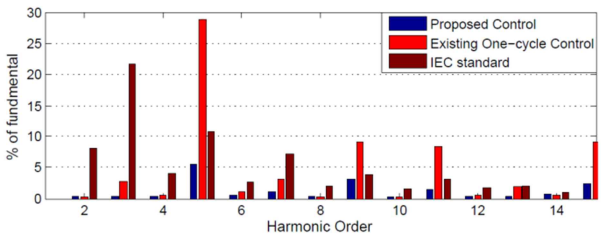
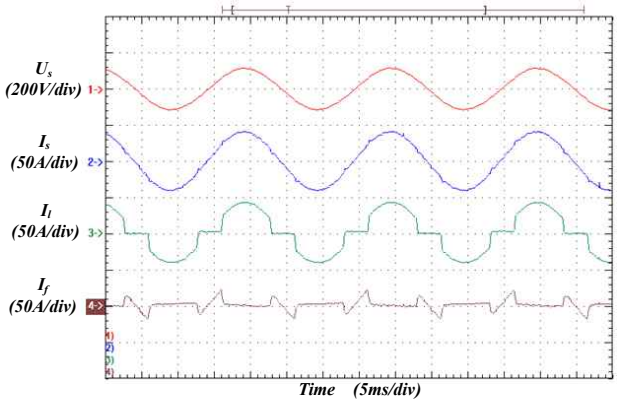
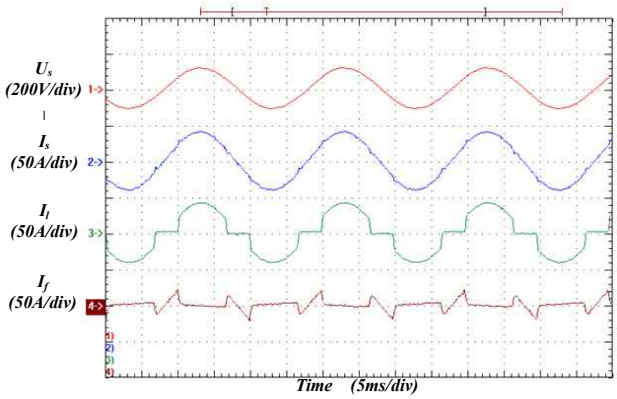


Fig. 18. Measured current spectra at distorted phase voltage.



(a) Grid frequency 49.5Hz



(b) Grid frequency 50.5Hz

Fig. 19. Test of the proposed controller under various grid frequencies.

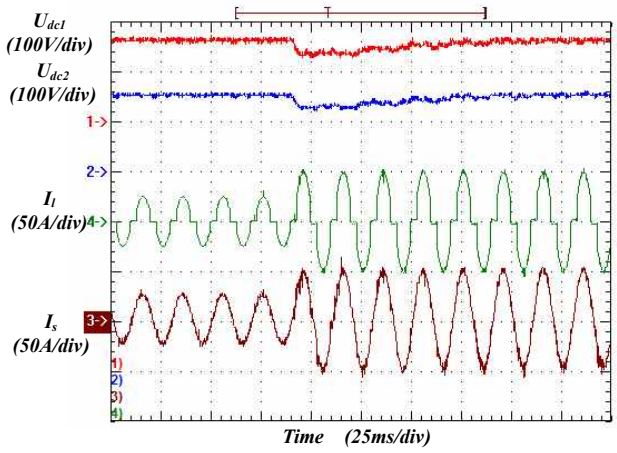


Fig. 20. Dynamic performance of the system.

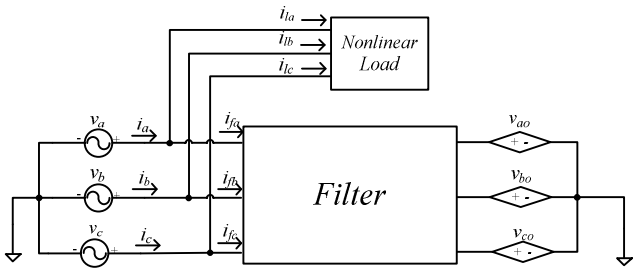


Fig. 21. Model of three-phase four-wire three-level load compensator.

V. Conclusion

A novel one-cycle control scheme for a three-phase, four-wire, three-level load compensator based on a plug-in repetitive controller was proposed. The voltage loop of this scheme is similar to the existing one-cycle control, in which a plug-in repetitive controller is added to the current loop. The detailed design of parameters of the repetitive controller is presented in this study through analyzing the loop gain and phase shift of the one-cycle control. A series of experiments was conducted to evaluate the performance of the proposed controller. A comparison between the performance of the proposed controller and that of the existing OCC confirmed that the former offers a superior harmonic suppression capability and lower sensitivity to the phase voltage distortion than the existing one-cycle controller, which suggests that the proposed scheme may be a good candidate under such condition.

Appendix A

One-Cycle Control Scheme of Three-Phase, Four-Wire, Three-Level Load Compensator

The model of the system is given in Fig. 21. The output voltage of the inverter can be derived through averaging the voltage over a single switching frequency:

$$\begin{cases} v_{ao} = d_{a1}U_{dc1} - d_{a2}U_{dc2} \\ v_{bo} = d_{b1}U_{dc1} - d_{b2}U_{dc2} \\ v_{co} = d_{c1}U_{dc1} - d_{c2}U_{dc2} \end{cases} \tag{19}$$

where v_a, v_b, and v_c represent the phase voltages; v_{ao}, v_{bo}, and v_{co} represent the outputs of inverter; d_{a1}, d_{b1}, and d_{c1} represent the high-output duty ratio of each leg; and d_{a2}, d_{b2}, and d_{c2} represent the low-output duty ratio of each leg.

The filter parameters are relatively small with regard to a 50 Hz system because the filter works at a high frequency. The voltage drop across the filter v_{af}, v_{bf}, and v_{cf} is neglected [32].

Therefore, the following equations hold:

$$\begin{cases} v_a \approx v_{ao} \\ v_b \approx v_{bo} \\ v_c \approx v_{co} \end{cases}. \tag{20}$$

The control goal of the load compensator is to force three-phase currents to follow the three-phase sinusoidal voltage. Thus, the impedance of looking into the whole system should be resistive. The control goal is to realize the following relationship:

$$\begin{cases} v_a = i_a R_e \\ v_b = i_b R_e \\ v_c = i_c R_e \end{cases} \tag{21}$$

Combining Eqs. (19), (20), and (21) yields

$$\begin{cases} i_a R_e \approx d_{a1}U_{dc1} - d_{a2}U_{dc2} \\ i_b R_e \approx d_{b1}U_{dc1} - d_{b2}U_{dc2} \\ i_c R_e \approx d_{c1}U_{dc1} - d_{c2}U_{dc2} \end{cases} \tag{22}$$

Reshaping Eq. (22) yields

$$\begin{cases} i_a \approx d_{a1}\dfrac{U_{dc1}}{R_e} - d_{a2}\dfrac{U_{dc2}}{R_e} \\ i_b \approx d_{b1}\dfrac{U_{dc1}}{R_e} - d_{b2}\dfrac{U_{dc2}}{R_e} \\ i_c \approx d_{c1}\dfrac{U_{dc1}}{R_e} - d_{c2}\dfrac{U_{dc2}}{R_e} \end{cases} \tag{23}$$

Comparing to the duty ratio d_{x1} and d_{x2}, it can be easily seen that the DC-link voltages U_{dc1} and U_{dc2} change much slower and can be regarded as constants. V_{m1} and V_{m2} are defined as the output of the voltage loop which controls the DC-link voltages and their value can achieved by the balance of active power of system.

$$\begin{cases} V_{m1} = \dfrac{U_{dc1}}{R_e} \\ V_{m2} = \dfrac{U_{dc2}}{R_e} \end{cases} \tag{24}$$

Theoretically, there are infinite sets of dx_1 and dx_2 fulfilling Eq. (23). To minimize switching loss, one of the duty ratios is set as zero, and the other duty ratio is controlled to satisfy Eq. (23):

$$d_{x1} = \begin{cases} \dfrac{i_{x0}}{V_{m1}} & (i_{sx} > 0) \\ 0 & (i_{x0} < 0) \end{cases} \quad (x = a,b,c) \tag{25}$$

$$d_{x1} = \begin{cases} 0 & (i_{sx} > 0) \\ -\dfrac{i_{x0}}{V_{m1}} & (i_{x0} < 0) \end{cases}$$

Two integrators with time constant of V_{m1}=T_{sw} and V_{m2}=T_{sw} and two comparers satisfy Eq. (25), where T_{sw} represents the switch period, as Fig. 4 shows.

Appendix B

Model of Voltage Loop of Proposed Load Compensator

To design the voltage loop of the LC, a model is derived to determine the transfer function between $v_m(s)$ and $u_{dc}(s)$. If

the DC-link capacitor is sufficiently large, then the ripples of the DC-link voltage are low and can be neglected. Thus, the difference between two DC-link voltages is neglected because they are mainly ripples. Under such assumption, Eq. (19) can be written as

$$v_{xo} = (d_{x1} - d_{x2})U_{dc}, \qquad (x = a,b,c) \tag{26}$$

where U_{dc} is the voltage of the DC link. The differences between the outputs of two voltage loops are also ignored considering the symmetrical characteristic of the two voltage loops. The duty ratios d_{x1} and d_{x2} can be acquired using Eq. (25). Thus,

$$v_{xo} = i_x \frac{U_{dc}}{V_m} \qquad (x = a,b,c) \tag{27}$$

where V_m is the output of the voltage loop. Considering Eq. (20), the line current of each phase can be expressed as

$$v_{xo} = i_x \frac{U_{dc}}{V_m} \qquad (x = a,b,c). \tag{28}$$

The three-phase four-wire system can be considered as three single-phase systems. Thus, a single-phase system with phase voltage v_s and phase current i_s is analyzed as an example. The phase voltage can be expressed as

$$v_s(t) = \sqrt{2}V_s \sin(\omega t). \tag{29}$$

The input power from the grid can then be expressed as

$$P_{in} = v_s i_s = \frac{V_m}{U_{dc}} V_s{}^2 (1 - \cos(2\omega t)). \tag{30}$$

Considering the low bandwidth of the voltage loop, the term that varies with twice that of the utility frequency will be filtered out by the controller. This term can thus be ignored. When averaging the model over the line frequency, the input power can be expressed as

$$\langle P_{in} \rangle_T = \frac{\langle V_m \rangle_T}{\langle U_{dc} \rangle_T} \langle V_s \rangle_T{}^2 \tag{31}$$

where T represents the line period. The total input power from the grid P_{all} can be written as

$$\langle P_{all} \rangle_T = 3\langle P_{in} \rangle_T = 3\frac{\langle V_m \rangle_T}{\langle U_{dc} \rangle_T} \langle V_s \rangle_T{}^2. \tag{32}$$

The nonlinear load consumes most of the input power and the rest can charge or discharge the DC-link capacitors. Thus, the averaging model is given as

$$\langle P_{all} \rangle_T = \langle P_L \rangle_T + \frac{d\langle E \rangle_T}{dt}. \tag{33}$$

where $\langle P_L \rangle_T$ is the power that the nonlinear load consumes, and $\langle E \rangle_T$ is the energy stored in the two DC-link capacitors. With the DC-link voltage U_{dc}, $\langle E \rangle_T$ can be expressed as

$$\langle E \rangle_T = C_{dc} \langle U_{dc} \rangle_T{}^2. \tag{34}$$

V_s and P_L are regarded as constants because the LC is connected to a steady grid, and the power of the nonlinear load does not change. Small-signal perturbation is applied around the steady state of the system to linearize the model.

$$\begin{aligned} \langle V_m \rangle_T &= V_m + \tilde{v}_m \qquad \langle U_{dc} \rangle_T = U_{dc} + \tilde{u}_{dc} \\ \langle E \rangle_T &= E + \tilde{E} \qquad \langle P_{all} \rangle_T = P_{all} + \tilde{p}_{all} \end{aligned} \tag{35}$$

The Taylor series expansion of Eq. (32) can be written as

$$\tilde{p}_{all} = \frac{\partial \langle P_{all} \rangle_T}{\partial \langle U_{dc} \rangle_T} \tilde{u}_{dc} + \frac{\partial \langle P_{all} \rangle_T}{\partial \langle V_m \rangle_T} \tilde{v}_m. \tag{36}$$

where

$$\frac{\partial \langle P_{all} \rangle_T}{\partial \langle U_{dc} \rangle_T} = -\frac{3V_s{}^2 V_m}{U_{dc}{}^2}. \tag{37}$$

$$\frac{\partial \langle P_{all} \rangle_T}{\partial \langle V_m \rangle_T} = \frac{3V_s{}^2}{U_{dc}}. \tag{38}$$

Combining Eqs. (36), (37), and (38) yields

$$\tilde{p}_{all} = \frac{3V_s{}^2}{U_{dc}} \tilde{v}_m - \frac{3V_s{}^2 V_m}{U_{dc}{}^2} \tilde{u}_{dc}. \tag{39}$$

Similarly, the Taylor series expansion of Eq. (34) can be written as

$$\tilde{E} = \frac{d\langle E \rangle_T}{d\langle U_{dc} \rangle_T} \tilde{u}_{dc} = 2C_{dc} U_{dc} \tilde{u}_{dc}. \tag{40}$$

The small-signal perturbation of Eq. (33) is

$$\tilde{p}_{all} = \frac{d\tilde{E}}{dt} \tag{41}$$

Combining Eqs. (39), (40), and (41) yields

$$2C_{dc} U_{dc} \frac{\tilde{u}_{dc}}{dt} + \frac{3V_s{}^2 V_m}{U_{dc}{}^2} \tilde{u}_{dc} = \frac{3V_s{}^2}{U_{dc}} \tilde{v}_m. \tag{42}$$

Thus, the small signal model between v_m and u_{dc} is

$$\frac{\tilde{u}_{dc}(s)}{\tilde{v}_m(s)} = \frac{3V_s{}^2 U_{dc}}{2C_{dc} U_{dc}{}^3 s + 3V_s{}^2 V_m}. \tag{43}$$

ACKNOWLEDGMENT

This work is supported by the National Natural Science Foundation of China (NSFC) (#51177147 and #51177149).

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