JPE 15-2-10

http://dx.doi.org/10.6113/JPE.2015.15.2.389
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Medium Voltage Resonant Converter with Balanced Input Capacitor Voltages and Output Diode Currents

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Abstract

This paper presents a 1.92 kW resonant converter for medium voltage applications that uses low voltage stress MOSFETs (500V) to achieve zero voltage switching (ZVS) turn-on. In the proposed converter, four MOSFETs are connected in series to limit the voltage stress of the power switches at half of the input voltage. In addition, three resonant circuits are adopted to share the load current and to reduce the current stress of the passive components. Furthermore, the transformer primary and secondary windings are connected in series to balance the output diode currents for medium power applications. Split capacitors are adopted in each resonant circuit to reduce the current stress of the resonant capacitors. Two balance capacitors are also used to automatically balance the input capacitor voltage in every switching cycle. Based on the circuit characteristics of the resonant converter, the MOSFETs are turned on under ZVS. If the switching frequency is less than the series resonant frequency, the rectifier diodes can be turned off under zero current switching (ZCS). Experimental results from a prototype with a 750-800 V input and a 48V/40A output are provided to verify the theoretical analysis and the effectiveness of the proposed converter.

Key words: Interleaved PWM, PWM converters, Switching mode power supplies

I. INTRODUCTION

Full-bridge converters with a simple structure, constant frequency pulse-width modulation and soft switching turn-on [1]-[4] have been adopted in medium power applications. However, power switches should suffer the input voltage due to the full-bridge structure. High input DC/DC converters have been developed for ship electric power distribution systems [5], three-phase AC/DC converters and the traction systems for light trains [6]-[7]. Three-level DC/DC converters [8]-[10] with low voltage and current stresses were presented to reduce the voltage stress on active switches. However, the power switches are operated at hard switching. High switching losses on the power switches reduce the circuit efficiency. In order to achieve soft switching and reduce switching losses, three-level zero voltage switching (ZVS) converters for high input voltage applications were proposed in [11]-[14]. In [13], four power switches with $V_{in}/2$ voltage stress and two power switches with V_{in} voltage stress are used in the three-level ZVS hybrid full bridge converter. The drawback of this circuit is that two power switches with high voltage stress are used in this converter. Resonant converters [15]-[18] have been proposed for the advantages of high conversion efficiency and high power density. Power switches are turned on under ZVS from low load to full load. If the switching frequency is less than the series resonant frequency, the rectifier diodes at output side are turned off under zero current switching (ZCS). The series-parallel connection techniques have been discussed in [19]-[21]. In [19], two transformers are adopted in three-level converter with current double rectifier for medium voltage application. However, the high current rating of rectifier diodes and large size of filter inductors are needed in this circuit topology for high load current application. The circuit efficiency will be drop at light load due to the high circulating current in conventional three-level PWM converter. The input split capacitor voltages cannot be automatically balanced. An active clamp forward converter with parallel connection in primary side was presented in [20] to achieve soft switching. However, this circuit topology cannot be used for medium voltage applications due to its high voltage stress on the power switches. A three-level resonant converter with duty cycle control has been presented in [21] to have ZVS turn-on

Manuscript received Aug. 27, 2014; accepted Nov. 7, 2014
Recommended for publication by Associate Editor Joung-Hu Park.
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for all of the power switches and ZCS turn-off for all of the rectifier diodes. The output currents of the two secondary sides are automatically balanced due to the series connection of the transformers. However, the input split capacitor voltages cannot be balanced automatically and the duty cycle is decreased under a light load case. Thus, the circuit efficiency under a light load is decreased.

A ZVS DC/DC converter for high input voltage and load current applications is studied in this paper. Two half-bridge legs with split capacitors are connected in series at the high voltage side to clamp the voltage stress of the power switches at half of the input voltage. Two balance capacitors are used between the AC sides of the two half-bridge legs to automatically balance the input split capacitor voltages. Three resonant circuits are used at the high voltage side in order to reduce the current stress of the resonant components. The secondary windings of the transformers are connected in series to automatically balance the output diode currents. Since the input impedance of the resonant tank is an inductive load at the switching frequency, the power switches are turned on under ZVS. As a result, the switching losses on the power switches are reduced. Finally, experiments from a 750-800 V input and 48V/40A output prototype were provided to verify the performance of the proposed converter.

II. Proposed Converter and Operation Principle

For three-phase power factor corrector converters with a 380V or 480V utility voltage or a DC traction system, the input voltage of the DC/DC converter is equal to or higher than 750V. Fig. 1 gives the circuit topology of the proposed converter for medium voltage applications. The circuit components at the high voltage side include the input voltage V_{in}, power MOSFETs S_1-S_4 with their body diodes and parallel capacitors C_{oss1}-C_{oss4}, resonant capacitors C_{r1}-C_{r6}, resonant inductors L_{r1}-L_{r3}, and transformers T_1-T_4. Two center-tapped rectifiers are used at the low voltage side to share the load current and to reduce the current stress of the passive components. The secondary windings of T_1 and T_3 are connected in series so that the primary currents i_{Lr1} and i_{Lr3} are balanced. Similarly, the primary currents i_{Lr2} and i_{Lr3} are balanced since the secondary windings of T_2 and T_4 are connected in series. Thus, the primary and secondary winding currents of T_1-T_4 are balanced. (S_1 and S_3) and (S_2 and S_4) have the same PWM waveforms with a 0.5 duty cycle. However, the driving signals of S_2 and S_4 are complementary with the driving signals of S_1 and S_3 with a short dead time. The components S_1-S_4 and C_{r1}-C_{r6} establish a switched capacitor circuit [22]. Therefore, the input capacitor voltages are balanced, $v_{Cr1}+v_{Cr2}=v_{Cr3}+v_{Cr4}=v_{Cr5}+v_{Cr6}=V_{in}/2$. The proposed converter includes three resonant circuits at the high voltage side. A variable frequency scheme is adopted to regulate the output voltage.

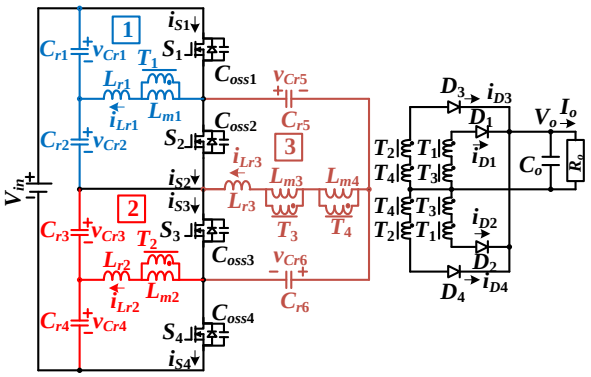


Fig. 1. Circuit configuration of the proposed converter.

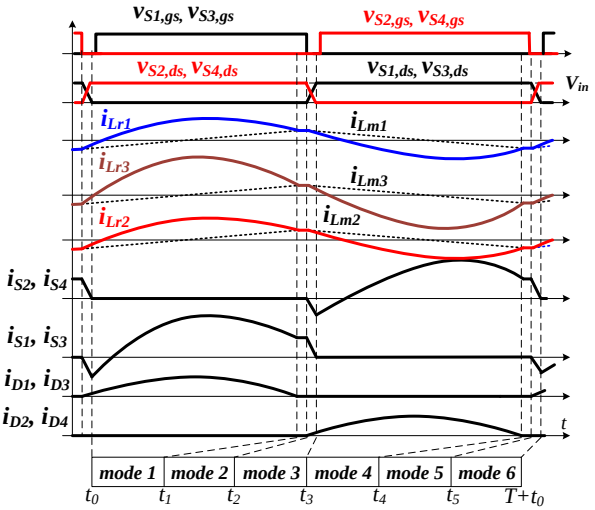


Fig. 2. Key waveforms of the proposed converter.

The following assumptions are presumed to simplify the system analysis of the three resonant circuits. The transformers T_1-T_4 have the magnetizing inductances $L_{m1}=L_{m2}=2L_{m3}=2L_{m4}=L_m$ and the turns ratios $n_1=n_2=2n_3=2n_4=n$. The resonant capacitances are $C_{r1}=C_{r2}=C_{r3}=C_{r4}=C_{r5}=C_{r6}=C_r$. The resonant inductances are identical $L_{r1}=L_{r2}=L_{r3}=L_r$. The power MOSFETs S_1-S_4 have the same output capacitances $C_{oss1}=C_{oss2}=C_{oss3}=C_{oss4}=C_{oss}$. The capacitor voltages $v_{Cr1}+v_{Cr2}=v_{Cr3}+v_{Cr4}=v_{Cr5}+v_{Cr6}=V_{in}/2$. If the switching frequency f_{sw} is less than the series resonant frequency f_r, there are six operating modes in a switching cycle. The main PWM waveforms of the proposed converter under $f_{sw}<f_r$ are shown in Fig. 2 and Fig. 3. They give the corresponding equivalent circuit for each operation mode. If the switching frequency $f_{sw}>f_r$, then the resonant circuit has only four operation modes (modes 1, 3, 4 and 6) in a switching cycle. In the following statements, the six modes of operation are discussed in each switching cycle. Before time t_0, S_1-S_4, D_2 and D_4 are in the off-state. C_{oss1} and C_{oss3} are discharged, and C_{oss2} and C_{oss4} are charged.

***Mode 1* [t_0 - t_1]:** Mode 1 starts at time t_0 when C_{oss1} and C_{oss3} are discharged to zero voltage. Since $i_{Lr1}(t_0)<0$, $i_{Lr2}(t_0)<0$ and

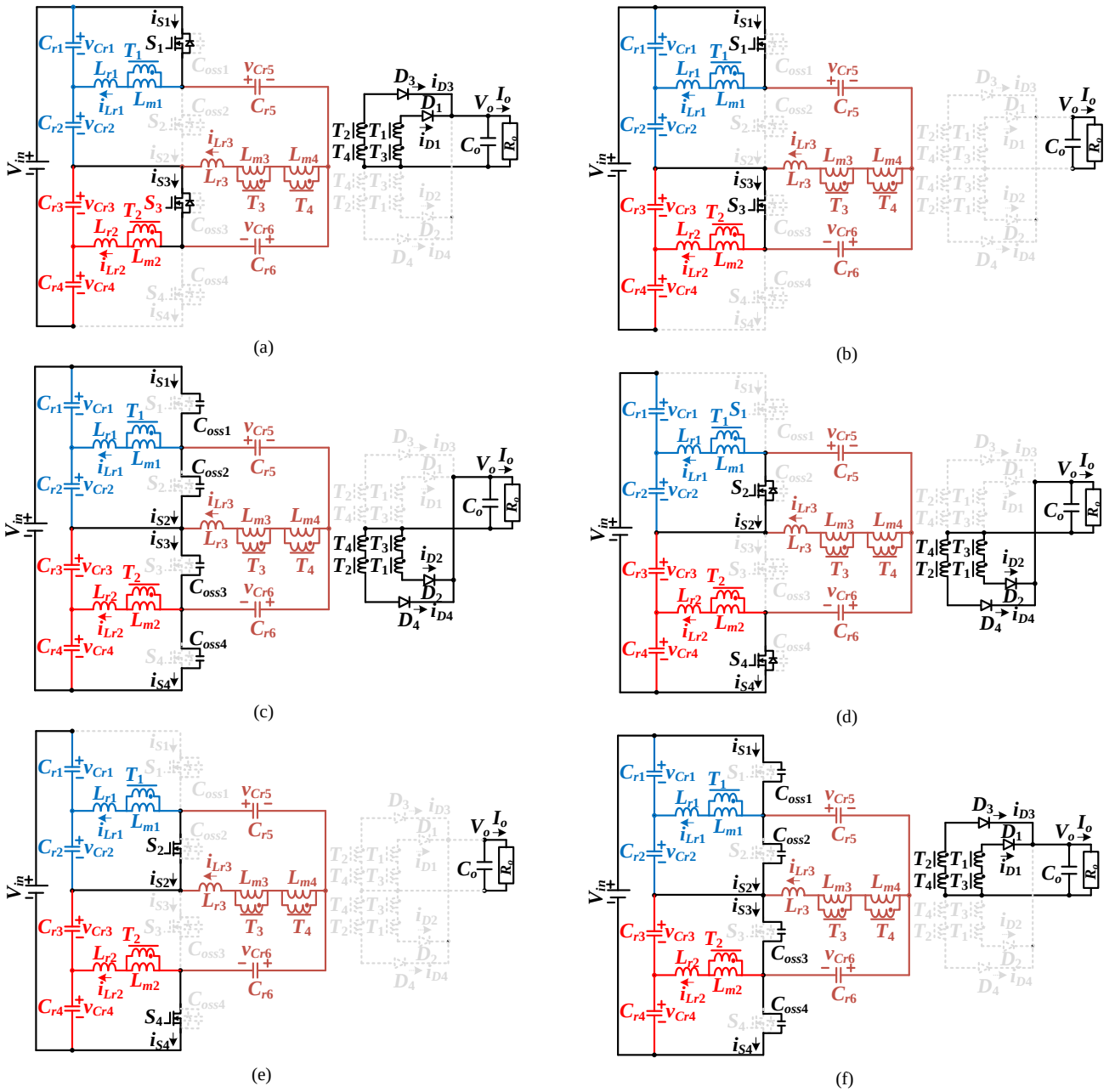


Fig. 3. Operation modes of the proposed converter in a switching cycle. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

$i_{Lr3}(t_0)<0$, the anti-parallel diodes of S_1 and S_3 are conducting. Thus, S_1 and S_3 are turned on at this moment under ZVS. The voltage stresses of S_2 and S_4 are equal to $v_{Cr1}+v_{Cr2}$ and $v_{Cr3}+v_{Cr4}$, respectively. In this mode, the capacitor voltage $v_{Cr5}+v_{Cr6}=v_{Cr1}+v_{Cr2}$. On the other hand, the capacitor voltage $v_{Cr5}+v_{Cr6}=v_{Cr3}+v_{Cr4}$ in mode 3. Thus, it can be obtained that $v_{Cr1}+v_{Cr2}=v_{Cr3}+v_{Cr4}=v_{Cr5}+v_{Cr6}=V_{in}/2$ in steady state. Since $i_{Lr1}>i_{Lm1}$, $i_{Lr2}>i_{Lm2}$ and $i_{Lr3}>i_{Lm3}$, diodes D_1 and D_3 are conducting. In this mode, v_{Lm1} - v_{Lm4} are positive and i_{Lm1} - i_{Lm5} increase. In addition, L_{r1}, C_{r1} and C_{r2} are resonant in circuit 1; L_{r2}, C_{r3} and C_{r4} are resonant in circuit 2; L_{r3}, C_{r5} and C_{r6} are resonant in circuit 3; and power is transferred from the input voltage V_{in} to the output load R_o. The resonant frequency is $f_r = 1/2\pi\sqrt{2L_rC_r}$.

***Mode 2* [t_1 - t_2]:** At time t_1, $i_{Lr1}(t_1)=i_{Lm1}(t_1)$, $i_{Lr2}(t_1)=i_{Lm2}(t_1)$ and $i_{Lr3}(t_1)=i_{Lm3}(t_1)=i_{Lm4}(t_1)$. Thus, diodes D_1-D_4 are all in the off-state. In this mode, L_{r1}, L_{m1}, C_{r1} and C_{r2} are resonant in circuit 1; L_{r2}, L_{m2}, C_{r3} and C_{r4} are resonant in circuit 2; and L_{r3}, L_{m3}, L_{m4}, C_{r5} and C_{r6} are resonant in circuit 3. The resonant frequency is $f_p = 1/2\pi\sqrt{2(L_r+L_m)C_r}$.

***Mode 3* [t_2 - t_3]:** At time t_2, S_1 and S_3 are turned off. Diodes D_2 and D_4 are conducting, v_{Lm1} - v_{Lm4} are negative, and i_{Lm1} - i_{Lm4} decrease. Since $i_{Lr1}(t_2)>0$, $i_{Lr2}(t_2)>0$ and $i_{Lr3}(t_2)>0$, C_{oss1}

and C_{oss3} are charged and C_{oss2} and C_{oss4} are discharged. C_{oss2} and C_{oss4} can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} at t_2 is greater than the energy stored in C_{oss1} - C_{oss4}.

***Mode 4* [t_3 - t_4]:** At time t_3, v_{Coss2}=v_{Coss4}=0. Since $i_{Lr1}(t_3)$>0, $i_{Lr2}(t_3)$>0 and $i_{Lr3}(t_3)$>0, the anti-parallel diodes of S_2 and S_4 are conducting. S_2 and S_4 can be turned on at this moment under ZVS. In mode 4, D_2 and D_4 are conducting, i_{Lm1} - i_{Lm4} decrease. In addition, v_{Coss1}=v_{Cr1}+v_{Cr2}, v_{Coss3}=v_{Cr3}+v_{Cr4}, and v_{Cr5}+v_{Cr6}=v_{Cr3}+v_{Cr4}. L_{r1}, C_{r1} and C_{r2} are resonant in circuit 1; L_{r2}, C_{r3} and C_{r4} are resonant in circuit 2; L_{r3}, C_{r5} and C_{r6} are resonant in circuit 3; and power is transferred from the input voltage V_{in} to the output load R_o. The resonant frequency is $f_r = 1/2\pi\sqrt{2L_rC_r}$.

***Mode 5* [t_4 - t_5]:** At time t_4, $i_{Lr1}(t_4)$=$i_{Lm1}(t_4)$, $i_{Lr2}(t_4)$=$i_{Lm2}(t_4)$ and $i_{Lr3}(t_4)$=$i_{Lm3}(t_4)$=$i_{Lm4}(t_4)$. Diodes D_1-D_4 are all in the off-state. L_{r1}, L_{m1}, C_{r1} and C_{r2} are resonant in circuit 1; L_{r2}, L_{m2}, C_{r3} and C_{r4} are resonant in circuit 2; L_{r3}, L_{m3}, L_{m4}, C_{r5} and C_{r6} are resonant in circuit 3; and the resonant frequency is $f_p = 1/2\pi\sqrt{2(L_r+L_m)C_r}$.

***Mode 6* [t_5 - T+t_0]:** At time t_5, S_2 and S_4 are turned off. Diodes D_1 and D_3 are conducting. The magnetizing voltages v_{Lm1} - v_{Lm4} are positive and the magnetizing currents i_{Lm1} - i_{Lm4} increase. Since $i_{Lr1}(t_5)$<0, $i_{Lr2}(t_5)$<0 and $i_{Lr3}(t_5)$<0, C_{oss1} and C_{oss3} are discharged and C_{oss2} and C_{oss4} are charged. C_{oss1} and C_{oss3} can be discharged to zero voltage if the energy stored in L_{r1} - L_{r3} at t_5 is greater than the energy stored in C_{oss1} - C_{oss4}. Then, the operating modes of the proposed converter in a switching period are completed.

III. Converter Performance Analysis and Design Example

Three resonant circuits are included in the proposed converter to share the load power. The power transferred through the three resonant circuits is a function of the switching frequency. The input terminal of the resonant circuit is a square wave voltage. If the bandwidth of the resonant circuit is less than the switching frequency, the harmonics of the input square wave voltage can be neglected at the output terminal. The secondary side currents i_{D1}+i_{D2} and i_{D3}+i_{D4} are quasi-sinusoidal currents. If the primary inductor currents are greater than the magnetizing currents, then diodes D_1 and D_3 are conducting and v_{Lm1}=v_{Lm2}=nV_o/2 and v_{Lm3}=v_{Lm4}=nV_o/4. On the other hand, v_{Lm1}=v_{Lm2}=-nV_o/2, v_{Lm3}=v_{Lm4}=-nV_o/4 and rectifier diodes D_2 and D_4 are conducting when the primary inductor currents are less than the magnetizing currents. Since the charge/discharge time of output capacitors C_{oss1}-C_{oss4} in modes 3 and 6 and the time intervals in modes 2 and 5 are much less than the time intervals in modes 1 and 4, the magnetizing inductor voltages v_{Lm1}-v_{Lm4} approximate quasi-square waveforms.

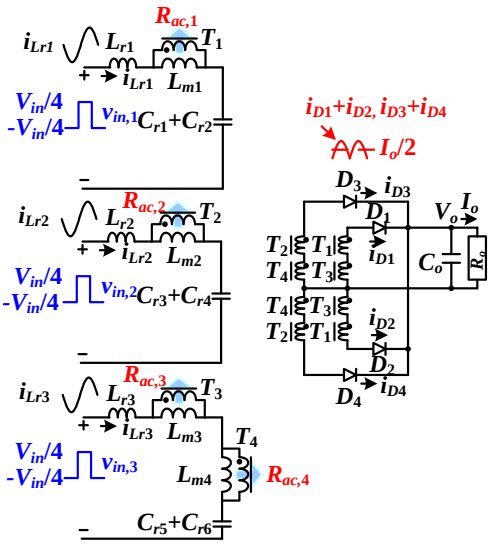


Fig. 4. Equivalent circuit of the proposed converter for the derivation of steady state model.

$$v_{Lm1} = v_{Lm2} = \sum_{m=1,3,5...} \frac{2nV_o}{m\pi}\sin(2\pi m f_s t - \theta_m) \quad (1)$$

$$v_{Lm3} = v_{Lm4} = \sum_{m=1,3,5...} \frac{nV_o}{m\pi}\sin(2\pi m f_s t - \theta_m) \quad (2)$$

where θ_m is the phase angle of the m-th harmonic frequency. The peak secondary winding currents are given as:

$$\hat{i}_{T1,\sec} = \hat{i}_{T2,\sec} = \hat{i}_{T3,\sec} = \hat{i}_{T4,\sec} = \pi I_o/4 \quad (3)$$

Thus, the load resistance R_o reflected to the transformer primary sides is shown as:

$$R_{ac,1} = R_{ac,2} = \frac{\hat{v}_{Lm1,f}}{\hat{i}_{T1,\sec}/n} = \frac{8n^2}{\pi^2}R_o \quad (4)$$

$$R_{ac,3} = R_{ac,4} = \frac{\hat{v}_{Lm3,f}}{\hat{i}_{T3,\sec}/n} = \frac{4n^2}{\pi^2}R_o \quad (5)$$

Fig. 4 shows the AC resonant circuits excited by the effective sinusoidal input voltage and the effective resistive loads $R_{ac,1}$-$R_{ac,4}$. The input impedances $Z_{in,1}$-$Z_{in,3}$ of the resonant circuits are expressed as:

$$\begin{aligned} Z_{in,1}(f_s) &= Z_{in,2}(f_s) \\ &= \frac{R_{ac,1}(j2\pi f_s L_{m,1})}{R_{ac,1}+j2\pi f_s L_{m,1}} + j2\pi f_s L_{r1} + \frac{1}{j2\pi f_s(C_{r1}+C_{r2})} \\ &= \frac{R_{ac,1}(j2\pi f_s L_m)}{R_{ac,1}+j2\pi f_s L_m} + j2\pi f_s L_r + \frac{1}{j2\pi f_s(2C_r)} \end{aligned} \quad (6)$$

$$\begin{aligned} Z_{in,3}(f_s) &== Z_{in,1}(f_s) = Z_{in,2}(f_s) \\ &= \frac{(R_{ac,3}+R_{ac,4})j2\pi f_s(L_{m3}+L_{m4})}{(R_{ac,3}+R_{ac,4})+j2\pi f_s(L_{m3}+L_{m4})} + j2\pi f_s L_{r3} + \frac{1}{j2\pi f_s(C_{r5}+C_{r6})} \\ &= \frac{R_{ac,1}(j2\pi f_s L_m]}{R_{ac,1}+j2\pi f_s L_m} + j2\pi f_s L_r + \frac{1}{j2\pi f_s(2C_r)} \end{aligned} \quad (7)$$

The frequency modulation (FM) approach is adopted to regulate the AC voltage gain of the resonant circuit. The AC voltage gain of the resonant circuit is approximately expressed as:

$$|G_{ac}(f)| = 1/\sqrt{[1+k(1-\frac{f_r^2}{f_s^2})]^2 + Q^2(\frac{f_s}{f_r}-\frac{f_r}{f_s})^2} \quad (8)$$

where $Q = \sqrt{L_r/(2C_r)}/R_{ac,1}$, $f_r = 1/(2\pi\sqrt{2L_rC_r})$, $k=L_r/L_m$ and f_s is the switching frequency. The DC voltage gain G_{dc} of the proposed converter is given as $G_{dc} = 2nV_o/V_{in}$. The AC voltage gain at the no-load condition (Q=0) and f_s=∞ is given as $|G_{ac}(f)|_{NL,f_s=\infty} = 1/(1+k)$. In order to regulate the output voltage from no-load to full load, the minimum DC voltage gain must be greater than the AC voltage gain at the no-load condition. Thus, the minimum turns ratio of transformers T_1 and T_2 is given in (9).

$$n_{\min} \geq \frac{V_{in,\max}}{2V_o(1+k)} \quad (9)$$

A design example of the prototype circuit is provided in order to verify the system analysis of the proposed converter. A laboratory prototype was constructed to verify the effectiveness of the proposed converter. The electric specifications are V_{in}=750-800 V, V_o=48 V, and $I_{o,rated}$=40 A. The selected series resonant frequency f_r is 120 kHz. The selected inductance ratio L_m/L_r=1/k=7.

A. Turns Ratio of T_1-T_4

In the prototype circuit, the DC voltage gain is equal to $G_{dc} = 2nV_o/V_{in}$. Thus, the minimum turns ratio is given as $n = G_{dc,\min}V_{in,miax}/(2V_o)$. If the minimum DC voltage gain is selected as unity at the series resonant frequency, then the turns ratio of T_1-T_4 is given as:

$$n_1 = n_2 = \frac{n_p}{n_s} = \frac{G_{dc,\min}V_{in,\max}}{2V_o} = \frac{1\times 800}{2\times 48} = 8.33 \quad (10)$$

$$n_3 = n_4 = \frac{n_1}{2} = 4.166 \quad (11)$$

The actual primary and secondary turns used in T_1-T_4 are $n_{p,T1}$=$n_{p,T2}$=66 turns, $n_{s,T1}$=$n_{s,T1}$=8 turns, $n_{p,T3}$=$n_{p,T4}$=33 turns and $n_{s,T3}$=$n_{s,T4}$=8 turns. The actual turns ratios of T_1 and T_2 are 8.25, and the turns ratios of T_3 and T_4 are 4.125.

B. DC Voltage Gain of the Proposed Converter

Based on the selected turns ratio of T_1-T_4, the minimum and maximum DC voltage gains of the proposed converter are derived as:

$$G_{dc,\min} = \frac{2nV_o}{V_{in,\max}} = \frac{2\times(66/8)\times 48}{800} = 0.99 \quad (12)$$

$$G_{dc,\max} = \frac{2nV_o}{V_{in,\min}} = \frac{2\times(66/8)\times 48}{750} = 1.056 \quad (13)$$

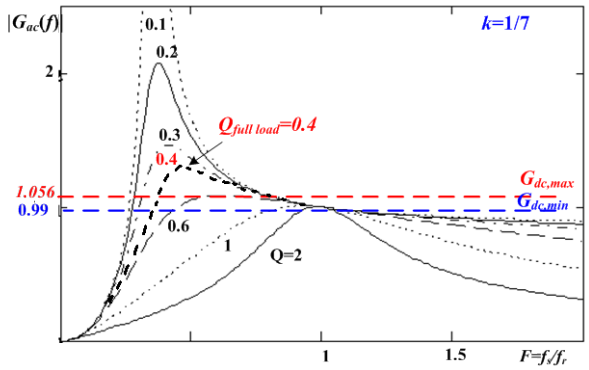


Fig. 5. AC voltage gain and DC voltage gain at different frequency ratio f_s/f_r.

C. Q Value at Full Load and AC Equivalent Resistance

Fig. 5 gives the AC voltage gain versus the frequency ratio f_s/f_r with k=1/7. Since the minimum and maximum DC gains are 0.99 and 1.056, respectively, the maximum Q at a full load should be less than 0.4 in order to effectively regulate the output voltage. In this prototype, the Q value at a full load is selected as 0.4. Based on (4) and (5), the AC equivalent resistances $R_{ac,1}$-$R_{ac,4}$ at a full load are derived as:

$$R_{ac,1} = R_{ac,2} = \frac{8n^2}{\pi^2}R_o = \frac{8\times(66/8)^2}{3.14159^2}\times\frac{48}{40} \approx 66.2\Omega \quad (14)$$

$$R_{ac,3} = R_{ac,4} = \frac{4n^2}{\pi^2}R_o = \frac{4\times(66/8)^2}{3.14159^2}\times\frac{48}{40} \approx 33.1\Omega \quad (15)$$

D. Resonant Capacitances and Inductances

Since $f_r = 1/2\pi\sqrt{2L_rC_r}$ and $Q = \sqrt{L_r/(2C_r)}/R_{ac,1}$, the resonant capacitances C_{r1}-C_{r6} and inductances L_{r1}-L_{r3} are obtained as:

$$L_{r1} = L_{r2} = L_{r3} = L_r = \frac{QR_{ac,1}}{2\pi f_r} = \frac{0.4\times 66.2}{2\pi\times 120000} \approx 35\mu H \quad (16)$$

$$C_{r1} = \ldots = C_{r6} = C_r = \frac{1}{8\pi^2 L_r f_r^2} = \frac{1}{8\pi^2\times 35\times 10^{-6}\times(120000)^2} \approx 25nF \quad (17)$$

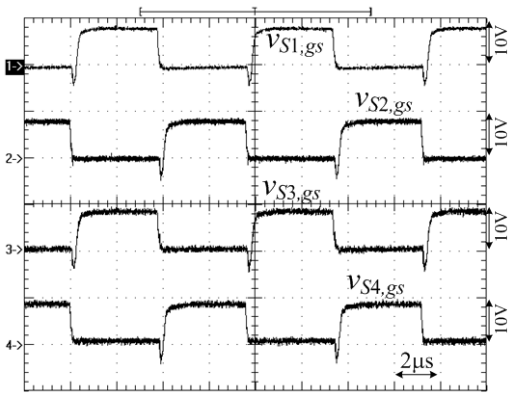
The magnetizing inductances of T_1-T_4 are expressed as:

$$L_{m1} = L_{m2} = L_r/k = \frac{35\mu H}{1/7} = 245\mu H \quad (18)$$

$$L_{m3} = L_{m4} = L_{m1}/2 = 122.5\mu H \quad (19)$$

E. Power Semiconductors

The input maximum voltage is 800 V and the voltage stresses of S_1-S_4 are equal to V_{in}/2=400 V. Power MOSFETs (IRFP460) with a 500 V voltage rating and a 13 A current rating at $100^{\circ}C$ are used for power switches S_1-S_4. The output voltage is 48 V and the load current is 40 A. The average currents of D_1-D_4 are equal to 40 A/4=10 A. The voltage stresses of D_1-D_4 are equal to $2V_o$=96 V. Fast



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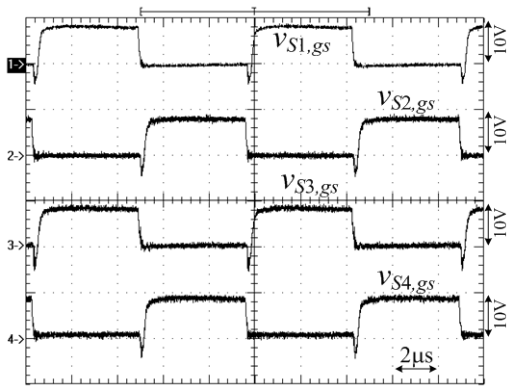

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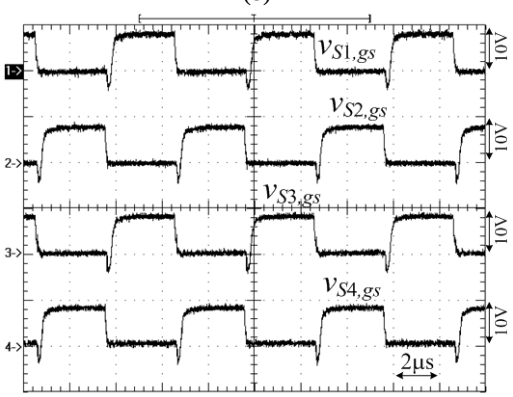

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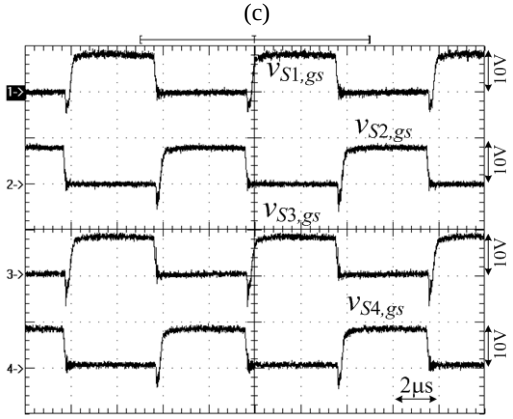


(d)

Fig. 6. Measured PWM waveforms of S_1-S_4 at (a) V_{in}=750 V and 25% load. (b) V_{in}=750 V and 100% load. (c) V_{in}=800 V and 25% load. (d) V_{in}=800 V and 100% load.

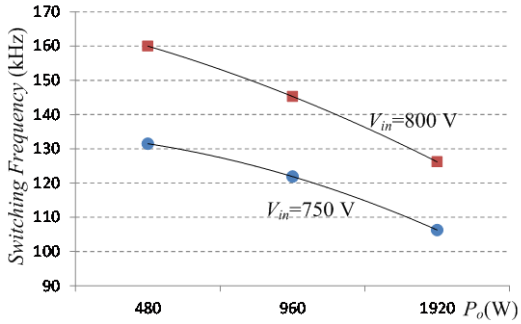
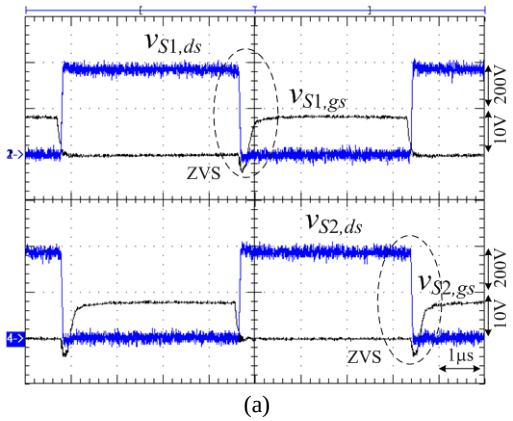


Fig. 7. Measured switching frequencies at different input voltages and load conditions.

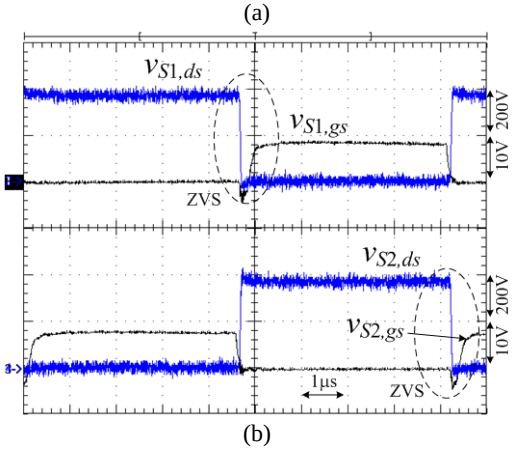
recovery diodes (KCU30A20) with a 200 V voltage rating and a 30 A current rating are adopted for D_1-D_4 in the prototype circuit.

IV. Experimental Results

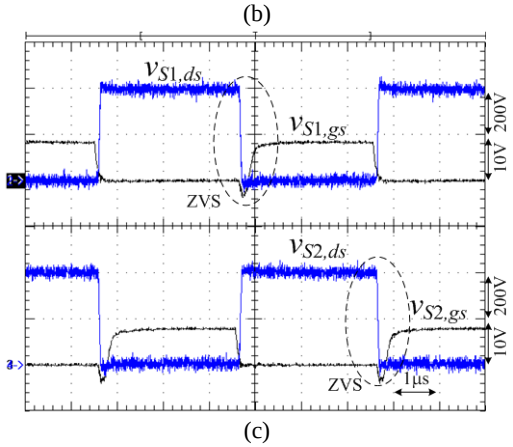
Based on the derived circuit parameters in the previous section, experimental verification is provided to demonstrate the performance of the proposed circuit. The measured PWM waveforms of S_1-S_4 at different input voltages and load conditions are given in Fig. 6. S_1 and S_3 have the same PWM waveforms, and S_2 and S_4 have identical PWM signals. However, the PWM signals of S_1 and S_2 are complementary each other to avoid short circuits at each half-bridge leg. At the same load power, the switching frequency at a low input voltage V_{in}=750 V is less than the switching frequency at a high input voltage V_{in}=800 V. At the same input voltage, V_{in}=800 V, the switching frequency at a full load is less than the switching frequency at a light load. Fig. 7 gives the measured switching frequency of the proposed converter at different input voltages and load conditions. The measured waveforms of the gate voltage and drain voltage of S_1 and S_2 at different input voltages and load conditions are illustrated in Fig. 8. In the same manner, Fig. 9 gives the test results of the gate voltage and drain voltage of S_3 and S_4 at different input voltages and load conditions. Before S_1-S_4 are turned on, the drain voltages are decreased to zero voltage. Therefore, the ZVS turn-on of S_1-S_4 is achieved. Fig. 10 shows the test waveforms of i_{Lr1}-i_{Lr3} at a full load and different input voltages. It is clear that inductor currents i_{Lr1} and i_{Lr2} are balanced. Fig. 11(a) shows the test waveforms of v_{Cr1}-v_{Cr6} at a full load and V_{in}=750 V. It is clear that v_{Cr1}, v_{Cr3} and v_{Cr6} have the same voltage waveforms and that the voltage waveforms of v_{Cr2}, v_{Cr4} and v_{Cr5} are balanced. Fig. 11(b) shows the test results of v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{C4} and v_{Cr5}+v_{Cr6}. From the test results in Fig. 11(b), it can be seen that the three voltages v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr5}+v_{Cr6} are balanced. In the same manner, the measured voltages v_{Cr1}-v_{Cr6}, v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr5}+v_{Cr6} at V_{in}=800 V are shown in Fig. 12. Fig. 13 shows the measured gate voltage $v_{S1,gs}$ and the output diode currents i_{D1}-i_{D4} at a full load and



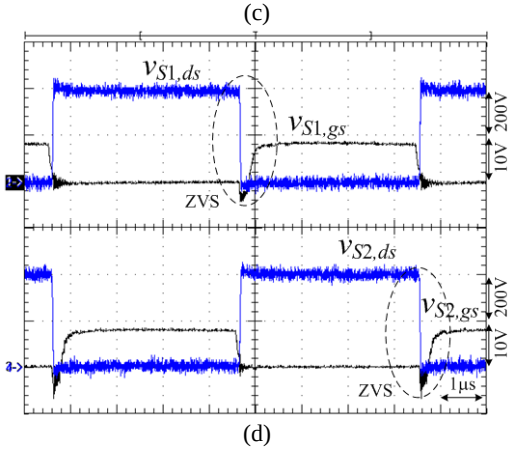
(a)



(b)

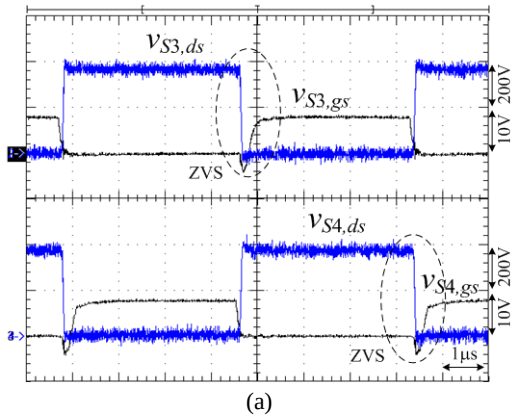


(c)

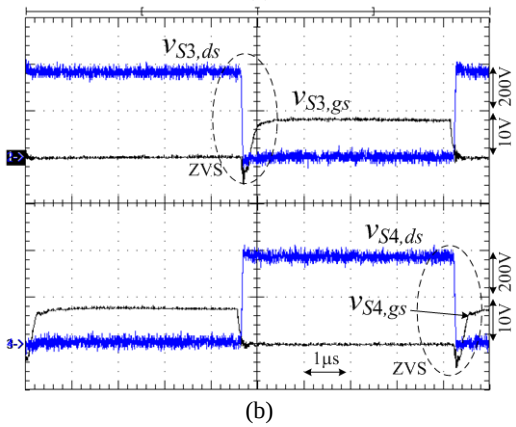


(d)

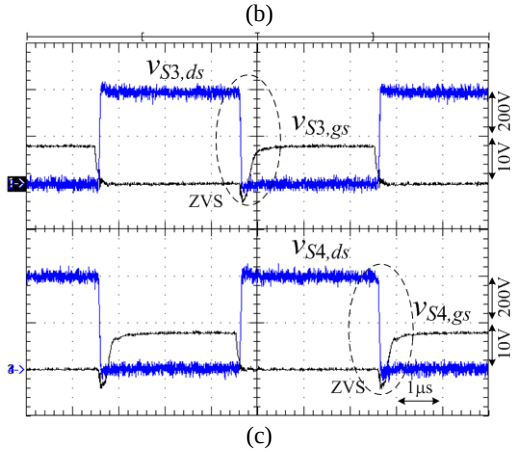
Fig. 8. Measured results of gate voltage and drain voltage of active switches. (a) S_1 and S_2 at 25% load with V_{in}=750 V. (b) S_1 and S_2 at 100% load with V_{in}=750 V. (c) S_1 and S_2 at 25% load with V_{in}=800 V. (d) S_1 and S_2 at 100% load with V_{in}=800 V.



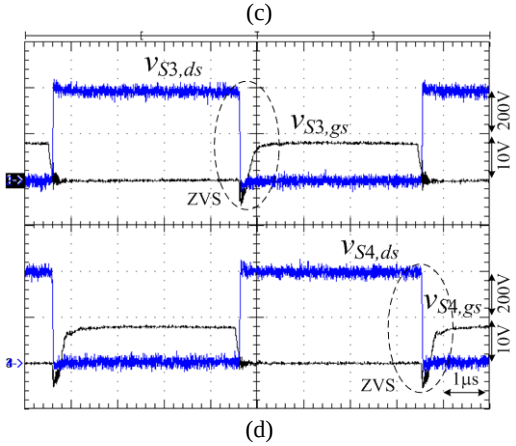
(a)



(b)



(c)



(d)

Fig. 9. Measured results of gate voltage and drain voltage of active switches. (a) S_3 and S_4 at 25% load with V_{in}=750 V. (b) S_3 and S_4 at 100% load with V_{in}=750 V. (c) S_3 and S_4 at 25% load with V_{in}=800 V. (d) S_3 and S_4 at 100% load with V_{in}=800 V.

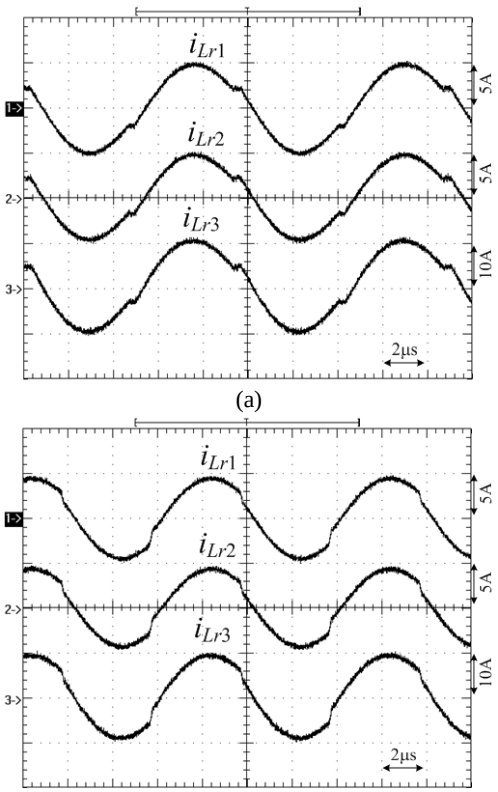


Fig. 10. Measured results of the resonant inductor currents i_{Lr1}-i_{Lr3} at full load and (a) V_{in}=750 V. (b) V_{in}=800 V.

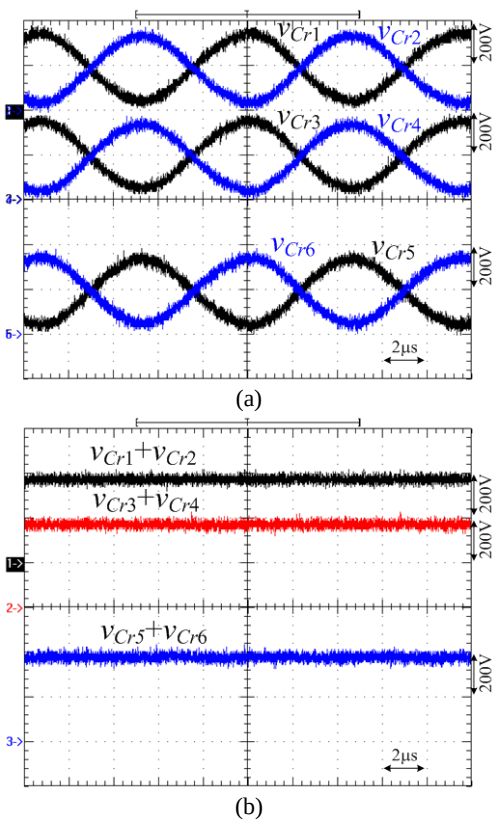


Fig. 11. Measured capacitor voltage waveforms of C_{r1}-C_{r6} at V_{in}=750 V and full load. (a) v_{Cr1}-v_{Cr6}. (b) v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr5}+v_{Cr6}.

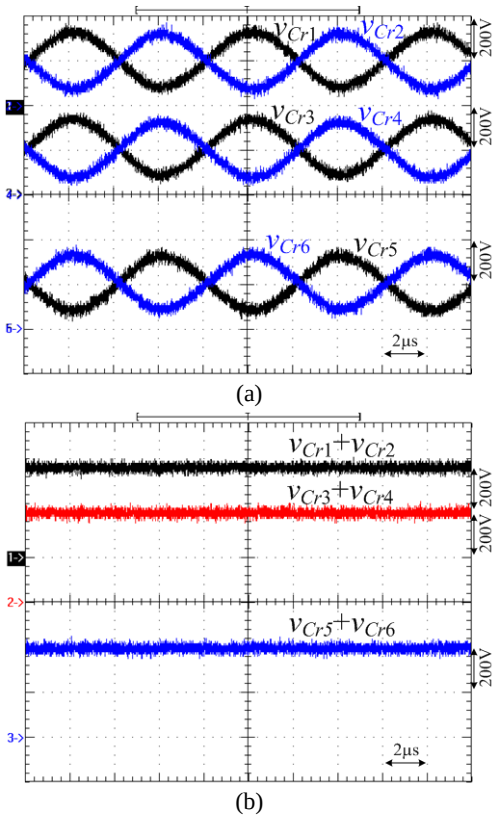


Fig. 12. Measured capacitor voltage waveforms of C_{r1}-C_{r6} at V_{in}=800 V and full load. (a) v_{Cr1}-v_{Cr6}. (b) v_{Cr1}+v_{Cr2}, v_{Cr3}+v_{Cr4} and v_{Cr5}+v_{Cr6}.

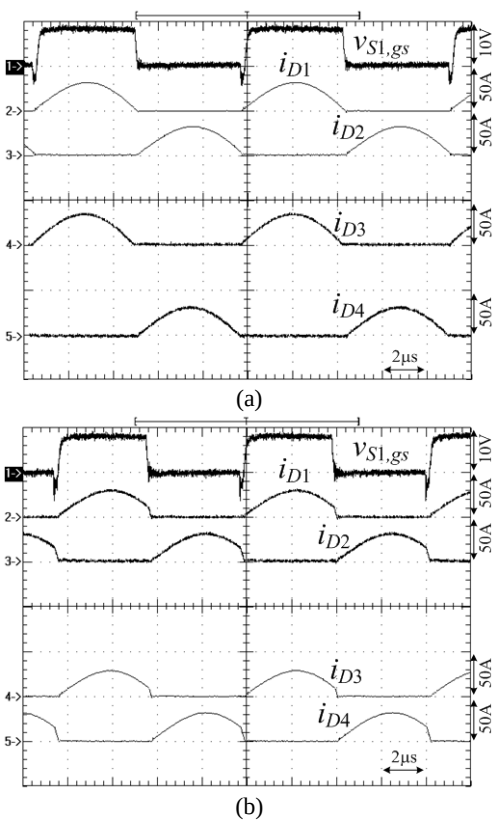


Fig. 13. Measured output diode currents at full load under (a) V_{in}=750 V (b) V_{in}=800 V.

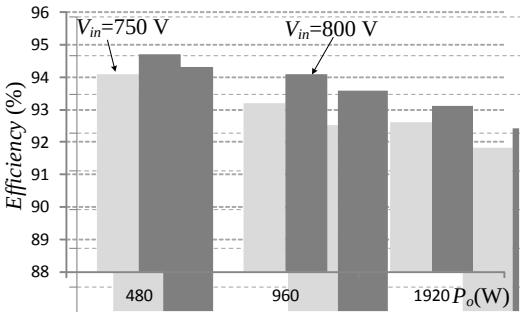


Fig. 14. Measured efficiencies at different input voltages and load conditions.

different input voltages. The diode currents i_{D1} and i_{D3} are balanced, and i_{D2} and i_{D4} are also balanced. The measured circuit efficiencies at different loads are shown in Fig. 14. The measured efficiency is greater than 92% from a 25% load to a full load.

V. Conclusion

A new soft switching DC/DC converter with balanced diode currents at the output side and low voltage stress of the power MOSFETs is presented for medium voltage applications. Three resonant circuits are adopted at the primary side and a series-connection of isolation transformers at the secondary side in order to balance the output diode currents of the proposed converter. The power rating of each resonant circuit is equal to half of the load power so that the current stresses of the passive components and transformer windings are reduced. Two half-bridge circuits with four spilt capacitors are adopted so that the voltage stress of the power MOSFETs are clamped at half of the input voltage. Two resonant capacitors C_{r5} and C_{r6} are also adopted to balance the input split capacitor voltages. When compared to conventional parallel three-level converters, the proposed converter has a lower power switch count. Finally, experiments with a 1.92 *k*W prototype are provided to demonstrate the performance of the converter.

Acknowledgment

This project is supported by the National Science Council of Taiwan under Grant NSC 102-2221-E-224 -022 -MY3.

References

[1] S.-Y. Cho, I.-O. Lee, J.-K. Kim, and G.-W. Moon, "A new standby structure based on a forward converter integrated with a phase-shift full-bridge converter for server power supplies," *IEEE Trans. Power Electron.*, Vol. 28, No. 1, pp. 336-346, Jan. 2013.

[2] Z. Guo, D. Sha, X. Liao, and J. Luo, "Input-series-output-parallel phase-shift full-bridge derived DC–DC converters with auxiliary LC networks to achieve wide zero-voltage switching range," *IEEE Trans. Power Electron.*, Vol. 29 , No. 10, pp. 5081-5086, Oct. 2014.

[3] B. Gu, J.-S. Lai, N. Kees, and C. Zheng, "Hybrid-switching full-fridge DC–DC converter with minimal voltage stress of bridge rectifier, reduced circulating losses, and filter requirement for electric vehicle battery chargers," *IEEE Trans. Power Electron.*, Vol. 28, No. 3, pp. 1132-1144, Mar. 2013.

[4] Y. Jiang, Z. Chen, and J. Pan, "Zero-voltage switching phase shift full-bridge step-up converter with integrated magnetic structure," *IET Proceedings –Power Electron.*, Vol. 3, No. 5, pp. 732-739, 2010.

[5] B. M. Song, R. McDowell, A. Bushnell, and J. Ennis, "A three-level DC-DC converter with wide input voltage operations for ship-electric-power-distribution systems," *IEEE Trans. Plasma Science.* Vol. 32, No. 5, pp. 1856-1863, Oct. 2004.

[6] A. D. Cheok, S. Kawamoto, T. Matsumoto, and H. Obi, "High power AC/DC and DC/AC inverter for high speed train," in *Proc. of IEEE TENCON Conf.*, pp. 423-428, 2000.

[7] U. Drofenik and F. Canales, "European trends and technologies in traction," in *Proc. of IPEC Conf.*, 2014.

[8] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM DC-to-DC converter," *IEEE Trans. Power Electron.*, Vol. 8, No. 4, pp. 486-492, Oct. 1993.

[9] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level DC/DC converter," *IEEE Trans. Power Electron.*, Vol. 17, No. 6, pp. 898-904, Nov. 2002.

[10] Y. Gu, Z. Lu, L. Hang, Z. Qian, and G. Huang, "Three-level LLC series resonant DC/DC converter," *IEEE Trans. Power Electron.*, Vol. 20, No. 4, pp. 781-789, Jul. 2005.

[11] Y. Shi and X. Yang, "Zero-voltage switching PWM three-level full-bridge DC–DC converter with wide ZVS load range," *IEEE Trans. Power Electron.*, Vol. 28 , No. 10, pp. 4511-4524, Oct. 2013.

[12] J. L. Duarte, J. Lokos, and F. B. M. van Horck, "Phase-shift-controlled three-level converter with reduced voltage stress featuring ZVS over the full operation range," *IEEE Trans. Power Electron.*, Vol. 28, No. 5, pp. 2140-2150, May 2013.

[13] W. Chen and X. Ruan, "Zero-voltage-switching PWM hybrid full-bridge three-level converter with secondary-voltage clamping scheme," *IEEE Trans. Ind. Electron.*, Vol. 55, No. 2, pp. 644-654, Feb. 2008.

[14] J. P. Rodrigues, S. A. Mussa, I. Barbi, and A. J. Perin, "Three-level zero-voltage switching pulse-width modulation DC-DC boost converter with active clamping," *IET Proc.- Power Electron.*, Vol. 3, No. 3, pp. 345-354, 2010.

[15] B. Yang, F. C. Lee, A. J. Zhang, and G. Huang, "LLC resonant converter for front end DC/DC conversion," in *Proc. of IEEE APEC*, Vol. 2, pp. 1108-1112, 2002.

[16] R. Beiranvand, B. Rashidian, M. R. Zolghadri and S. M. H. Alavi, "Using LLC resonant converter for designing wide-range voltage source," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 5, pp. 1746-1756, May 2011.

[17] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 5, pp. 1321-1329, May 2009.

[18] R. Beiranvand, B. Rashidian, M. R. Zolghadri and S. M. H. Alavi, "A design procedure for optimizing the LLC resonant

converter as a wide output range voltage source," *IEEE Trans. Power Electron.*, Vol. 27, No. 8, pp. 3749-3763, Apr. 2012.
[19] B.-R. Lin and C.-C. Chien, "Analysis and implementation of a new soft switching DC/DC PWM converter," *IET Proc.–Power Electron.*, Vol. 6, No. 1, pp. 202-213, 2013.
[20] B.-R. Lin and H.-Y. Shih, "ZVS converter with parallel connection in primary side and series connection in secondary side," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 4, pp. 1251-1258, Apr. 2011.
[21] B.-R. Lin and P.-J. Cheng, "New ZVS DC--DC converter with series-connected transformers to balance the output currents," *IEEE Trans. Power Electron.*, Vol. 29, No. 1, pp. 246-255, Jan. 2014.
[22] C. Dong and Z. P. Fang, "A family of zero current switching switched-capacitor DC-DC converters," in *Proc. IEEE APEC Conf.*, pp. 1365-1372, 2010.

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