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Single-Phase Bridgeless Zeta PFC Converter with Reduced Conduction Losses

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Abstract

This paper presents a new single phase front-end ac–dc bridgeless power factor correction (PFC) rectifier topology. The proposed converter achieves a high efficiency over a wide range of input and output voltages, a high power factor, low line current harmonics and both step up and step down voltage conversions. This topology is based on a non-inverting buck-boost (Zeta) converter. In this approach, the input diode bridge is removed and a maximum of one diode conducts in a complete switching period. This reduces the conduction losses and the thermal stresses on the switches when compare to existing PFC topologies. Inherent power factor correction is achieved by operating the converter in the discontinuous conduction mode (DCM) which leads to a simplified control circuit. The characteristics of the proposed design, principles of operation, steady state operation analysis, and control structure are described in this paper. An experimental prototype has been built to demonstrate the feasibility of the new converter. Simulation and experimental results are provided to verify the improved power quality at the AC mains and the lower conduction losses of the converter.

Key words: AC-DC converter, Bridgeless rectifier, Conduction losses, Power factor correction, Zeta converter

I. INTRODUCTION

In recent years, single phase ac-dc PFC converters have received much attention due to the dramatic growth in the use of electronic equipment and these ac-dc converters introduce harmonic currents. These harmonic currents cause a lower power factor at the ac mains, voltage distortion and noise [1]-[3]. To comply with harmonic standards and to increase transmission efficiency in power systems, PFC techniques are necessary in ac-dc power converters [4], [5]. In addition, electronic equipment benefits from power converters with high efficiency over a wide range of input and output voltages [6]. However, conventional ac-dc converter designs cannot deliver high efficiency over a wide operation range in both step up and step down voltage conversions and it is difficult to design the control system. Therefore, a new topology design that improves efficiency and reduces the complexity of the control is desirable. In this paper, a novel bridgeless PFC rectifier topology is proposed to achieve these objectives.

The most common PFC converter architecture in the market consists of a front-end diode bridge rectifier circuit where the bridge rectifier is followed by a boost dc-dc converter. The boost converter is popular in PFC converter architecture due to its simple circuit, simple control scheme and low input current harmonics [7]-[13]. However, this architecture is not suitable for high power applications because of the high conduction losses caused by the input diode bridge. In addition, three semiconductors exist in the current flowing path in a complete switching period. Furthermore, one significant drawback of the boost converter which is used in the architecture is that the output voltage of the boost converter is always higher than the input voltage. Besides, the converter does not have the capability to protect against short circuits or load overcurrent [14].

Unlike boost converter, Cuk and SEPIC converters can be operated as a voltage step up or step down converter. However, these converters are not able to protect against the startup inrush current condition. Therefore, an additional circuit is necessary to protect against inrush current [4], [14].

To avoid the rectifier input bridge, a number of bridgeless PFC converter topologies have been proposed by numerous

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authors [12], [15]-[26]. Most of the proposed bridgeless PFC converters utilize a boost topology because of its high efficiency, improved power factor, and simple control scheme. When compared to the boost ac–dc PFC topology, the bridgeless PFC converter solves the heat problem generated by the input bridge rectifier. In addition, current flows through two semiconductor devices during each switching cycle which significantly reduces the total conduction losses. However, the rectifier has the same drawbacks as the boost converter. Furthermore, a complex circuit is needed to sense the current in the MOSFET and diode paths separately, and this topology has the problem of a high startup inrush current [27].

To overcome these constraints, a new single phase bridgeless PFC topology based on Zeta converter is proposed in this paper. The conduction losses are reduced in the proposed converter topology when compare to the conventional PFC converter due to the reduced number of semiconductors in the flowing current path. In addition, a wider operation range (up-and-down voltage conversion) can be achieved. The proposed converter is operated in DCM. Therefore, current loop is not required to shape the input current. As a result, the control circuit is simplified. In addition, the main switch is turned on and the output diode is turned off under zero current switching condition due to the DCM operation. Furthermore, this converter is capable of protecting itself against overload and inrush current. The proposed rectifier topology utilizes four inductors, which are described as a drawback of the topology. However, implementation of the coupled inductor technique can be used to reduce the magnetic components count.

The organization of this paper is as follows: Section 2 presents the new proposed topology design, the principle of operation and analysis. The converter design procedure and an example are explained in detail in Section 3, followed by an efficiency comparison with conventional converter techniques. Section 4 presents simulation results. Section 5 provides experimental validation and analysis of the proposed topology.

II. OPERATION AND ANALYSIS

The power stages of a conventional Zeta PFC rectifier and the proposed bridgeless Zeta PFC rectifier are shown in Fig. 1 and Fig. 2, respectively. The new topology is derived by connecting two ZETAs. The proposed converter acts as a conventional Zeta converter during the positive input source voltage and as an inverting Zeta converter during the negative input source voltage with the same DC voltage gain for either polarity of the input source voltage. The proposed topology utilizes two control switches. However, these switches (Sw_1 and Sw_2) can be driven with the same PWM signal, which reduces the complexity of the rectifier control circuit.

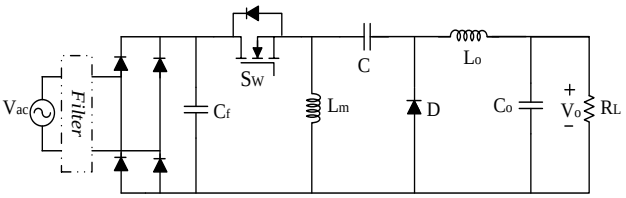


Fig. 1. Conventional Zeta PFC rectifier [28].

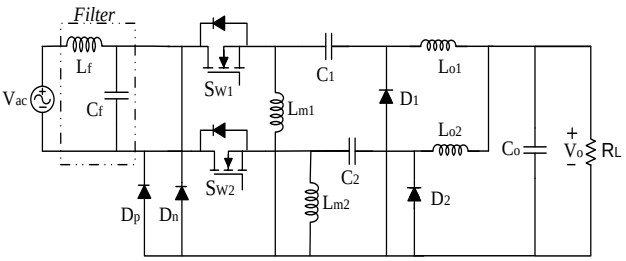


Fig. 2. Proposed bridgeless Zeta PFC.

Fig. 3 and Fig. 4 show the operational circuits of the proposed topology during the positive and negative half cycles of the input voltage, respectively. Referring to Fig. 3 and Fig. 4, one switch and one diode conduct in mode I and only one diode conducts in mode II. Therefore the conduction losses are reduced when compare to the conventional PFC converter. The converter operation is symmetrical in each of the half cycles of the input line voltage. Therefore, it is sufficient to explain the rectifier operation during one complete switching period (T_S) in a positive half period of the input voltage. It is assumed that the inductors in the converter are working in DCM. The operation of the Zeta converter in DCM has several advantages over continuous conduction mode (CCM) operation. These advantages are that the control circuit of the converter is simplified and includes soft turn on of the switch, reduced reverse recovery losses of the diode and inherent power factor correction. To simplify the analysis of the converter, it is assumed that the circuit is operating under the steady state condition and that all of the circuit elements of the converter are considered ideal. Furthermore, the output capacitance is considered to be large enough to make its voltage constant. In addition, the input voltage is assumed to be constant during a switching period.

According to the above assumptions, the converter operation can be classified into three stages in a switching cycle. Theoretical waveforms of the converter in DCM during a complete switching period (*Ts*) are shown in Fig. 5.

First stage (t_0, t_1)**:** When the switch is in the on state, the input source supplies energy to the inductors L_{m1} and L_{o1}, and the current through the inductors increase linearly. The voltages across the capacitors C_1 and C_o are considered to be constant and equal to V_o. In this stage, the diode D_1 is blocked by a reverse voltage V_{Df} that is given by:

$$V_{Df} = -(V_{in} + V_o) \tag{1}$$

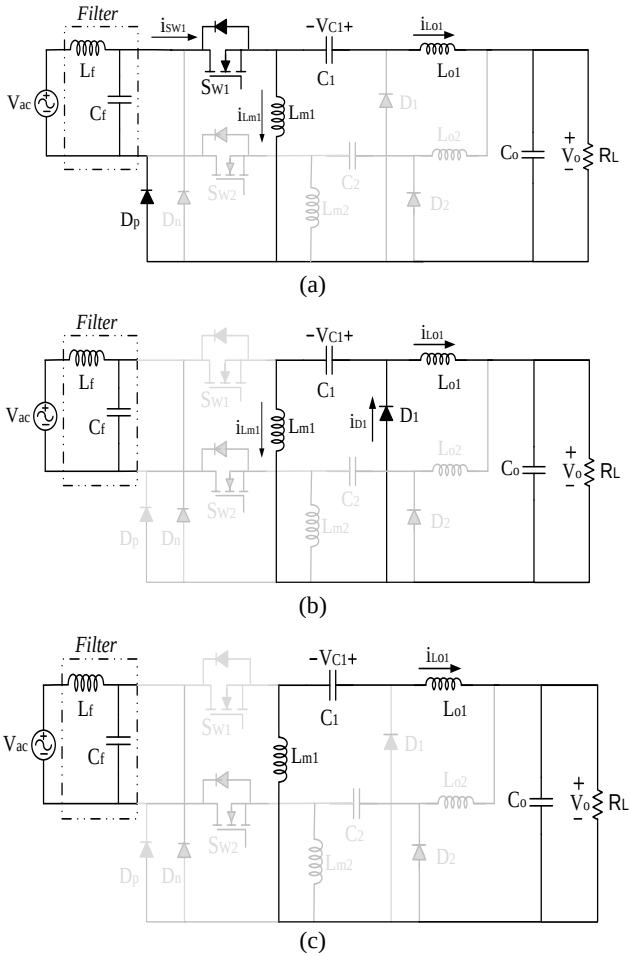


Fig. 3. Proposed converter operation in different modes (a-c) for positive half cycle of line voltage. (a) Mode I. (b) Mode II. (c) Mode III.

Second stage (t_1, t_2): When the switch is turned off, the diode D_1 starts to conduct, and the inductors currents iL_{m1} and iL_{o1} decrease linearly. In this stage, no energy circulates in the main line. As a result, the harmonic distortion is eliminated in the input line current. The voltage across the switch is given by:

$$V_{Sw} = V_{in} + V_o \tag{2}$$

Third stage (t_2, t_3): In this stage, when the currents through the inductors L_{m1} and L_{o1} become equal, the diode D_1 turns off. The voltages applied to the inductors L_{m1} and L_{o1} are zero and the current is constant until the switch is turned on.

The input voltage V_{in} of the converter is given by the following equation:

$$V_{in} = V_m.\sin(\omega t) \tag{3}$$

Referring to the first stage, the following input and output inductors current equations can be obtained.

$$i_{Lm1}(t) = \frac{V_m}{L_{m1}}.t.\sin(\omega t) + iL_{m1,\min} \tag{4}$$

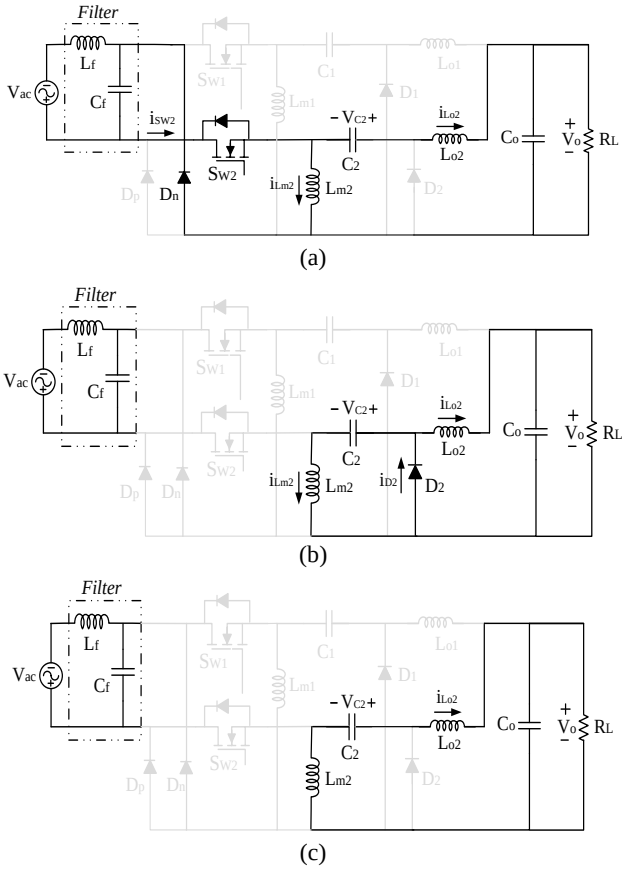


Fig. 4. Proposed converter operation in different modes (a-c) for negative half cycle of line voltage. (a) Mode I. (b) Mode II. (c) Mode III.

$$i_{Lo1}(t) = \frac{V_m}{L_{o1}}.t.\sin(\omega t) + iL_{o1,\min} \tag{5}$$

Where $iL_{m1,\min}$ and $iL_{o1,\min}$ are the minimum inductor currents through the inductors L_{m1} and L_{o1}, respectively. The switch current is given by the sum of the currents through the inductor $L_{m1,}$ and L_{o1} , resulting in:

$$i_{sw1}(t) = i_{Lm1}(t) + i_{Lo1}(t) \tag{6}$$

$$i_{sw1}(t) = \frac{V_m}{L_{eq}}.t.\sin(\omega t) + iL_{m1,\min} + iL_{o1,\min} \tag{7}$$

Where:

$$\frac{1}{L_{eq}} = \frac{1}{L_{m1}} + \frac{1}{L_{o1}} \tag{8}$$

The currents $iL_{m1,\min}$ and $iL_{o1,\min}$ are equal and opposite. Therefore, the switch current can be expressed as follows:

$$i_{Sw1}(t) = \frac{V_m}{L_{eq}}.t.\sin(\omega t) \tag{9}$$

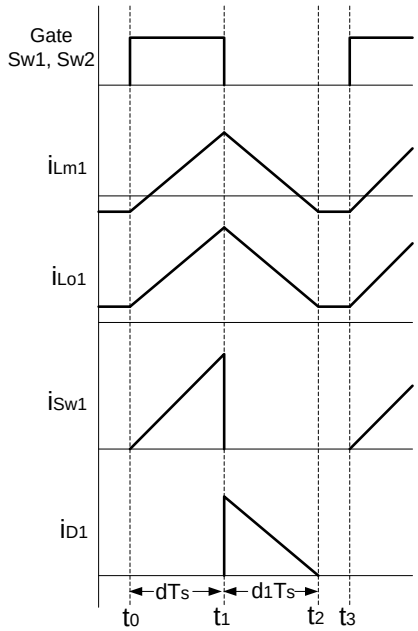


Fig. 5. Theoretical waveforms of the converter in DCM.

From Eq. (9), it can be concluded that the main switch Sw_1 turns on under the zero current switching condition.

In the second stage, the current through the inductors decrease linearly and the inductors current equations are given as follows:

$$iL_{m1}(t) = -\frac{V_0}{L_{m1}}.t + \frac{V_m}{L_{m1}}.\sin(\omega t).dT_S + iL_{m1,\min} \quad (10)$$

$$i_{Lo1}(t) = -\frac{V_0}{L_{o1}}.t + \frac{V_m}{L_{o1}}.\sin(\omega t).dT_S + iL_{o1,\min} \quad (11)$$

In the third stage, the diode current is zero. Referring to Fig. 3(b) and Fig. 3(c), the input current does not circulate. The input current in mode I is given by:

$$i_{in}(t) = i_{Lm1}(t) + i_{Lo1}(t) \quad (12)$$

Since, the currents $iL_{m1,\min}$ and $iL_{o1,\min}$ are equal and opposite in polarity, the input current can be simplified as follows:

$$i_{in}(t) = \frac{V_m}{L_{eq}}.t.\sin(\omega t) \quad (13)$$

The converter has an input filter to eliminate the harmonics. Therefore:

$$i_{in}(t) = \frac{V_m.D}{L_{eq}.f_s}.\sin(\omega t) \quad (14)$$

Where, D = Duty cycle and fs= switching frequency. From Eq. (14), it can be concluded that the low order harmonics do not exist in the converter [11].

III. Design Procedure and Example

This topology is derived by connecting two ZETAs. Therefore, the design procedure is similar to the conventional Zeta converter. In this section, an example of the proposed converter with the following specifications is explained.

A. Input Data

Output power: P_{out} = 150 W
Output voltage: V_o = 150 V
Switching frequency: f_s = 30 kHz
Line frequency: f_L = 50Hz;
Output voltage ripple: Δvo = ±2% $_{(max)}$ of Vo
Input voltage:

$$V_{in} = V_m \sin(2\pi 50t) = 311\sin(2\pi 50t)$$

Where, V_m is the peak input voltage.

The input current can be obtained from the following equation:

$$I_{in} = I_1 \sin(\omega t) = \frac{2P_{out}}{\eta V_m}\sin(\omega t) \quad (15)$$

If the efficiency is 90%, the input current can be expressed as:

$$I_{in} = 1.07\sin(2\pi 50t) \quad (16)$$

The equivalent load resistance is:

$$R_{eq} = \frac{V_o^{\,2}}{P_{out}} = 150\Omega \quad (17)$$

The output current I_o is calculated as follows:

$$I_o = \frac{P_{out}}{V_o} = 1A \quad (18)$$

B. Ensuring DCM Operation

The critical value of the inductance to operate at the boundary of the CCM and DCM is given as follows [14]:

$$L_c = \frac{\alpha.V_m.D_c^{\,2}}{4.I_o.f_s} = 584\mu H \quad (19)$$

Where:

$$\alpha = \frac{V_m}{V_o} \quad (20)$$

And:

$$D_C = \frac{1}{1+\alpha} \quad (21)$$

Where D_c is the critical duty cycle.

To ensure the DCM operation, the inductors L_{m1} and L_{m2} are selected as 500μH and the output inductances L_{o1} and L_{o2} are selected as 500μH [14].

The DC link capacitor is calculated as follows [29]:

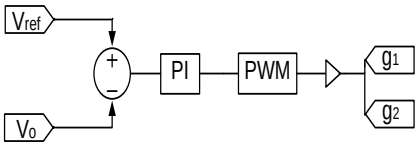


Fig. 6. Controller block diagram.

$$C_o = \frac{I_o}{2\omega\Delta V_o} = 796uF \quad (22)$$

Hence, the value of the DC link capacitor is selected as 990μF.

C. Maximum Ratings of the Switching Devices

The voltage stress of the main switch in the circuit is equal to the sum of the input voltage and the output voltage. Therefore, the maximum voltage across the switch is:

$$V_{SW,\max} = V_m + V_o = 461\text{V} \quad (23)$$

The peak voltage across the diode is:

$$V_{D,peak} = V_m + V_o = 461\text{V} \quad (24)$$

D. Control Circuit

The control of the Zeta converter in DCM is relatively simple. Due to the DCM operation, the converter only requires sensing of the output voltage, and current feedback is not required to shape the input current. Thus, the input current sensor can be eliminated. A simplified control block diagram of the converter is shown in Fig. 6.

The proposed converter is controlled using the voltage follower approach and a Pulse Width Modulation (PWM) signal is generated to maintain a desired DC output voltage. The discrete PI control scheme is used for the digital control of the converter. The error between the reference DC link voltage (V_{ref}) and the sensed DC link voltage (V_o) is fed to the PI voltage controller. The function of the discrete PI controller is to generate the control output V_C based on the error voltage V_e.

Where:

$$V_e = V_{ref} - V_o \quad (25)$$

The control output equation of a discrete PI controller at the k^{th} instant can be expressed as follows:

$$V_C(K) = V_C(K-1) + K_P\{V_e(K) - V_e(K-1)\} + K_i V_e(K) \quad (26)$$

Where:

K_P is the proportional gain, and K_i is the integral gain of the voltage controller.

The control output (V_C), after limiting, is considered to be a modulating signal for the PWM controller to generate the appropriate duty ratio of the switches S_{W1} and S_{W2}.

The Ziegler and Nichols suggested rule is used for tuning the PI controller (K_p and K_i). This method avoids the need for a model of the complex converter to be controlled, and solely relies on the step response of the converter. The values of the controller are determined based on the transient response characteristics of the converter. The step response curve of the converter is generated from a simulation. The Ziegler and Nichols method applies if the response to a step input exhibits an S-shaped curve [30]. The simulated curve of the converter is also an S-shaped curve, as shown in fig 7.

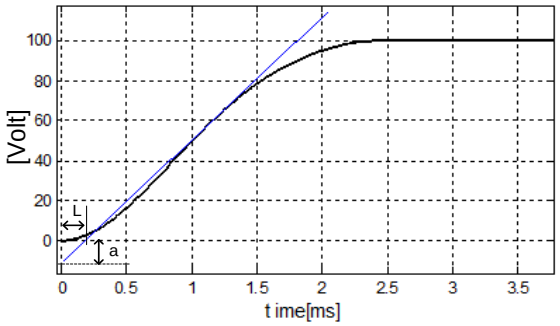


Fig. 7. Step response for the tuning of PI controllers according to Ziegler and Nichols Method.

TABLE I
TUNING OF PID CONTROLLER PARAMETERS
ACCORDING TO ZIEGLER AND NICHOLS METHOD [31]

Controller	K_p	T_i	T_d
P	1/a		
PI	0.9/a	3L	
PID	1.2/a	2L	L/2

The parameter for setting the PI controller according to the Ziegler and Nichols method is carried out in four steps as follows [31].

1) Obtain the plant step response, as shown in Fig. 7.
2) Draw the steepest straight-line tangent to this response.
3) Obtain the values of "a" and "L", from Fig. 7.
4) Set the parameters according to Table I

According to the Ziegler and Nichols method, the value of K_p is 0.075, and the value of K_i is 0.27. The control system of the converter is implemented using a DSP microcontroller (TMS320F28335).

E. Efficiency Improvement

Based on the circuit operation, the efficiency improvement of the proposed rectifier is verified by calculating the conduction losses of the reduced input bridge diodes during each switching cycle. The power dissipation of each bridge diode due to the conduction loss can be calculated by using the following equation:

$$P_{D,avg} = \frac{1}{T}\int_0^T V_D . I_D dt \quad (27)$$

When the gate signals are turned on, one diode of the

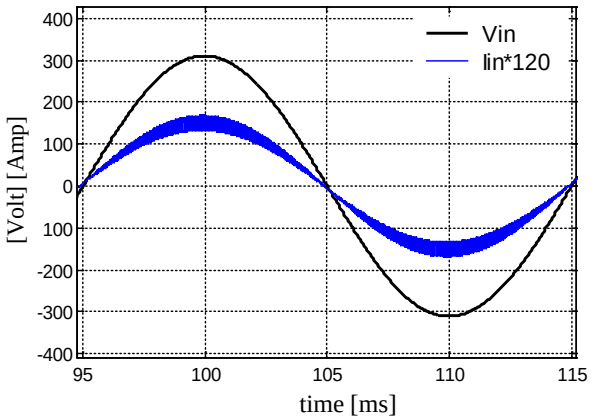


Fig. 8. Simulation waveforms of input voltage and input current.

proposed circuit is reduced in the input current flowing path when compare to the conventional Zeta PFC rectifier circuit. Therefore, the conduction loss of one diode can be calculated as follows:

$$P_{D,avg(on)} = \frac{1}{T}\int_0^T V_D.I_D.D dt \quad (28)$$

$$= \frac{1}{\pi}\int_0^\pi 1*1.07*0.25\sin(\omega) d\omega$$

$$P_{D,avg(on)} = 0.17\,\text{W} \quad (29)$$

When the gate signals are turned off, the input bridge is omitted from the converter. Therefore, the conduction losses of two diodes can be calculated as follows:

$$P_{D,avg(off)} = \frac{1}{T}\int_0^T 2.V_D.I_D.(1-D) dt \quad (30)$$

$$= \frac{1}{\pi}\int_0^\pi 2*1*1.07*0.75\sin(\omega) d\omega$$

$$P_{D,avg(off)} = 1.02\,\text{W} \quad (31)$$

Therefore, the efficiency improvement can be calculated by using the following equation:

$$\eta_{impv} = \frac{P_{D,avg(on)} + P_{D,avg(off)}}{150} = 0.8\,\% \quad (32)$$

IV. Simulation Results

The proposed bridgeless Zeta PFC rectifier is simulated with the following specifications: $v_{in} = 311\ sin(\omega t)$, $f_L = 50$Hz, $f_s = 30$kHz, $L_{m1}=L_{m2}=500\mu H$, $L_{o1}=L_{o2}=500\mu H$, $C_1=C_2=1\mu F$, $C_o=990\mu F$, and $R_L = 150\Omega$. Fig. 8 shows the input current and input voltage of the converter under a full load to demonstrate the power quality. It can be observed that the source voltage and source current are in phase and sinusoidal with 4.18% THD of the input current. It can also be seen that the power factor is around 0.994. Since, the converter is operated in

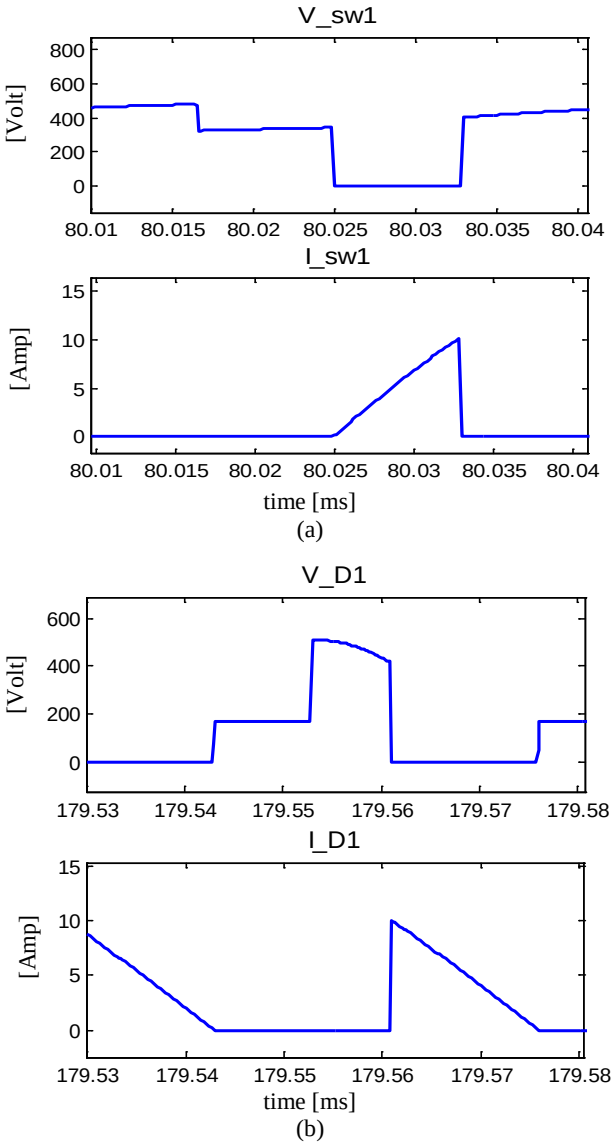


Fig. 9. Simulated waveforms of MOSFET and diode in DCM.

DCM, the main switch is turned on under the zero current switching condition, and the output diode is turned off under the zero current switching condition, as shown in Fig. 9 (a) and Fig. 9 (b), respectively. Therefore, the reverse recovery problem of the diode is resolved by employing the DCM operation of the Zeta converter. The simulated waveforms of the input and output inductor current and the switch current are shown in Fig. 10. Fig. 11 (a) and Fig. 11 (b) show the current of the main switches and output diodes during the positive and negative half cycles of the input voltage, respectively. The peak to peak output voltage ripple is shown in Fig. 11 (c).

V. Experimental Results

This section presents experimental results of the proposed bridgeless Zeta PFC converter and comparisons with the

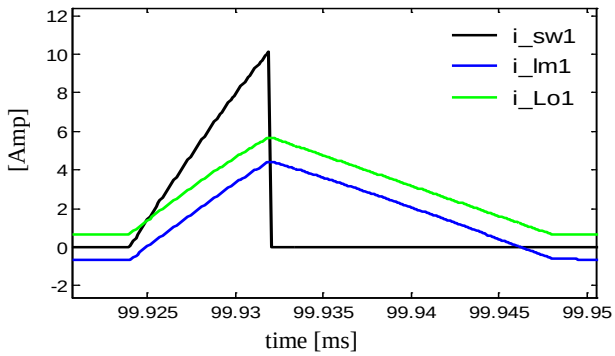


Fig. 10. Simulated waveforms for the converter in DCM.

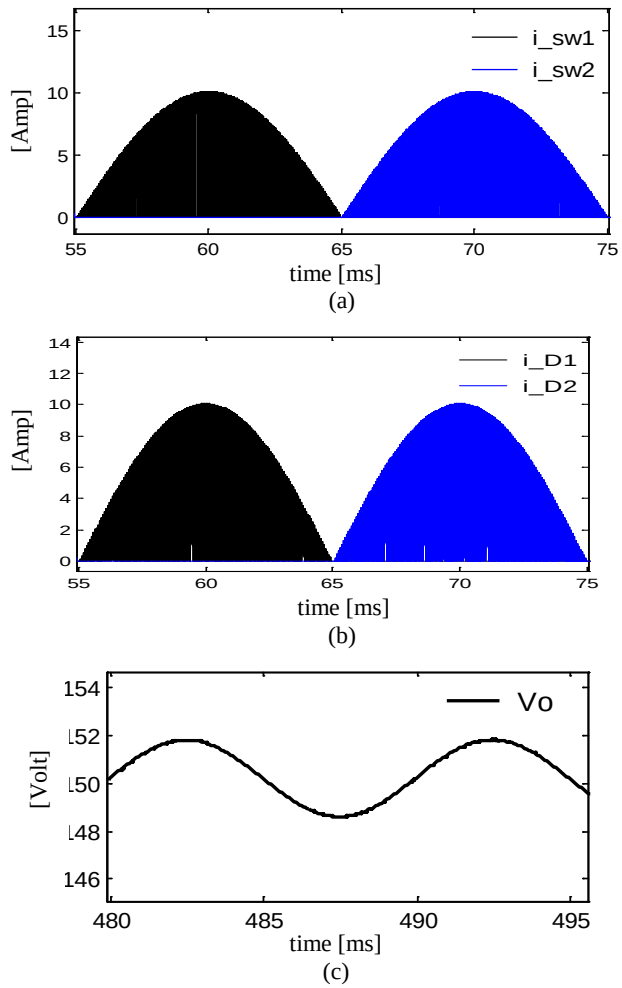


Fig. 11. Simulated waveforms. (a) Switch current. (b) Diode current. (c) DC output voltage.

conventional Zeta PFC converter. The proposed converter operates at 30kHz and utilizes IPP60R099C6 switches with $R_{DS(on),max}$ = 0.099 Ω and 20ETF06PBF diodes. The prototype parameters of the proposed converter are listed in Table II, and the conventional Zeta PFC converter specifications are as follows: L_m=1mH, L_o=1mH, C=2μF, and C_o=990μF. Fig. 12 shows experimental results of the input voltage and input current. It can be observed that the

TABLE II
EXPERIMENTAL CONVERTER PARAMETERS

Input voltage v_{ac}	120 V_{rms}
Output voltage V_o	60 V_{dc}
Output power P_{out}	40 W
Input inductor Lm_1=Lm_2	500 μH
Output inductor L_{o1}=L_{o2}	500 μH
Coupling capacitor C_1=C_2	1 μF
Filter capacitor C_o	990 μF
Switching frequency f_s	30 kHz
Diodes D_1,D_2,D_n,D_p	20ETF06PBF
MOSFET Sw_1,Sw_2	IPP60R099C6 With $R_{DS(on),max}$ = 0.099 Ω

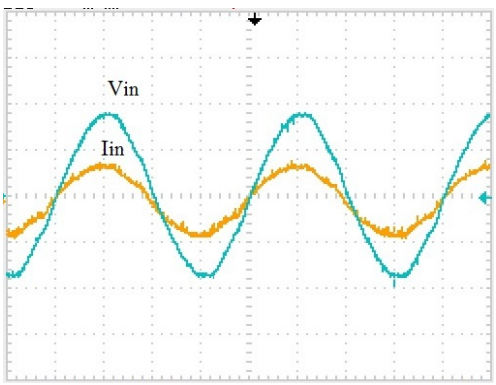


Fig. 12. Line voltage and input line current [V: 100V/div, I: 1 A/div, t: 5 ms/div].

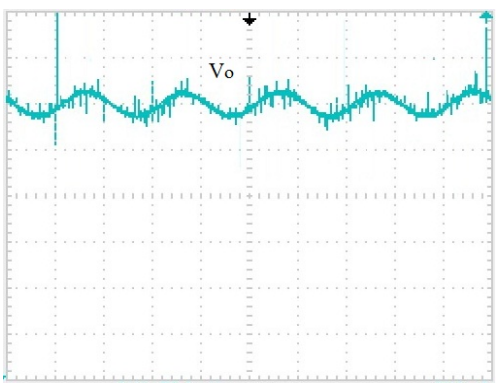
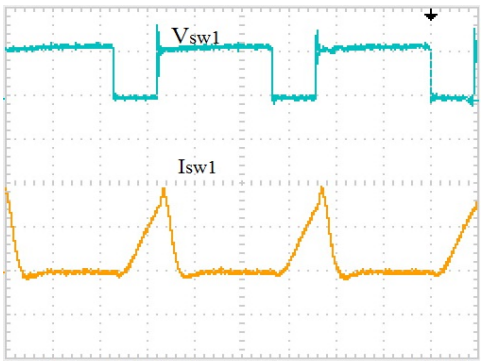
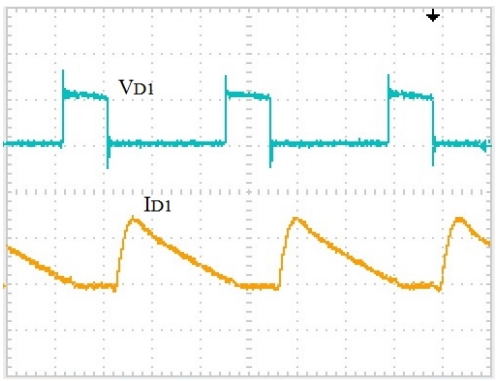


Fig. 13. Output voltage ripple at 60V dc [V: 5V/div, t: 10 ms/div].

input line current is a perfect replica of the input line voltage and that the measured power factor is near unity. The peak to peak output voltage ripple is less than 4 at 60V of output voltage and 40W of output power, as shown in Fig. 13. Fig. 14 (a) and Fig. 14 (b) illustrate the switching waveforms of the MOSFET and diode, respectively. It can be observed that the MOSFET turns on and the diode turns off under the zero current condition due to the DCM operation of the converter. The voltage of the capacitor C_1 is shown in Fig.15. Fig.16 shows the behavior of the output voltage of the PI controller when the input voltage changes. A comparative analysis of the number of diode conducts during each switching period in



(a)



(b)

Fig. 14. Voltage and current waveform of (a) switch Sw_1 [V: 200V/div, I: 2A/div, t:10 µs/div] (b) diode D_1 in a switching period [V: 200V/div, I: 2A/div, t:10 µs/div].

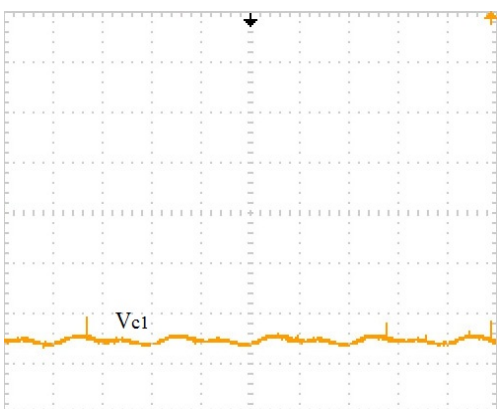


Fig. 15. Voltage waveform of capacitor C_1 [V: 50 V/div, t: 5ms/div].

DCM of the proposed converter with the existing bridgeless PFC topologies and the conventional Zeta PFC is shown in Table III**.** The measured power factor curve of the proposed converter is provided in Fig.17, and it is compared with the conventional Zeta PFC converter. The power factor of the proposed converter is close to 0.99 at 190 Vrms of input voltage. The input current THD of the conventional Zeta and the proposed PFC converter curve is shown in Fig. 18. The measured input current THD of the proposed converter was 1.2% at 190 V_{rms} of input voltage. Fig.19 shows an efficiency comparison between the proposed converter and the

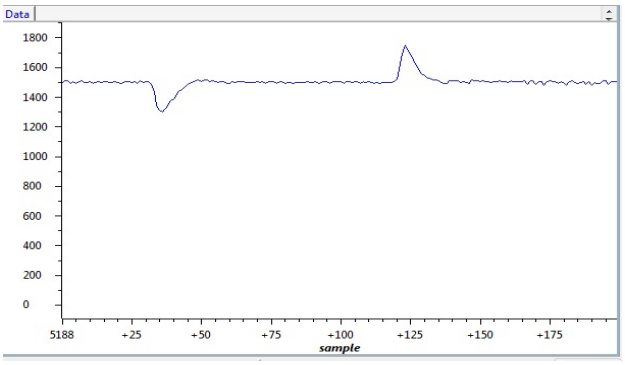


Fig. 16. Behavior of the output voltage of the PI controller, in experiment, due to input voltage variations.

TABLE III
COMPARATIVE ANALYSIS OF PROPOSED CONVERTER WITH EXISTING PFC TOPOLOGIES IN DCM

Configuration	No. of diode conducts during each switching stage in DCM		
	Stage 1	Stage 2	Stage 3
BL-Cuk [32]	2	3	2
BL-SEPIC[5]	2	3	2
Con.Zeta [28]	2	3	2
Proposed	1	1	0

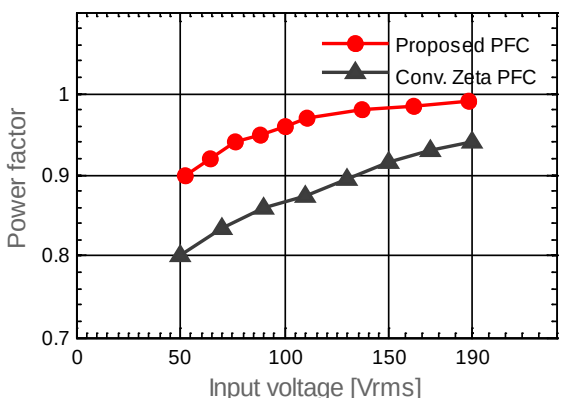


Fig. 17. Power Factor versus input voltage curve.

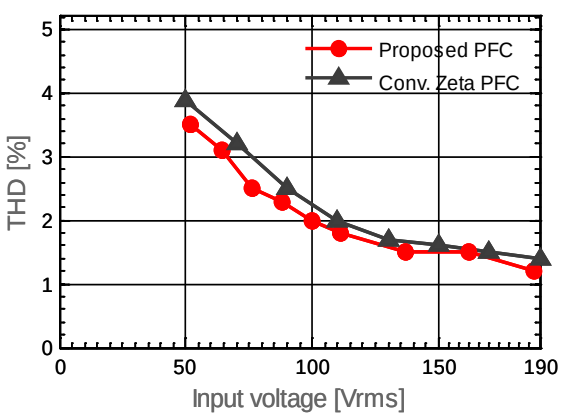


Fig. 18. Total harmonic distortion versus input voltage curve.

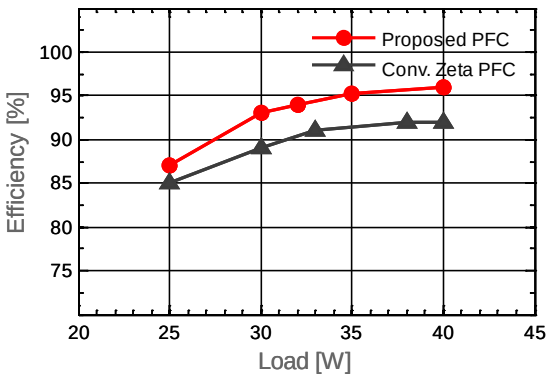


Fig. 19. Measured efficiency curve at Vin = 120 Vrms and Vo = 60 V.

conventional Zeta PFC converter. The proposed converter achieves a 96% peak efficiency at 40W of output power, 120 V_{rms} of input voltage and 60V of output voltage.

VI. Conclusions

In this paper, a new bridgeless ac-dc converter with a low input current ripple and lower conduction losses has been presented. The proposed topology addresses several of the disadvantages of the conventional Zeta PFC converter through the development of a new bridgeless topology. The front end bridgeless Zeta PFC converter has been operated in discontinuous conduction mode to achieve an inherent power factor correction. Due to the DCM operation, the current control loop is eliminated and the control circuit is simplified. The main features of the converter are that the input diode bridge is eliminated and the efficiency is improved when compare to a conventional PFC rectifier. The merits of the proposed design include a high efficiency, an improved power factor, low line current harmonics, and operation across a wide range of input and output voltages. In addition, theoretical analyses of the proposed scheme and simulation results have been presented. Finally a prototype of the proposed converter has been built to validate its performance.

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