IEIE Transactions on Smart Processing and Computing, vol. 4, no. 1, February 2015
http://dx.doi.org/10.5573/IEIESPC.2015.4.1.059

Design of 10-bit 10MS/s Time-Interleaved Flash-SAR ADC Using Sharable MDAC

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Received April 5, 2014; Revised June 13, 2014; Accepted November 19, 2014; Published February 28, 2015

** Regular Paper*

***Abstract*:** This paper presents a 10-bit 10 MS/s Time-Interleaved Flash-SAR ADC with a shared Multiplying DAC. Using shared MDAC, the total capacitance in the SAR ADC decreased by 93.75%. The proposed ADC consumed 2.28mW under a 1.2V supply and achieved 9.679 bit ENOB performance. The ADC was implemented in 0.13μm CMOS technology. The chip area was 760 × 280 μm^2.

***Keywords*:** Time-Interleaved, Flash-SAR ADC, Multiplying DAC

1. Introduction

Among the many types of ADCs (Analog to Digital Converters), the SAR ADC is used widely because of its advantages of low power consumption and simplicity. However, an exponential increase in the capacitance with increasing resolution restricts the use of applications requiring high conversion speeds.

On the other hand, Flash ADC, having the highest conversion speed in many types of ADC, has great power consumption and chip area. Therefore, flash ADC is limited under 8 bit resolution.

Pipeline ADC can be a good alternative to use a fast conversion speed in a small area. However, because the op-amp based MDAC should be used at each stage, it requires a relatively large current.

Therefore, there has been some research on Time-Interleaving ADC, such as : Flash-SAR ADC [1, 2], pipelined-SAR ADC [3].

This paper presents a 10-bit 10MS/s Time-Interleaved Flash-SAR ADC architecture with the fast speed of a flash ADC and the low power of a SAR ADC. In addition, a Sharable Multiplying-DAC was added to remove the unnecessary increase in capacitance.

The remainder of this paper is organized as follows. Section 2 presents the architecture of the proposed Time-Interleaved Flash-SAR ADC. Section 3 presents a detailed description of the proposed building blocks. Section 4 shows the experimental results. The conclusions are reported in Section 5.

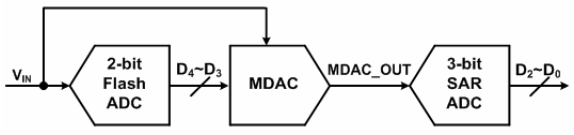
2. Time-Interleaved Flash-SAR ADC Architecture

Fig. 1(a) shows a conceptual block diagram of Flash-SAR ADC. In the Flash-SAR ADC architecture, the front-end flash ADC receives an analog input signal (V_{IN}) and decides the MSBs. Using these bits, MDAC conducts a residue process to make the input of the back-end SAR ADC. Finally, the remaining LSBs are achieved in SAR ADC.

Fig. 1(b) shows the operation of the ADC. Note that because $MDAC_{OUT}$ is amplified by a factor of 4 (in this example), the resolution of back-end SAR ADC can be decreased.

As shown in Fig. 1(c), the flash ADC uses only 1 clock cycle for its MSBs conversion and the SAR ADC can start its operation. Therefore, if only 1 channel SAR ADC is used, the front-end flash ADC does not work during the SAR ADC's successive process period.

Using a multi-channel SAR ADC with the time-interleaving method, the idle time of flash ADC can be removed and at every clock cycle, a new analog input (V_{IN}) can be processed in the flash ADC.



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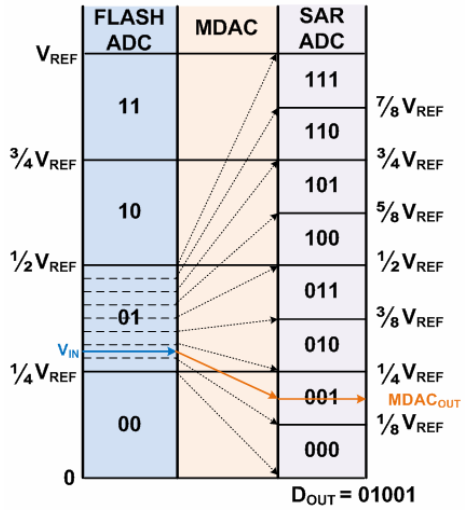

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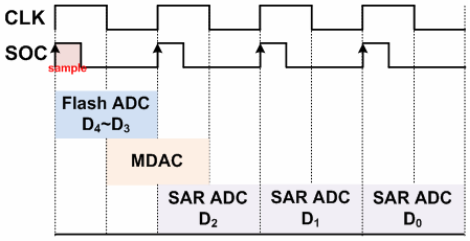


(c)

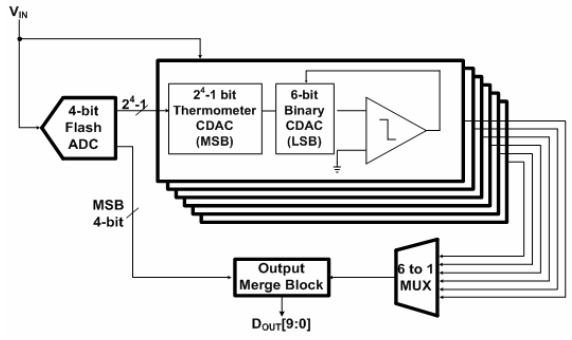
Fig. 1. (a) Conceptual Block Diagram of the Flash-SAR ADC (5-bit example), (b) Operation of the Flash-SAR ADC, (c) Timing diagram of Flash-SAR ADC.

On the other hand, using a multi-channel SAR ADC makes the architecture too bulky. Fig. 2(a) shows the 10-bit Time-Interleaved flash-SAR ADC combined 4-bit flash ADC with a 6 channel 10-bit SAR ADC using thermometer code.

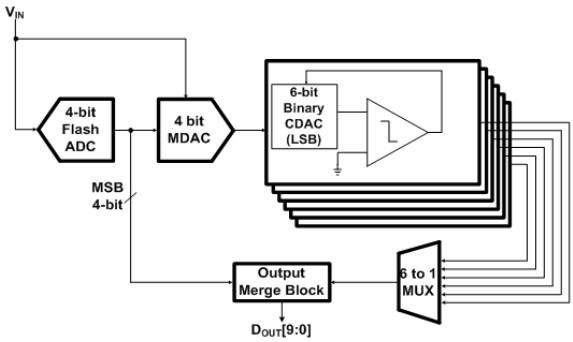
Although this architecture has the advantage of a faster conversion speed than the conventional SAR ADC, the total capacitance, dominant area of SAR ADC, increases 6 times compared to the conventional 10-bit SAR ADC.

On the other hand, the proposed 10-bit Time-Interleaved Flash SAR ADC has a sharable MDAC between 4-bit Flash ADC and 6-bit SAR ADC. By implementing the sharable MDAC, a 2^4-1 bit thermometer CDAC in the fine SAR ADC can be removed so that the size of the ADC can be decreased dramatically.

Table 1 lists the comparison results of the total capacitance of each ADC type. Compared to the conventional 10-bit flash-SAR ADC using the Thermometer CDAC [1, 2], the proposed flash-SAR ADC in this paper can reduce the total capacitance 2^4 times, which leads



(a)



(b)

Fig. 2. (a) Block diagram of the Time-Interleaved Flash-SAR ADC architecture using a thermometer CDAC, (b) Block diagram of the proposed Time-Interleaved Flash-SAR ADC Block Diagram.

Table 1. Total Capacitance of each ADC Type (@ 10 bit).

Type of ADC	Total Capacitance
10 Bit SAR ADC	2^{10} C
10 Bit Flash SAR ADC (4b flash + 6*10b SAR) (Thermometer CDAC) [1, 2]	2^{10} C × 6
10 Bit Flash SAR ADC (4b flash + 6*6b SAR) (Proposed)	2^6 C × 6

directly to the reduction of the total size of the circuit.

Moreover, to minimize the area and current consumption of the SAR ADC in each channel, a Dual-Sampling SAR ADC structure was adopted and Adaptive Power Control (APC) mode was added to the comparator of the SAR ADC.

Fig. 3 shows the timing diagram of the proposed 10-bit 10MS/s Time-Interleaved Flash-SAR ADC.

At a sample rate of 10MS/s, the duties of the Clock and Start of Conversion (SOC) signal were 50% and 25%, respectively, and the sampling frequency was 10MHz. When the SOC signal was high, the Sample & Hold circuit in the ADC samples the analog input signal V_{IN}. On the other hand, when the SOC signal is low, the Sample & Hold circuit maintains the sampled signal V_{IN}, and the Flash ADC and MDAC process the sampled signal V_{IN}.

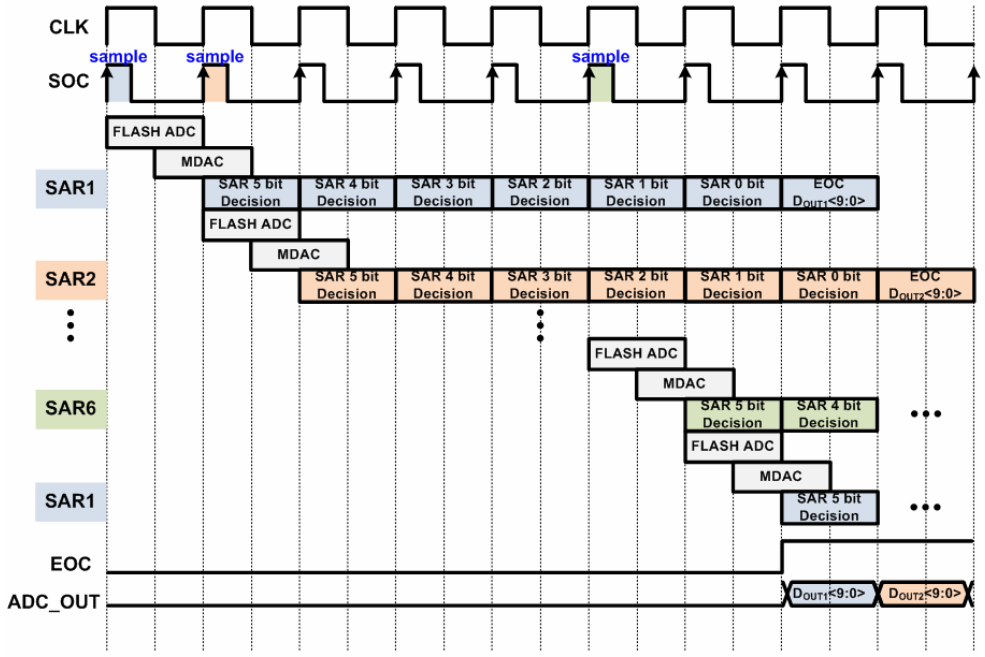


Fig. 3. Timing diagram of the proposed 10 bit 10MS/s Time Interleaved Flash-SAR ADC.

The front-end flash ADC decides 4-bit MSBs then these bits control the MDAC for the residue process. After the residue process, the back-end 6-bit SAR ADC can use the output voltage of the MDAC as the input voltage. Note that when the SAR ADC starts its MSB decision process using the previous one, the flash ADC samples the new input voltage simultaneously.

In this architecture, a 7 clock cycle latency exists. Therefore, the output code of flash ADC should maintain its value 6 clock cycles and merge the back-end SAR ADC output code. Therefore, flip-flops are designed as an output merge block. These flip-flops use the EOC (end of conversion) signal of each channel for triggering.

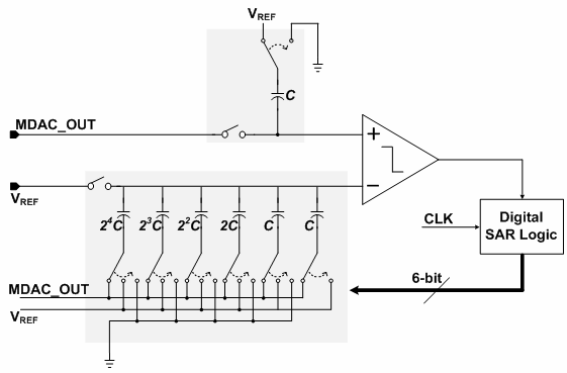


Fig. 4. Block Diagram of 6-bit SAR ADC.

3. Building Blocks

To reduce the chip area, the dual-sampling SAR ADC structure was implemented [4]. Fig. 4 shows a block diagram of the implemented SAR ADC. In general, a 6-bit SAR ADC requires 2^6 C for its binary searching algorithm. On the other hand, in this architecture, using a single sampling capacitor on the opposite side of CDAC, the total capacitance of SAR ADC is reduced to almost a half. Therefore, the area of 6-channel SAR ADC can be decreased.

In ADC, a comparator is one of the most important blocks because it greatly affects the accuracy and power consumption of ADC. Fig. 5 presents a schematic diagram of the comparator [5]. This is a combined structure of a preamplifier stage and dynamic latch stage. The use of a pre-amplifier at the input stage can reduce the effect of kickback noise. In addition, using the Adaptive Power Control (APC) function, the unnecessary power consumption can be reduced.

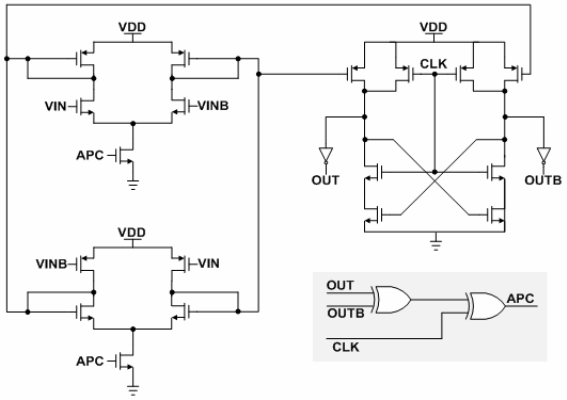
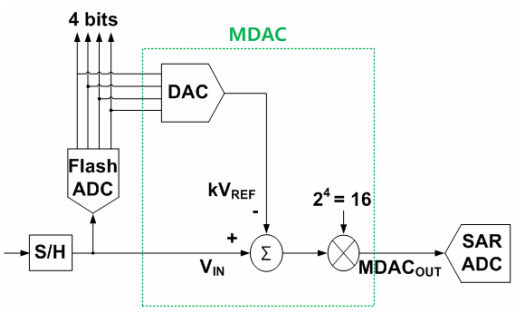
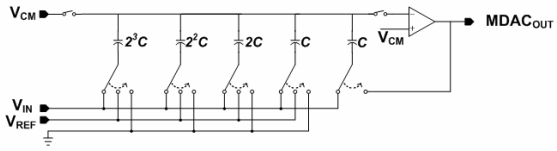


Fig. 5. Schematic of the Comparator in SAR ADC.

In this paper, a sharable MDAC was implemented to reduce the total capacitance in SAR ADC.



(a)



(b)

Fig. 6. (a) Residue Process in the MDAC, (b) Schematic diagram of the MDAC.

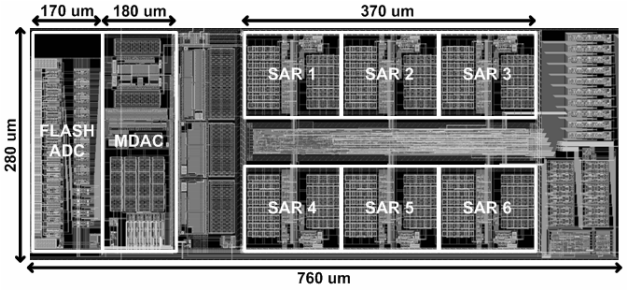
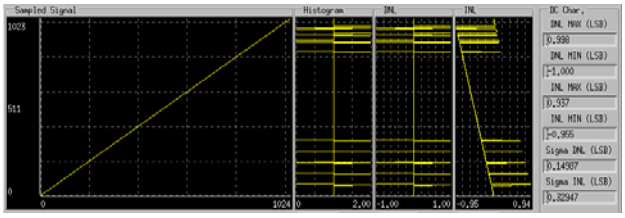
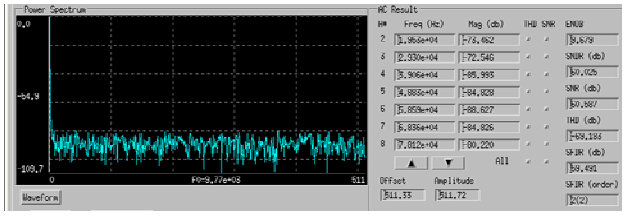


Fig. 7. Layout of the proposed architecture.



(a)



(b)

Fig. 8. (a) INL/DNL Results, (b) SNDR / ENOB Results.

Table 2. Performance Summary.

Process	0.13 um
Supply	1.2 V
Resolution	10 bits
Sampling rate	10 MS/s
Power	2.28 mW
DNL	-1.000 ~ 0.998 LSB
INL	-0.955 ~ 0.937 LSB
SNDR	60.025 dB
ENOB	9.679 bits
Core area	0.21 mm^2

Fig. 6(a) describes the residue process in MDAC. After flash ADC decides the 4-bit MSB codes, these codes can be used in MDAC. Using these MSBs, the coefficient k is decided from 0 to 15/16, and calculated with an analog input V_{IN}. Finally, by multiplying residue value by 2^4, the output of the MDAC is generated as follows:

$$MDAC_{OUT} = {}^{4}({}_{IN} - \cdot \quad) \tag{1}$$

After the $MDAC_{OUT}$ is made, it is delivered to the input of the 6 channel SAR ADC and used to determine the remaining LSB 6-bits.

4. Experimental Results

The proposed ADC designed with a 0.13 μm CMOS occupies 760 × 280 ㎛^{2} (Fig. 7). The size of the flash ADC, MDAC and SAR ADC is 170 × 280 ㎛^{2}, 180 × 280 ㎛^{2} and 370 × 280 ㎛^{2}, respectively.

Fig. 8(a) shows the simulation results of the differential nonlinearity (DNL) and integral nonlinearity (INL). The peak DNL and INL were -1.000/0.998 LSB and -0.955/0.937 LSB, respectively. Fig. 8(b) shows the FFT spectrum at a 10-MS/s sampling rate. The result of SNDR is 60.025 dB. The resulting ENOB is 9.679 bits. At a 1.2 V supply voltage, the proposed ADC consumes 2.28 mW. The figure-of-merit of the ADC was calculated using the following equation.

$$FOM = \frac{Power}{2^{ENOB} \times f_s} \tag{2}$$

The FOM of the proposed Time-Interleaved Flash-SAR ADC is a 278.14fJ/conversion-step.

5. Conclusion

A Time-Interleaved Flash SAR ADC using a sharable MDAC was presented. The proposed ADC architecture can lead to a faster conversion speed than the conventional SAR ADC and a smaller total capacitance than the other Time-Interleaving ADC architecture.

The proposed ADC achieves a 10MS/s operation speed with a power consumption of 2.28mW. In addition. it has a FOM of 278.14 fJ/conversion-step and occupies an active area of only 0.21 mm^2.

Acknowledgement

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2010114).

This work was supported by IDEC (IPC, EDA Tool, MPW).

References

[1] Ba Ro Saim Sung, Sang-Hyun Cho, Chang-Kyo Lee, Jong-In Kim, and Seung-Tak Ryu "A Time-Interleaved Flash-SAR Architecture for High Speed A/D Conversion." ISCAS 2009, Article (CrossRef Link)

[2] Ba Ro Saim Sung, Chang-Kyo Lee, Wan Kim, Jong-In Kim, Hyeok-Ki Hong, Ghil-geun Oh, Choong-Hoon Lee, Michael Choi, Ho-Jin Park, and Seung-Tak Ryu "A 6 bit 2 GS/s Flash-Assisted Time-Interleaved (FATI) SAR ADC with Background Offset Calibration." ASSCC 2013, Article (CrossRef Link)

[3] Lu Sun, Yuxiao Lu and Tingting Mo "A 300MHz 10b Time-Interleaved Pipelined-SAR ADC.", CARFIC 2013, Article (CrossRef Link)

[4] Binhee Kim, Long Yan, Jerald Yoo, Namjun Cho, and Hoi-Jun Yoo "An Energy-Efficient Dual Sampling SAR ADC with Reduced Capacitive DAC." ISCAS 2009, Article (CrossRef Link)

[5] Song Lan, Chao Yuan, Yvonne Y.H.Lam and Liter Siek "An Ultra Low-Power Rail-to-Rail Comparator for ADC Designs.", MWSCAS 2011, Article (CrossRef Link)

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