IEIE Transactions on Smart Processing and Computing, vol. 4, no. 1, February 2015
http://dx.doi.org/10.5573/IEIESPC.2015.4.1.051

Digital Error Correction for a 10-Bit Straightforward SAR ADC

Behnam Samadpoor Rikan, Hamed Abbasizadeh, Sung-Han Do, Dong-Soo Lee, and Kang-Yoon Lee

College of Information and Communication Engineering, Sungkyunkwan University / Suwon, South Korea
{behnam, hamed, dsh0308, blackIds, klee}@skku.edu

***** Corresponding Author: Kang-Yoon Lee

Received April 5, 2014; Revised June 13, 2014; Accepted November 19, 2014; Published February 28, 2015

** Regular Paper*

***Abstract*:** This paper proposes a 10-b SAR ADC. To increase the conversion speed and reduce the power consumption and area, redundant cycles were implemented digitally in a capacitor DAC. The capacitor DAC algorithm was straightforward switching, which included digital error correction steps. A prototype ADC was implemented in CMOS 0.18-μm technology. This structure consumed 140μW and achieved 59.4-dB SNDR at 1.25MS/s under a 1.8-V supply. The figure of merit (FOM) was 140fJ/conversion-step.

***Keywords*:** Redundancy, Digital error correction, Straightforward, SAR ADC

1. Introduction

High performance analog-to-digital conversion on the nanometer scale is performed according to the high speed switching rather than amplifying. The nature of a charge redistribution successive-approximation-register (SAR) analog-to-digital converter (ADC) is based on high speed switching. As the demand for low power consumption and high precision is increasing, the prominent power efficiency of this structure has made it popular for high resolution analog-to-digital conversion applications. Moreover, a verification of recent publications confirmed that the attitude toward SAR ADCs has increased rapidly.

While the low-power characteristics of SAR ADC has increased the applications of this structure, it suffers from low speed because for each conversion, a large number of decision cycles are required. The necessity and interest in high speed structures and low power consumption for SAR ADCs, has prompted many efforts to increase the speed of this block and overcome this drawback. In addition, many techniques have been used to further decrease the power consumption of these blocks [1].

Applying redundancy to the conversion steps is an alternative approach for SAR ADC design. A redundant structure has two benefits. First, a redundancy decision causes in built-in error resilience, in which a bounded decision error in the early steps can be absorbed into the redundant conversion ranges of the later steps. The settling accuracy in most MSB conversion steps of the DAC can largely be relaxed and the conversion speed can be expedited. Second, the redundancy allows overlapped conversion curves in parts of the ADC transfer function, which is instrumental to a digital domain treatment of DAC mismatch errors. In this paper for DAC settling error problem in binary decision SAR ADCs, a digital error correction (DEC) technique has been applied. The DEC technique leaves the capacitor intact and employs digital addition only [2].

The organization of this paper is as follows. Section 2 reviews the conventional structure and straightforward algorithms for SAR ADCs. Section 3 proposes the digital error correction technique used for the SAR ADC structure. A 10-bit prototype SAR ADC using digital error correction technique is implemented in section 4. Section 5 reports the simulation results and section 6 concludes the paper.

2. Conventional vs Straightforward SAR structures

Fig. 1 shows the block diagram of the SAR ADC. Input is sampled and held in the S&H sub-block. DAC is a capacitor array, in which according to the control bits from SAR logic, a voltage is created. The output voltage of the DAC is compared with the sampled input in a comparator. The SAR logic decides the control bits according to the

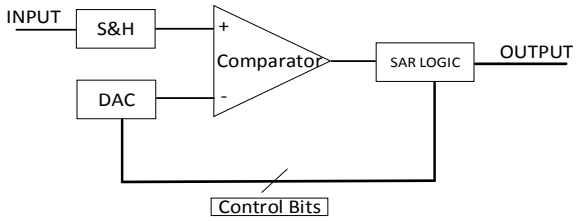


Fig. 1. Structure of SAR ADC.

comparator output in each cycle. The output of the ADC will be available after the decision of the N bit finished.

Fig. 2 summarizes the structure and switching sequence of a 3 bit dual sampling SAR ADC as an example. Initially, the input is sampled in C1, and CDAC is sampled to VREFT-VIN. At the hold step, the MSB is decided and according to the MSB bit, the SAR logic decides how to redistribute the charge in the next step.

If the MSB is 1, (1/2)VREFT is added to the CDAC voltage by connecting bottom plate of one half of the unit capacitors to VREFT. In this step (3/2)VREFT-VIN is compared with the VIN and the second bit is decided. In the case that MSB is 0, the CDAC voltage again boosts to 1.5VREFT-VIN, and the bottom plate of the sample capacitor (C1) is connected to the VREFT, which causes an increase in the input voltage at the positive input of the comparator to the VREFT+VIN.

For the third bit decision, the voltage in C1 will be unchanged and if the output of the comparator is 1, one more capacitor in the cap-bank will be connected to the VREFT, and if the output of the comparator is 0, one of the capacitors, in which bottom plate is connected to the VREFT, will go back to the VREFB. This structure is called dual sampling because the analog signals are sampled and held asymmetrically at each input side. In this structure, the MSB bit is decided with no switching so the power consumption of this structure will be lower than the conventional SAR ADCs. In addition, the number of unit capacitors in CDAC has been decreased to half compared to conventional structures. Here VREFT and VREFB are a substitution of VDD and VSS, respectively, because for some error correction reasons, the exact VDD and VSS values cannot be used. Therefore, VREFT, which is slightly lower than VDD, and VREFB, which is slightly higher than VSS, were used.

The reason that this structure is reviewed is to give the reader some insight into SAR ADC and switching sequence in a capacitor bank. Moreover, in most SAR logics the switching algorithm is to some extent similar to this structure. For more detailed information reader can refer to [3].

For each cycle, we need to charge or discharge some of the capacitors from VREFT to VREFB and vice versa, which requires a long time and consumes large amounts of energy. Moreover, according to these simulations, to achieve a high performance structure we need to increase the unit capacitor value. In addition, the amount of C1 needs to be several pF. When small values are used for this capacitor, the performance of the SAR ADC degrades.

The structure used for the proposed ADC is called straightforward DAC switching. This reduces the wasted power and increases the speed of switching. Note that a similar concept has been reported [4-6].

The positive input of the comparator is connected to the VCM which is created in the reference generator and there is no need to be sampled. The other inputs are connected to the CDAC.

Similar to the dual sampling structure, Fig. 3 summarizes the detailed switching sequence for the 3bit straightforward SAR ADC. At the sampling mode, the output of CDAC is charged to VCM-VIN and in hold

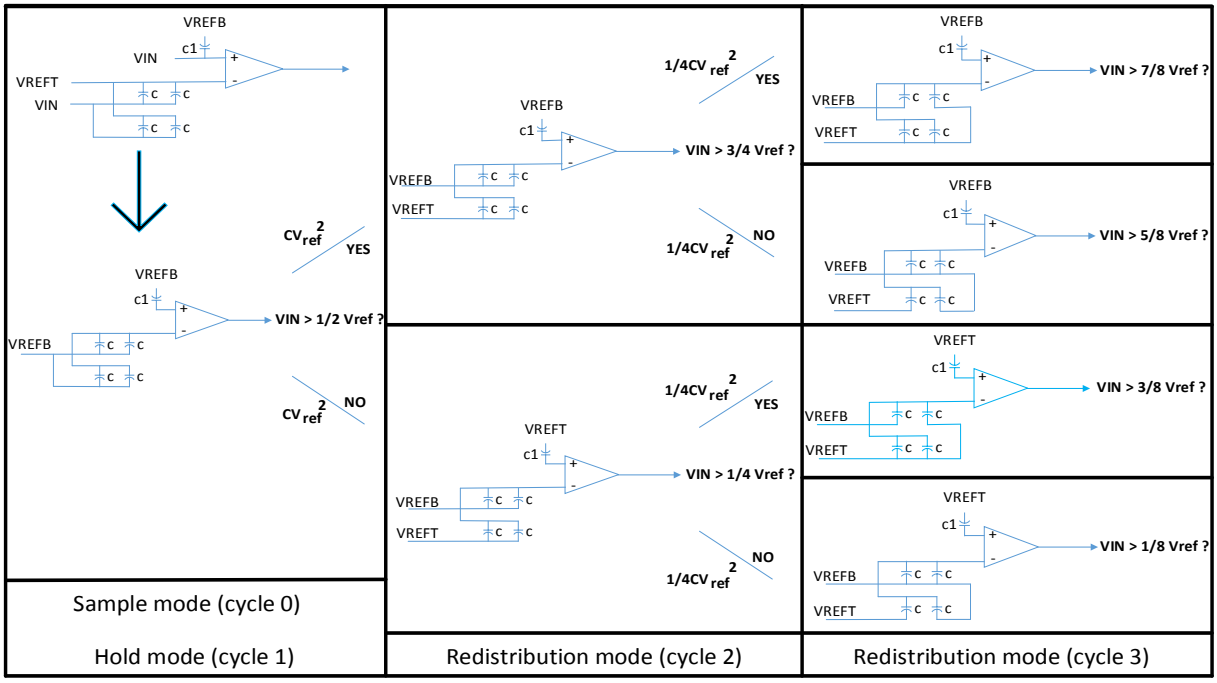


Fig. 2. 3 bit dual sampling switching sequence.

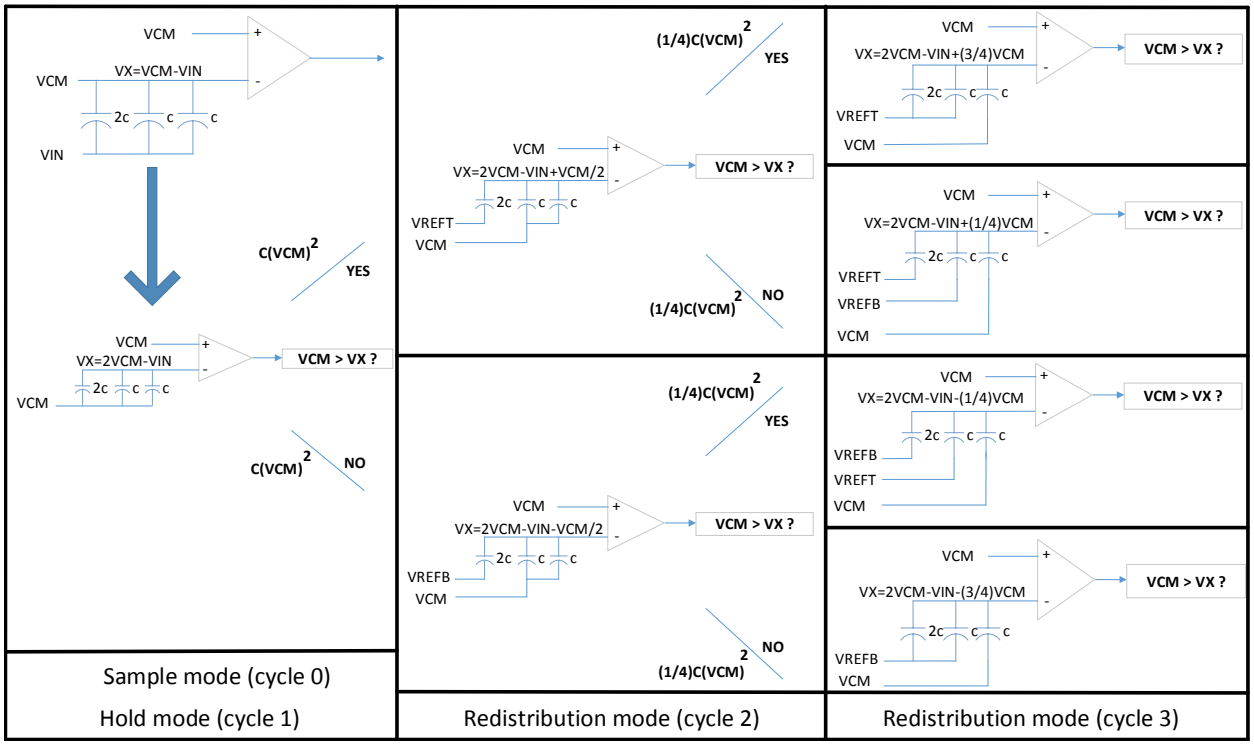


Fig. 3. 3 bit straightforward switching sequence.

mode it goes to 2VCM-VIN and can be compared with the VCM. According to the decision of the comparator, the bottom plate of 2C will connect to VREFT or VREFB at the next cycle. This will continue in the next steps as well. In each step, the switching is performed from VCM to VREFT or VREFB. Therefore, the amount of charge or discharge voltage decreases to half. Consequently, the amount of energy will be a quarter of the previous case. Moreover, the speed of the switching can be increased. Therefore, this structure is more energy efficient than the conventional structures and has a higher speed.

The bottom-plate sampling-based straightforward structure can be used for higher resolution as it provides better linearity in principle [7].

2. Digital error correction technique using redundant cycles

In high resolution ADCs, the difference between the coarse capacitor values and fine capacitor values normally causes decision errors in MSB bits. In particular, when the speed increases, the DAC is not settled properly in the decision phases for MSBs. This will cause error at MSB codes, which cannot be recovered in the following cycles. To solve this problem, some redundant cycles are normally predicted. Redundancy can be applied by adding some extra capacitors to the hardware and predicting some redundant decision cycles. Digital error correction was used to solve this problem. This does not require any extra hardware and the CDAC structure remains intact. The concept is explained for a 4 bit example, which has 4 bits and 5 decision cycles.

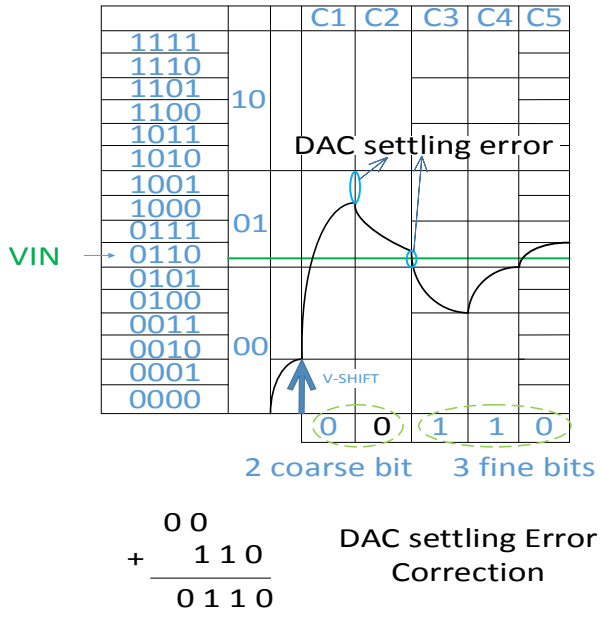


Fig. 4. DAC settling error correction concept using redundant cycle (C3).

As implemented in Fig. 4, the decision procedure in the SAR ADC was divided into two steps. The first step decides the 2 coarse bits and the second step is a decision of the 3 fine bits. One bit redundancy was predicted.

Coarse decision thresholds were at 6/16 and 10/16. The decision levels were shifted 0.5LSB of the coarse resolution here. Therefore, the MSB decision with the DAC level is started at 5/8 VREF instead of 1/2 VREF. In the example, the SAR ADC has a slow VDAC settling,

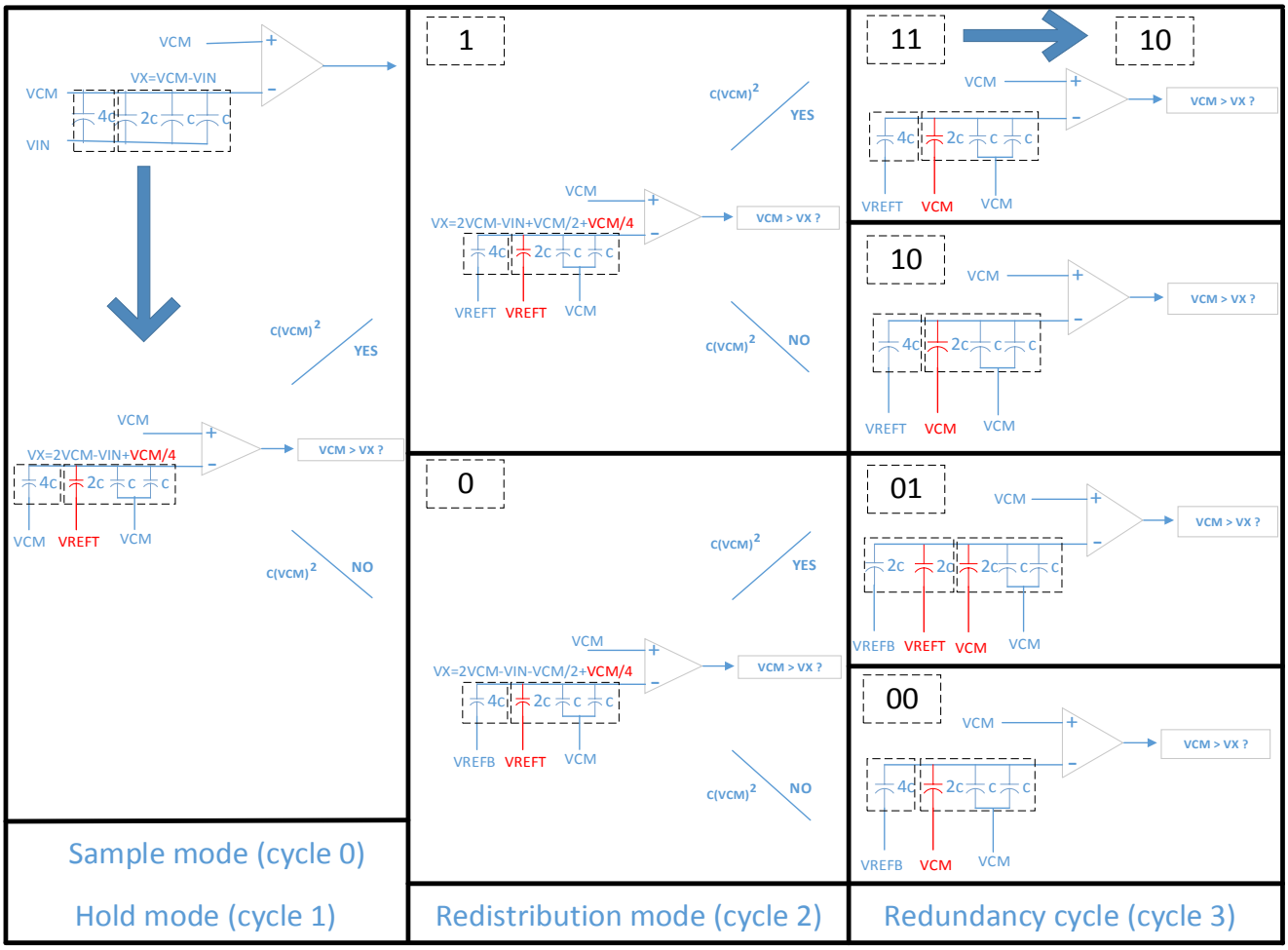


Fig. 5. Switching sequence with the error correction technique for 2 coarse and 1 redundancy bits in a 4 bit structure.

which results in decision error. For the given VIN, 00 is created for two MSB bits, which is not correct. The redundancy will be implemented by one additional decision step. To determine the three fine bits, the VDAC decision level will shift back to its regular decision level by 0.5LSB, shifting it down, which has been done at the beginning to determine the coarse bits. A redundant decision is then implemented. With two more decisions after this step, 3 LSB bits are determined. By adding two coarse bits and three fine bits with one bit overlap, the coarse bit error can be eliminated. As long as the error amount is less than 0.5LSB of the coarse resolution, the error can be eliminated. This will relax the DAC settling and the sampling decision speed can be increased, despite there being more conversion steps. A similar concept was implemented in [2, 7].

Fig. 5 presents the switching sequence for 2 coarse and 1 redundancy decisions. The switching sequence for 2 fine bits will be the same as the straightforward structure as explained before. This structure is the same as the straightforward structure and the redundancy has been implemented by only changing the decision levels.

The capacitor DAC has been segmented into two sub-DACs virtually. One of these sub-DACs decides the 2 coarse bits and the other one decides the 3 fine bits. After the input signal is sampled, except for the largest capacitor of second sub-DAC, all other capacitors are connected to VCM. 2C is connected to VREFT and implements the threshold offset (V-SHIFT) for digital error correction purposes. The MSB is decided in this step. According to the MSB bit value, the 4C capacitor is connected to VREFT or VREFB and the MSB-1 will be decided. As shown in Fig. 5, the CDAC switching operation for the redundant decision phase will be different for each case. In this step, for a further bit decision, the VDAC should be located at the center of determining the input range for the digital error correction algorithm. Moreover, 2C should go back to VCM for the next decision steps of the following LSB bits. In the case that MSB-1 bit is 0, these two conditions are satisfied by switching 2C back to the VCM. As shown in Fig. 6(a), by switching 2C to VCM, the determined input range will be double, and the VDAC will be located at the center of this range. The redundancy bit and 2 other fine bits will then be decided. The final bits can be obtained by adding 2MSB and 3LSB bits with a one bit overlap. As shown in Fig. 6(a), the error in MSB-1 bit has been corrected in the redundancy decision step safely.

In the case that two MSB bits are 01 (Fig. 6(b)), if 2C is switched to the VCM, the VDAC will not be in the center of the determined input range (it will be at the

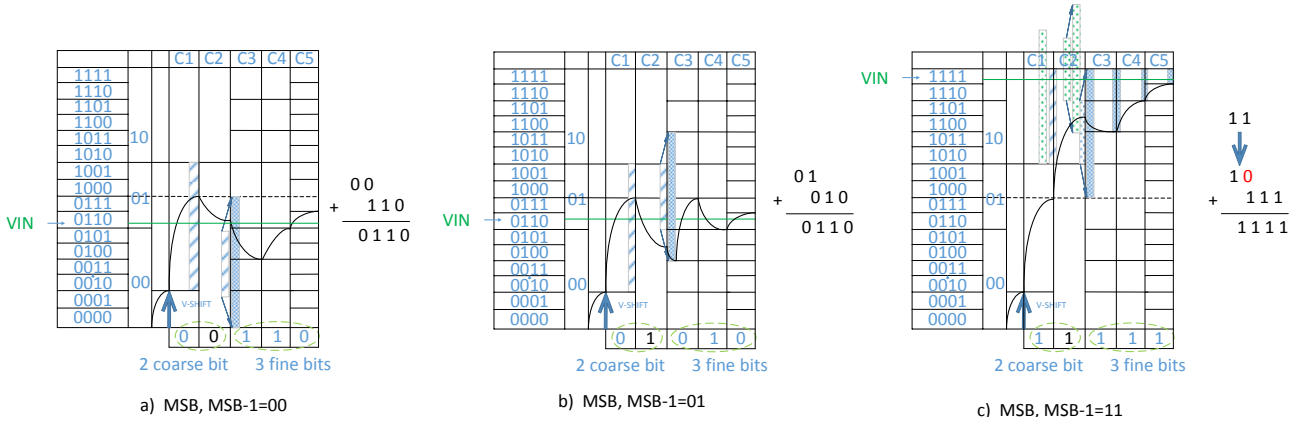


Fig. 6. Determined input ranges for different MSB and MSB-1 bits in a 4 bit digital error corrected SAR ADC.

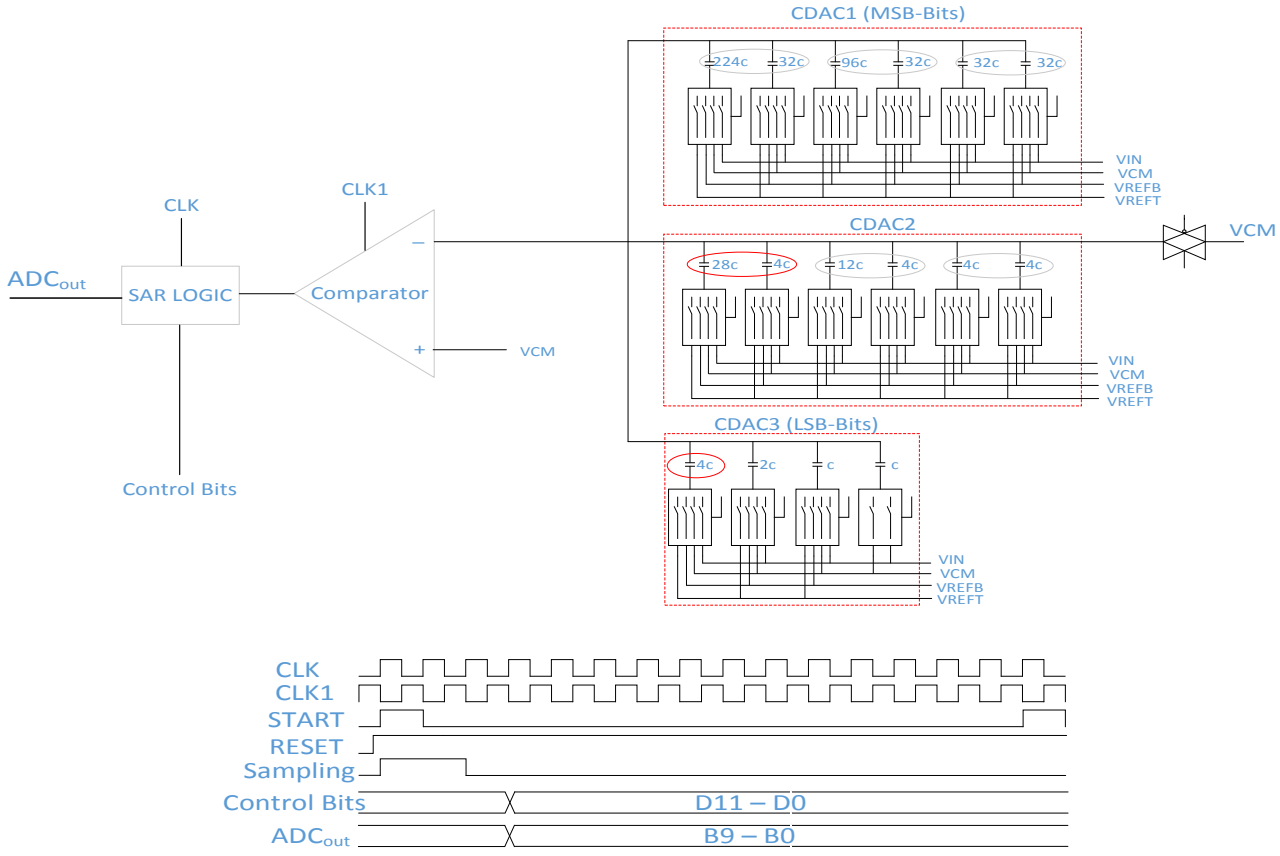


Fig. 7. 10-bit error corrected SAR ADC structure and timing diagram.

bottom of this range). On the other hand, for a further bit decision, 2C should return to the VCM. To solve this problem and satisfy the abovementioned conditions, as the required amount of VDAC change is double that of the returning 2C from VREFT to VCM, 4C was divided into two 2C capacitors and one of them was switched from VREFB to VREFT. Moreover, 2C in the lower sub-DAC was switched back to VCM. This moved the VDAC up to the desired level. The remainder of the decisions were identical to the previous case.

Finally, the last case is where all the MSB bits are 1. In this case, MSB capacitor was connected to VREFT, so the same procedure as the previous case cannot be followed. On the other hand, the MSB-1 bit can simply be changed to 0 and a similar operation can be performed, as done for the case when this bit was 0. The details for this case can be found in Fig. 6(c). For similar concepts, the reader can refer to [8].

In [8], during the redundancy cycle, if all the MSB bits of higher sub-DAC become 1, a problem occurs. In this case, in the redundant cycle, the MSB capacitor of the lower sub-DAC that is connected to VREFT should switch back to the VCM and at the same time, a capacitor with the same size in the higher sub-DAC that is connected to the VREFB should be found and switched to the VREFT. On the other hand, this is impossible because all the bits that have been decided by higher sub-DAC are 1, so all the capacitors of this sub-DAC are already connected to the

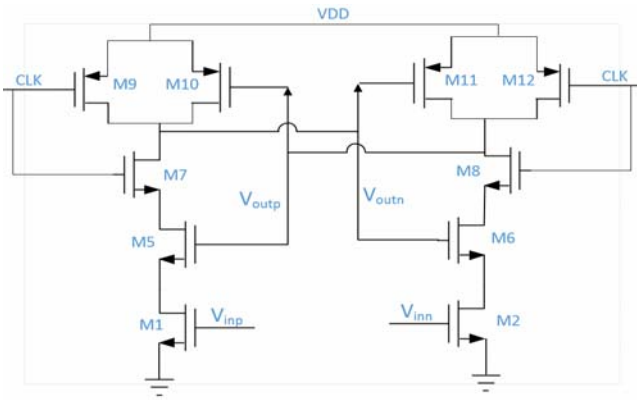


Fig. 8. Comparator structure.

VREFT. The proposed switching sequence of this paper solved this problem, as verified before. As shown in Fig. 5, the switching sequence for each case has been illustrated clearly and all the cases have been considered.

4. 10-bit prototype SAR ADC using digital error correction

The 10-bit SAR structure using the explained error correction technique has been implemented in Fig. 7. The capacitor weights are intact compared to the straightforward structure. The CDAC has been segmented into three sub-DACs virtually. Each sub-DAC creates 4bits. CDAC1, CDAC2 and CDAC3 create D11-D8, D7-D4 and D3-D0, respectively, in which D7 and D3 are decided in the redundant cycles. The largest capacitor in CDAC2 is 32C (28C+4C), so each capacitor of CDAC1 is broken into two capacitors, of which one of them is 32C. This is for the purpose of redundancy in the case that D8 is 1 and D11D10D9D8 bits are not 1111 (as explained in the previous section). Therefore, for this case, one of the 32C capacitors that is connected to the VREFB can be found and switched to the VREFT in the redundant cycle. For a similar reason, the capacitors of CDAC2 were broken into two parts, of which one of them was 4C as the largest capacitor in CDAC3 is 4C.

The reader might be concerned about the number of switches. Note that the number of switches has been increased but size of these switches has been decreased proportionally. Moreover, the unit capacitor size used in this structure is 29fF, which is the minimum capacitor size limited by the process. As the capacitor size is reduced, the speed can be increased and the power consumption and area can be decreased. Fig. 8 presents the comparator structure.

5. Simulation Results

Simulation results for proposed ADC structure are implemented in this section. Finesim was used for the simulations. The process was 0.18-µm CMOS technology.

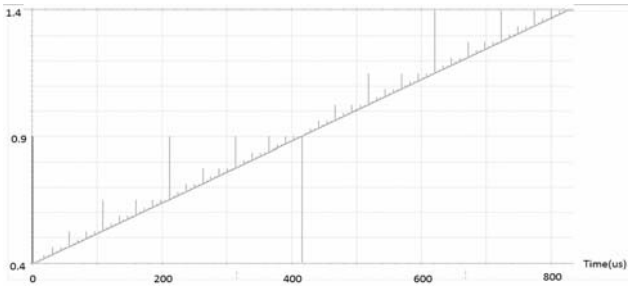


Fig. 9. Ramp Simulation Result.

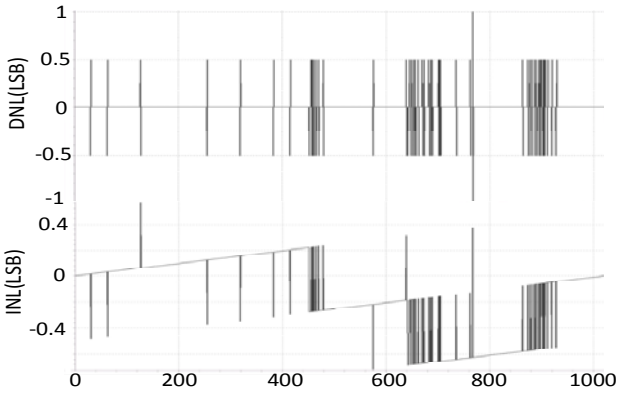


Fig. 10. DC Analysis Results.

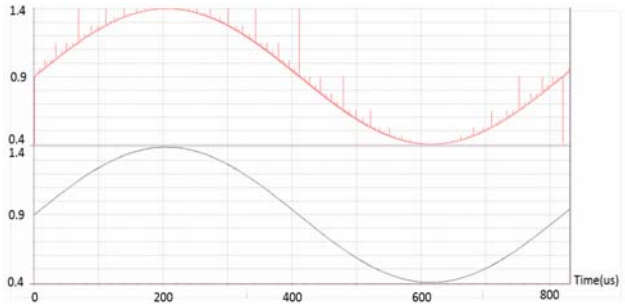


Fig. 11. Sine Simulation Result.

Fig. 9 shows the ramp simulation result for the proposed ADC. The sampling speed per cycle was 1.25MHz. The number of samples for this simulation was 1024.

Fig. 10 shows the DC analysis results for this ADC. The results were extracted from the ramp simulation. DNL max and DNL min were 0.998 and -1.0 LSB, respectively. INL max and INL min were 0.562 and -0.719 LSB, respectively, and Sigma DNL and Sigma INL for this structure were 0.155 and 0.294 LSB, respectively.

Fig. 11 presents a sine wave simulation. The input frequency for this simulation was 1.22KHz and the clock sampling was 1.25MHz. Fig. 12 presents the implementation of the FFT of the output. The input was a 62 KHz sine wave sampled at 1.25MHz. For this input frequency, the effective number of bits (ENOB) was 9.4. The SNDR and SNR were 58.3 and 60.2dB, respectively, and the amount of SFDR was 63.4dB. This ADC consumed approximately 80µA from 1.8V source. Therefore, the current consumption of this structure was

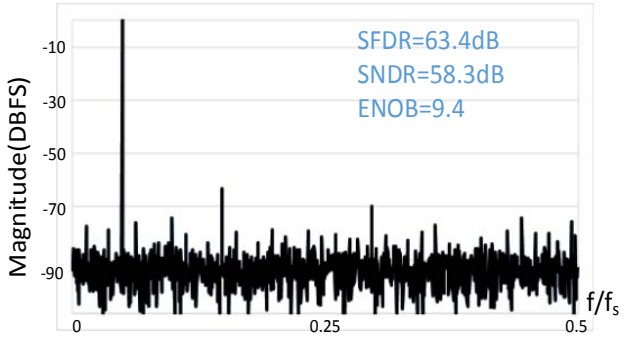


Fig. 12. Spectrum of the output samples for the input 62 KHz at 1.25MHz.

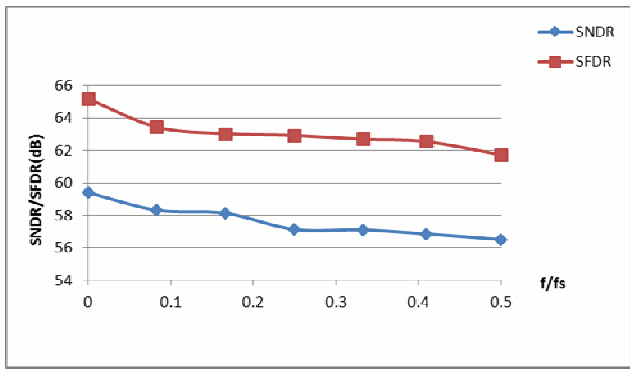


Fig. 13. SNDR and SFDR for the different input ranges from DC to Nyquist rate.

Table 1. Summary and comparison results.

Parameters	[9]	[10]	This work
Process(nm)	0.35	180	180
Resolution(bit)	10	10	10
Sampling Rate (MS/S)	2	0.137	1.25
Supply voltage	3.3	1.5	1.8
$ENOB_{Peak}$	8	8.65	9.57
$SNDR_{peak}$(dB)	-	53.8	59.4
$SFDR_{peak}$(dB)	-	-	65.2
Sigma DNL(LSB)	0.5	0.56	0.155
Sigma INL(LSB)	0.5	0.38	0.294
Power(mW)	3	13.4	0.14
FOM(fJ/Conv-step)	-	243	140

140μW. Fig. 13 illustrates the SNDR and SFDR for different input frequencies from DC to Nyquist rates.

$$FOM = \frac{Power}{2^{ENOB} \times \min\{2 \times ERBW, f_s\}} \quad (1)$$

According to (1), the figure of merit (FOM) was calculated to be 140fF. Finally, Table 1 summarizes and compares the work with recent studies in SAR ADC.

6. Conclusion

This paper proposed a 10 bit SAR ADC. A digital error correction was used for the straightforward structure. This ADC was implemented in CMOS 0.18-μm technology. The power consumption for this structure was 140μW under a 1.8-V supply. The structure had 59.4-dB SNDR, 61.3 SNR and 65.2 SFDR (peak values) for a 1.25MS/s conversion speed. The unit capacitor in the CDAC structure was 29fF. At this conversion speed, for all frequencies from DC to Nyquist rate, the ENOB was above 9 bits. The figure of merit (FOM) was 140fJ/conversion-step.

Acknowledgement

This study was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2010114).

This work was supported by IDEC (IPC, EDA Tool, MPW).

References

[1] W. Liuet, P. Huang and Y. Chiu, "A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter with Digital Calibration," *IEEE Journal of Solid-State Circuits*, VOL. 46, NO. 11, Nov. 2011. Article (CrossRef Link)

[2] S-H. Cho, C-K. Lee, J-K. Kwon and S-T. Ryu, "A 550-uW 10-b 40-MS/s SAR ADC with Multistep Addition-Only Digital Error Correction," *IEEE Journal of Solid-State Circuits*, VOL. 46, NO. 8, Aug. 2011. Article (CrossRef Link)

[3] B. Kim, L. Yan, J. Yoo, N. Cho and H-J Yoo, "An Energy-Efficient Dual Sampling SAR ADC with Reduced Capacitive DAC," *Circuits and Systems, ISCAS. IEEE International Symposium*, 2009. Article (CrossRef Link)

[4] V. Hariprasath, J. Guerber, S-H. Lee and U-K. Moon, "Merged capacitor switching based SAR ADC with highest switching energy-efficiency," *Electronic Letters*, 2010. Article (CrossRef Link)

[5] Y. Chen, S. Tsukamoto and T. Kuroda, "A 9b 100MS/s 1.46mW SAR ADC in 65nm CMOS," *IEEE Asian Solid-State Circuits Conference* pp. 16-18, Nov. 2009. Article (CrossRef Link)

[6] Y. Zhu, C-H. Chan, U-F. Chio, S-W. Sin, S-Pan U, R. P. Martins and F. Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, VOL. 45, NO. 6, Jun. 2010. Article (CrossRef Link)

[7] P. W. LI, M. J. Chin, P. R. Gray and R. Castello, "A Ratio-Independent Algorithmic Analog-to-Digital Conversion Technique," *IEEE Journal of Solid-State Circuits*, VOL. SC-19, NO.6, Dec. 1984. Article (CrossRef Link)

[8] S-H. Cho, C-K. Lee, J-K. Kwon, and S-T. Ryu, "A 550μW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction," *Custom Integrated Circuits Conference (CICC),* 2010. Article (CrossRef Link)

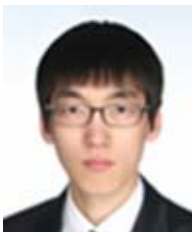
[9] C. Jun, R. Feng and Xu M. H., "IC Design of 2Ms/s 10-bit SAR ADC with Low Power," *High Density Packaging and Microsystem Integration,* 2007. Article (CrossRef Link)

[10] H-K. Kim, Y-J. Min, Y-H. Kim and S-W. Kim, "A Low Power Consumption 10-bit Rail-to-Rail SAR ADC Using a C-2C Capacitor Array," *Electron Devices and Solid-State Circuits (EDSSC), IEEE International Conference on,* 2008. Article (CrossRef Link)

behnam Samadpoor Rikan was born in Urmia, Iran, in 1983. He received his B.S. degree in Electronic Engineering from Urmia University, Urmia, Iran in 2008 and M.S. degree in Electronic Engineering from Qazvin Azad University, Qazvin, Iran in 2013, where he is currently working toward a Ph.D. degree in School of Information and Communication Engineering, Sungkyunkwan University, Suwon, Korea. His research interests include the design of high-performance data converters, bandgap reference voltage, low-dropout regulators and ultra-low power CMOS RF transceivers.

Hamed Abbasizadeh was born in Suq, Iran, in 1984. He received his B.S. degree in Electronic Engineering from Bushehr Azad University, Bushehr, Iran in 2008 and M.S. degree in Electronic Engineering from Qazvin Azad University, Qazvin, Iran in 2012, where he is currently working toward a Ph.D. degree in the School of Information and Communication Engineering, Sungkyunkwan University. His research interests include the design of high-performance data converters, bandgap reference voltage, low-dropout regulators and ultra-low power CMOS RF transceiver.

Sung-Han Do was born in Jinju, Korea, in 1988. He received his B.S. degree from the Department of Semiconductor Systems Engineering at Sungkyunkwan University, Suwon, Korea, in 2014. He is currently working toward a M.S. degree in Semiconductor Display Engineering at Sungkyunkwan University. His research interests include Analog to Digital Converter and Sensor Interfaces design.



Dong-Soo Lee was born in, Korea, in 1987. He received his B.S., and M.S. degree from the Department of Electronic Engineering at Konkuk University, Seoul, Korea, in 2012, and electronic engineering at Sungkyunkwan University, Suwon, Korea, in 2014, respectively. He is currently working toward a Ph.D. degree in electronic engineering at Sungkyunkwan University. His research interests include CMOS RF IC and Phase Locked Loop, Silicon Oscillator, and Sensor Interfaces design.

Kang-Yoon Lee was born in Jeongup, Korea, in 1972. He received his B.S., M.S. and Ph.D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea, in 1996, 1998, and 2003, respectively. From 2003 to 2005, he was with GCT Semiconductor Inc., San Jose, CA, where he was a Manager of the Analog Division and worked on the design of CMOS frequency synthesizer for CDMA/PCS/PDC and single-chip CMOS RF chip sets for W-CDMA, WLAN, and PHS. From 2005 to 2011, he was with the Department of Electronics Engineering, Konkuk University as an Associate Professor. Since 2012, he has been with School of Information and Communication Engineering, Sungkyunkwan University, where he is currently an Associate Professor. His research interests include implementation of power integrated circuits, CMOS RF transceiver, analog integrated circuits, and analog/digital mixed-mode VLSI system.