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A Single Inductor Dual Output Synchronous High Speed DC-DC Boost Converter using Type-III Compensation for Low Power Applications

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** Regular Paper*

** Extended from a Conference: Preliminary results of this paper were presented at the IEEE ISCIT2014.*

***Abstract*:** This paper presents a high speed synchronous single inductor dual output boost converter using Type-III compensation for power management in smart devices. Maintaining multiple outputs from a single inductor is becoming very important because of inductor the sizes. The uses of high switching frequency, inductor and capacitor sizes are reduced. Owing to synchronous rectification this kind of converter is suitable for SoC. The phase is controlled in time sharing manner for each output. The controller used here is Type-III, which ensures quick settling time and high stability. The outputs are stable within 58µs.The simulation results show that the proposed scheme achieves a better overall performance. The input voltage is 1.8V, switching frequency is 5MHz, and the inductor used is 600nH. The output voltages and powers are 2.6V& 3.3V and 147mW&, 230mW respectively.

***Keywords*:** DC converter, Switch mode power supplies, SIMO converters

1. Introduction

As the technology advances, the desire for small area devices is increasing. Power management is the heart of all electronic devices, which makes the other blocks alive by supplying proper voltage levels. DC-DC converters provide a regulated supply for the rest of the circuit including the DSP chip in portable devices, with a different output level from the unregulated input supply. Voltage regulation for SoC (System-on-Chip) applications is required to fulfil a variety of functions [2]. These are classified into two categories, linear regulators and switching regulators. Conventional power management techniques consume high power under static conditions, but switching regulators have high efficiency compared to conventional techniques. Linear regulators waste most of their energy in the form of heat, requiring extra heat sinks. On the other hand switching regulators or choppers, dissipate a negligible amount of power during conversion. Chopper circuit requires at least two switches, one switching source, control circuit, one energy storage element. The input voltage is chopped off at a specific frequency. As the switching frequency is increased the charge and discharge region of the inductor shrinks and demands very careful calculations, timing diagrams and circuit design to generate proper signals for gate drives. Power loss at the power stage increases roughly with $\sqrt{f_s}$ [4]. These include; conduction losses and switching losses. Switching speed of MOSFET devices is calculated by the time required to charge/discharge the gate capacitor. Therefore, parallel multiple MOSFET's can be used to achieve a high switching speed. Bootstrap, ø-inverters,3rd generation gate drive techniques [5, 6] are ideal candidates for switching the gate voltage at higher speed. In this paper, a small amount of efficiency is sacrificed to achieve high speed and lower volume. In addition, efficiency is an inverse function of the difference between the input and output voltages. Conventional dc-dc converters suffer power losses due to their bulky nature and require many inductors as outputs. The popular control scheme for

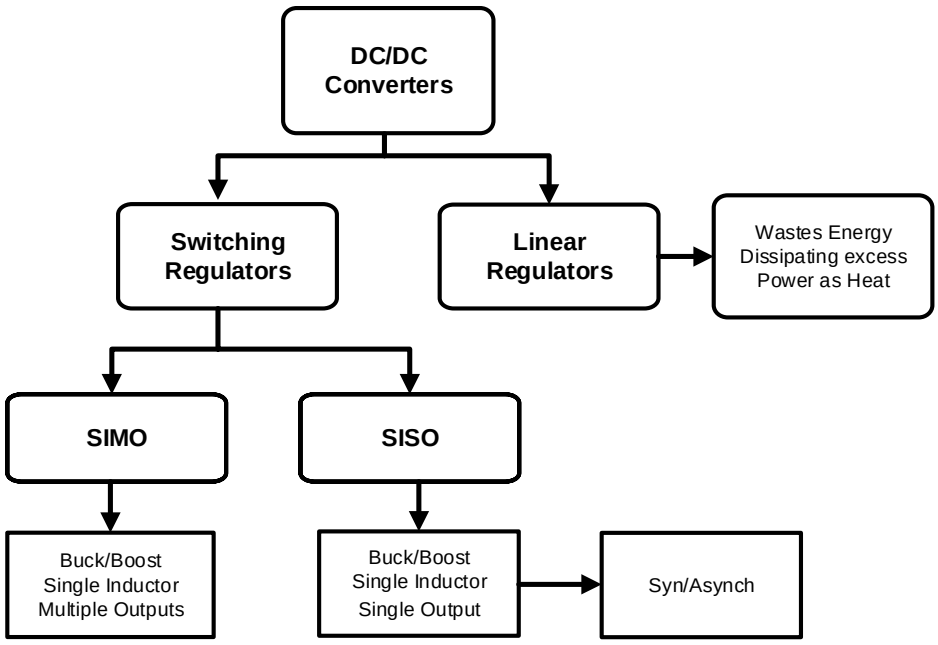

Fig. 1. Classification of DC-DC Converters.

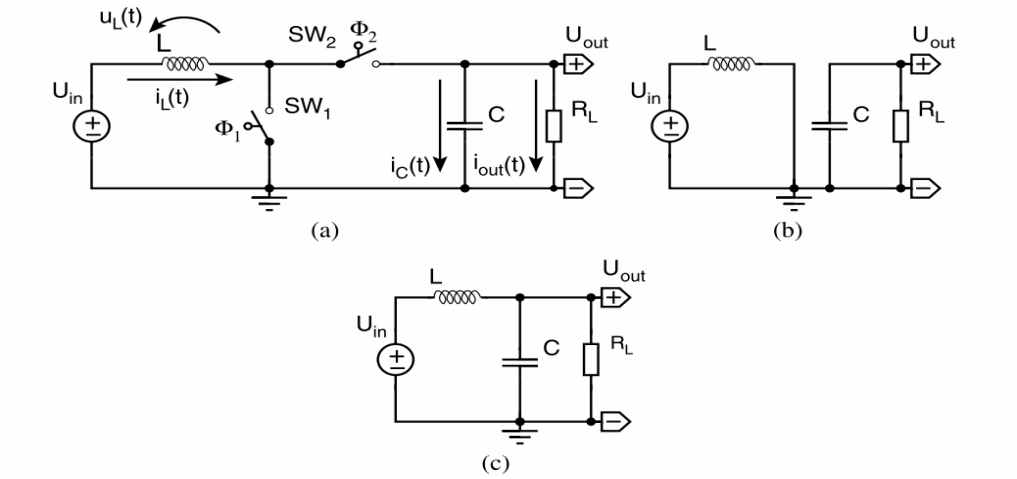

Fig. 2. (a) The circuit of an ideal boost DC-DC converter, (b) The equivalent circuit of the inductor charge phase, (c) the inductor discharge phase.

switching converters is pulse-width modulation (PWM). The control uses a constant switching frequency and varies the duty cycle as the load current varies. This scheme achieves good regulation, low noise spectrum, and high efficiency. A DC-DC converter, which is an essential block in PMIC (Power Management IC), provides a regulated output voltage from a linearly discharging battery in portable devices [7]. An LED driver is essentially a current source (or sink) that maintains a constant current required for achieving the desired color and luminous flux from an array of LEDs [8]. In the proposed converter design the inductor and capacitor sizes are reduced to 40% of the lowest average value published thus far. In addition a smooth handover block in the feedback loop was designed to assist the loop at start up and avoid indefinite unpredictable behavior.

2. Classification of Converters

Initially there are only two categories of dc-dc converters before the evolution of SIMO (Single Inductor Multiple Output) converters, linear regulators and switching regulators. Fig. 1 shows the classification of dc-dc converters according to the present times. Topologies in each category of switching regulators are divided into four classes: Buck Converter, Boost Convert, Inverting topology and transformer flyback topology. Inductor is charged at the first phase and energy of inductor with input supply is pushed to output node, just like fill and throw of energy to the output.

The inductor charge phase of a boost converter is shown in Fig. 2. The equivalent circuit for Φ1is shown in Fig. 2(b), which is simplified by closing SW1 and opening SW2 for a certain on-time ton. During Φ1 the inductor L is

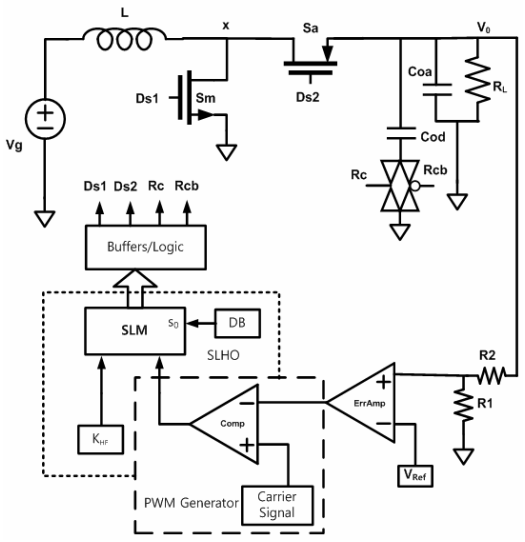

Fig. 3. Block Diagram of the Proposed Converter in [9].

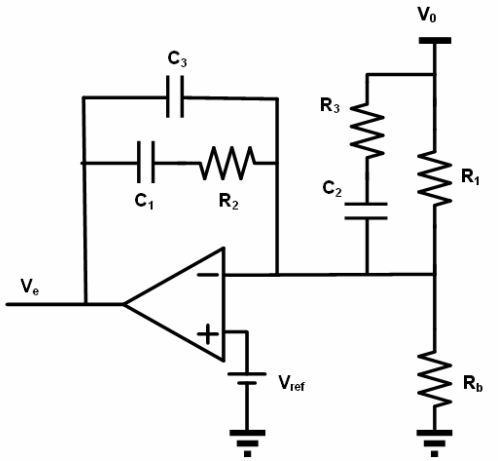

Fig. 4. Type-III Compensator.

charged by the voltage source Uin, causing the inductor current iL(t) to increase from its minimum value IL_min to its maximum value IL_max. Simultaneously the output capacitor C is discharged through the load RL. For the inductor discharge phase Φ2 , equivalent circuit is shown in Fig. 2(c), which is accomplished by opening SW1 and closing SW2 for a certainoff-time toff . During L is discharged into C and RL, causing iL(t) to decrease. As a result iL(t) is divided over C and RL, thereby charging C and providing power to RL. Because L is discharged in series with Uin it can be intuitively seen that the output voltage Uout will always be higher than Uin [9]

3. Related Work

The initial work with a single output has already been presented in our previous work [10] and [11]. A 3.7V High speed dc-dc synchronous boost converter with smooth loop handover is discussed. Switching frequency was 5MHz, inductor size was 600nH. Output of 3.7V is regulated from a supply of 1.8V. The three main blocks of dc-dc converter has been discussed. In the feedback loop PWM control is used. On the other hand in [11] we used Type-III compensation for single output converter to achieve quick settling time. In both papers the dual output with Type-III was not addressed.

In the architecture shown in Fig. 3 has three main blocks: Power stage, Control stage, and Gate drive stage. The control stage has further two sub-blocks: PWM generation and SLHO (Smooth Loop Hand Over). The current circulation in the power stage is much higher than the control stage. Output voltage is sensed scaled and compensated using error amplifier. It is compared with carrier signal to generate a PWM signal proportional to the output voltage. PWM signal generated from feedback loop and constant duty cycle signal are fed to Smooth Loop Mux (SLM). In the startup K_{HF} is engaged, while after the predetermined time which is set in DB (Delay Block) the PWM loop is engaged for the rest of the operation. Delay Block is triggered just after 20µs from power on of the converter. Simultaneously while depending on the load the C_{od} is connected and disconnected at the output using the control signals R_c and R_{cb} to reduce the ripples. D_{s1} and D_{s2} are two non-overlapped signals generated to avoid any loss or conflict in inductor current. This architecture works with CCM (continuous conduction mode) operation. S_m and S_a are used with anti parallel diodes, as MOSFET channel has to carry the positive current, e.g., n-channel MOSFET's drain to source. If the load is an inductive, interval that switch is turned on, current flows in the opposite direction, but this current will flow through the diode. Without a diode, the induced current generates peaks of high voltage, causing current to stop. At heavy loads conduction losses dominate while switching losses dominate at light loads. We used four stages of cascaded inverters as gate drives [10].

4. Control Techniques and Efficiency Model

There are many control techniques and compensation methods which are being used in dc/dc converters. Some of them are: Hysteretic, PI, Type-II and Type-III, with combination of voltage mode and current mode sensors. Peak inductor current and average current of inductor is acquired and monitored to make it as input for controllers. In the meantime feed-forward control also can be used for dynamic performance of the dc/dc converter. But in our case we used PI control technique.

Conventional PWM techniques have already been discussed in our previous work. But due to slow response time we re-designed our converter with Type-III controller. This controller is comparatively fast. Type-III compensation is used to improve the transient response, and to boost the crossover frequency and phase margin. It guarantees the targeted bandwidth and phase margin, as well as an unconditionally stable control loop [12]. Fig. 4 shows the conventional Type III compensation using voltage Op-Amp. Simulation results from discussed work of single inductor single output (SISO) is shown in Fig. 5.

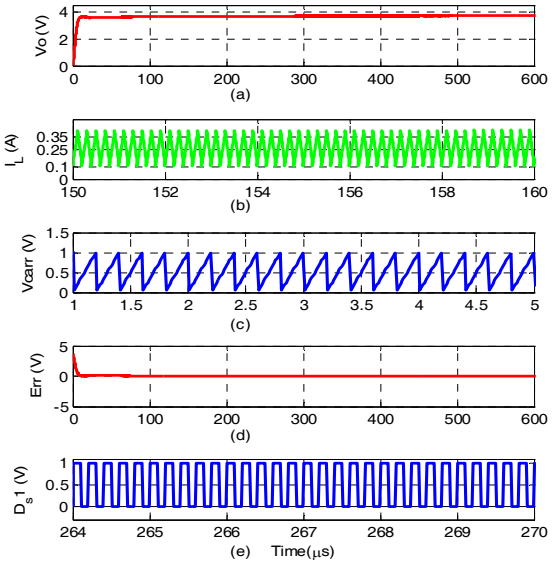

Fig. 5. Simulations Results of SISO.

There are two poles (f_{p1} and f_{p2}, besides the pole-at-zero f_{p0}) and two zeros (f_{z1} and f_{z2}) provided by this compensation. All passive components involved play a dual role in determining the poles and zeros. So, the calculation can become fairly cumbersome and iterative. But a valid simplifying assumption that can be made is that C_1 is much greater than C_3 [13]. So the locations of the poles and zeros are finally:

Transfer function with the feedback block is

$$f_{p0} = 1/[2\pi \times R_1(C_1 + C_3)] \approx 1/[2\pi \times R_1 C_1],$$
$$f_{p1} = 1/[2\pi \times R_3 C_2], f_{p2} = 1/\left[2\pi \times R_2\left(\frac{C_1 C_3}{C_1} + C_3\right)\right]$$
$$= 1/2\pi \times R_2(1/C_1 + 1/C_3)$$
$$\approx 1/(2\pi \times R_2 C_3)$$
$$f_{z1} = 1/[2\pi \times (R[_1 + R_3)C_2 f_{z2} = 1/[2\pi \times R_2 C_1] \quad (1)$$

$$\eta = P_o/(P_o + P_c + P_s) = \left\{1 + \frac{R_Y I_o}{V_o} + \frac{R_Z}{V_o I_o}\frac{\Delta I_L^2}{12} + \left[\frac{1}{2}\left(M + \frac{\Delta I_L}{2I_o}\right)(t_{rv} + t_{fl}) + \frac{V_o}{I_o}(C_{GN} + C_{GP} + C_X)\right] f_s\right\}^{-1} \quad (2)$$

where R_Y and R_Z are obtained using (7) and (8)

$$R_Y = R_L M^2 + R_{DSP} M + (R_C + R_{DSN} M)(M - 1) \quad (3)$$

$$R_Z = R_L + R_{DSN}\frac{M-1}{M} + \frac{R_{DSP} + R_C}{M} \quad (4)$$

P_o : Output power

P_c, P_s : Conduction and Switching losses

t_{rv} : Rise time

t_{fl} : Fall time

C_{GN} : NMOS gate capacitance

C_{GP} : PMOS gate capacitance

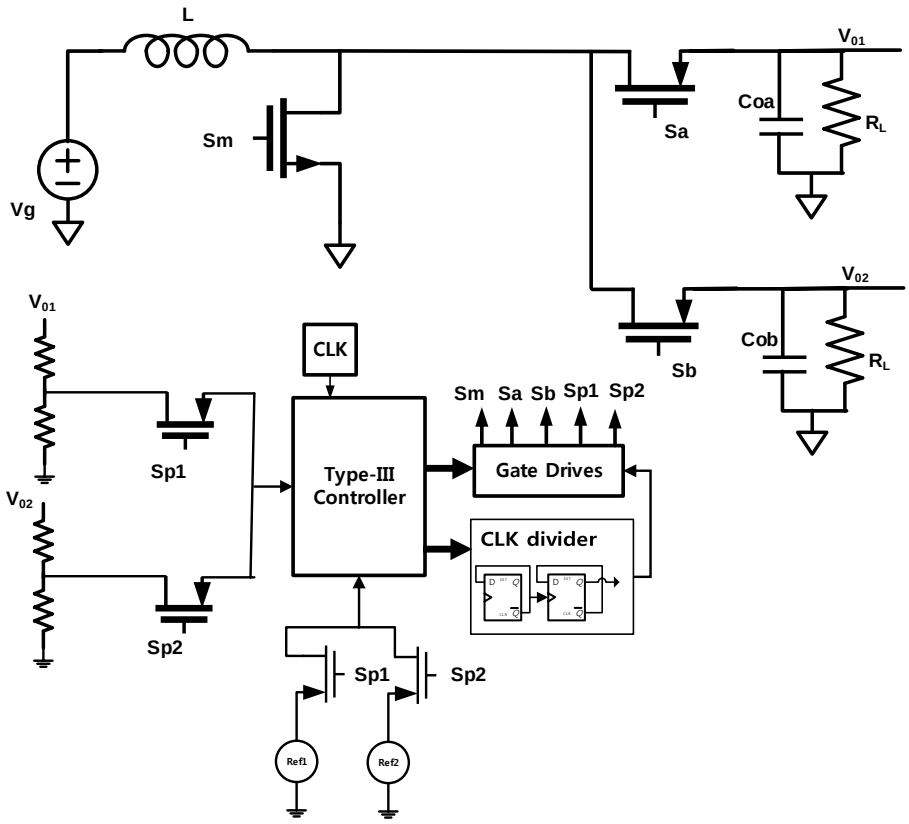

Fig. 6. Block diagram of proposed SIDO converter.

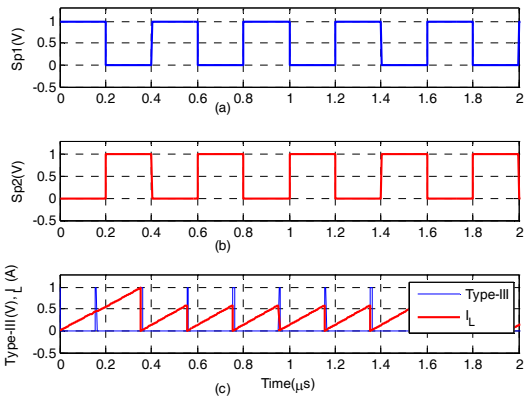

Fig. 7. Phase Control Signals and Type-III output.

C_X : Equivalent parasitic capacitance at node X

R_L, R_C : Equivalent series resistances of the inductor and capacitor respectively

5. Proposed Dual Output Architecture

In our design of proposed dual output converter as shown in Fig. 6, the inductor energy is shared between the two outputs. Dual output with phase control is presented in paper [1] with lower switching frequency, current sensors and high inductor value. In contrast we designed with high switching frequency, Type-III controller, lower inductor value, low load capacitor and without current sensors. Because current sensors occupy extra areas. Type-III controllers show a rapid response. To comply with higher switching frequency improved controllers are necessary. During phase 1output vo1 is maintained with coordination of Sm and Sa. In the meantime controller enables sp1 thus by selecting Ref1. On the other hand output vo2 is maintained with coordination of Sm and Sb. Charging time of Sm is decided by the controller depending upon the present output voltage at vo2. In this phase Ref2 is selected. Rate of charging inductor is same for both outputs with Vg/L, while discharge slope for phase1 is (Vg-Vo1)/L and for phase2 is (Vg-V02)/L. Filtering capacitors Coa and Cob smoothes the output glitches.

The overall controller output is shown in Fig. 7(c). Comparison with other works is summarizes in Table 1. For the time duration when sp1 is on, MOSFET S_m duty ratio is calculated to generate output required for the Vo1, similarly, when sp2 is on MOSFET S_m duty ratio is calculated to stable the output Vo2. At a time one sensor value is selected using sp1 and sp2. When sp1 is selected, reference voltage Ref1 becomes input to Type-III controller. In contrast when sp2 is selected Ref2 becomes the input for the controller. Each output is scaled and becomes input to Type-III controller where error signal is generated after subtracted from reference signals.

This error signal becomes input to comparator and

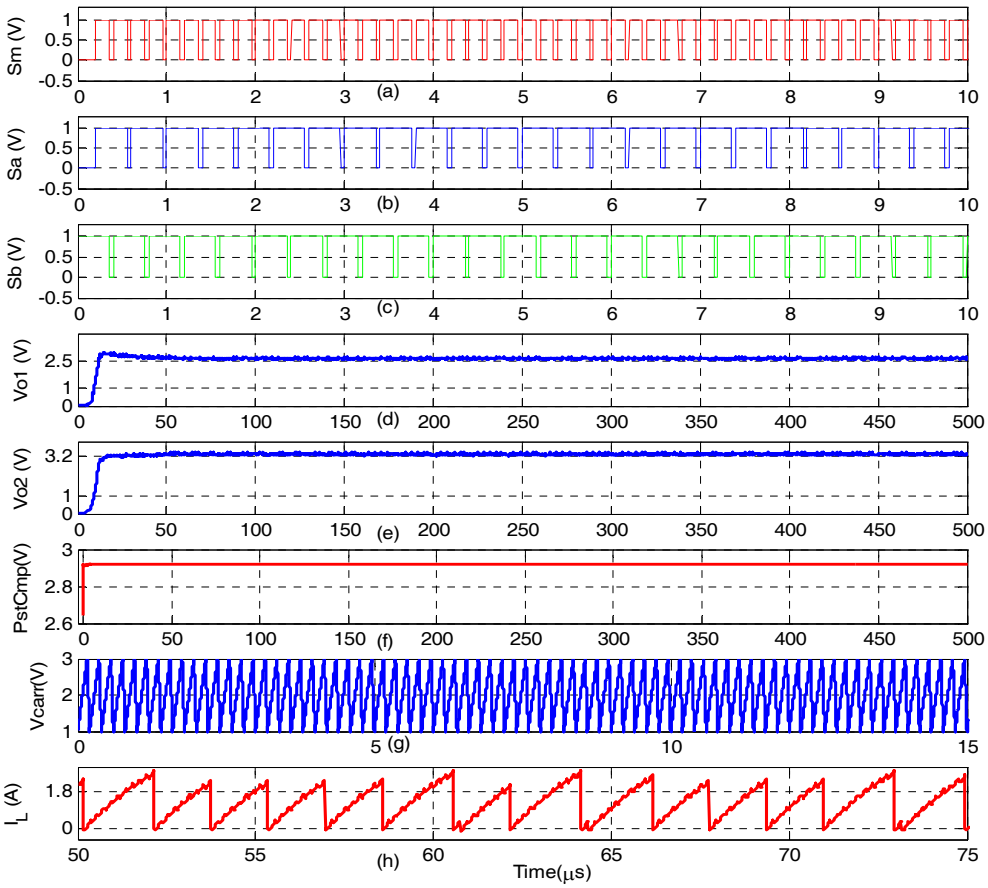

Fig. 8. Simulation Results of proposed Converter.

Table 1. Comparison Summary.

Parameters	Unit	[1]	[3]	[This Work]
Switching frequency	**Hz**	**500K**	**1M**	**5M**
Input voltage	V	1.8	2.6-5	1.8
Inductor	Henry	1μH	22μH	600nH
Output Voltages	V	3.0, 3.45	1.2	2.6, 3.3
Filtering Capacitors	Farad	44μ,47μ	35μ	1μ, 1μ
Compensation	-	-	-	Type-III
Settling time	Sec	-	-	58μs
Current sensors	-	Yes	No	No
Output power	W	150m, 170m	240m	147m, 230m

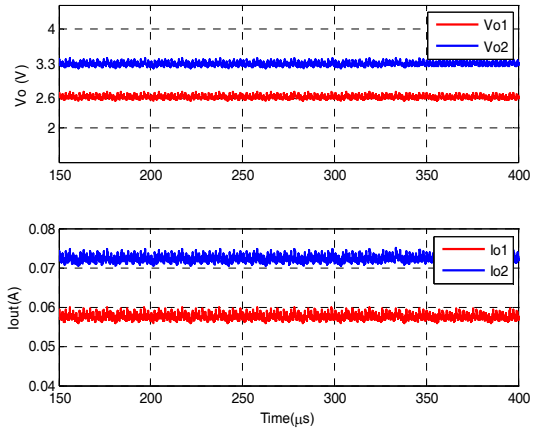

Fig. 9. Output Voltages and Load Currents.

from dead time control non overlapped signals are generated. Gate driver is used to generate high current and to turn and off the Power MOSFETs. We used existing clock for switching frequency using clock divider 2.5MHz is achieved through feedback of D-Flip-Flop to drive sp1 and sp2. The simulation results are shown in Figs. 8(a)-(h). NMOS signal S_m generated is shown in Fig. 8(a), Signal S_a, S_b are fed to high side PMOS switches located near the output Vo1 and Vo2 respectively. Boosted Output voltages are presented in Figs. 8(d) and (e), where output voltage level stables within 58μs. Comparator input is given in Fig. 8(f). Carrier signal and inductor current are illustrated in Figs. 8(g) and (h). Zoomed output voltages and load currents are shown in Fig. 9 for the same load resistors connected in both outputs. Average load current taken by Vo1 and Vo2 was 56mA and 70mA respectively.

6. Conclusion

This paper proposed a single inductor dual output dc-dc converter design using a Type-III compensation. In the beginning the existing single output and dual output architectures were discussed. The design was then formulated towards a dual output dc-dc converter with an improved control scheme, which is essential for high speed converters, ultimately reducing inductor and capacitor sizes. Settling time is 58μs. The Output voltage was scaled and fed to the controller in phase control mode. In each phase, the two phase control signals keeps track for adjusting the duty ratios to achieve the desired output.

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