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A 12-bit Hybrid Digital Pulse Width Modulator

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Abstract In this paper, a 12-bit high resolution, power and area efficiency hybrid digital pulse width modulator (DPWM) with process and temperature (PT) calibration has been proposed for digital controlled DC-DC converters. The hybrid structure of DPWM combines a 6-bit differential tapped delay line ring-mux digital-to-time converter (DTC) schema and a 6-bit counter-comparator DTC schema, resulting in a power and area saving solution. Furthermore, since the 6-bit differential delay line ring oscillator serves as the clock to the high 6-bit counter-comparator DTC, a high frequency clock is eliminated, and the power is significantly saved. In order to have a simple delay cell and flexible delay time controllability, a voltage controlled inverter is adopted to build the deferential delay cell, which allows fine-tuning of the delay time. The PT calibration circuit is composed of process and temperature monitors, two 2-bit flash ADCs and a lookup table. The monitor circuits sense the PT (Process and Temperature) variations, and the flash ADC converts the data into a digital code. The complete circuits design has been verified under different corners of CMOS 0.18um process technology node.

Key Words : DC/DC converter, PT calibration, Digital PWM. ADC

1. 서 론

Digital control implemented in switching power converter is receiving increasing attention [1]-[5]. It offers additional advantages in system energy management such as improved flexibility and increased functionality compared to an analog design. Programmable compensator and protection features make it possible to design a single controller that handles a range of power stage parameters such as L and C values and system configuration specifications such as current limits. Advanced digital algorithm and computation unit that is capable of self- diagnose, estimation and auto calibrations optimizes the system performance without external components and I/Os. Sophisticated digital programming also enables online monitoring and communications between different controllers and system management. Plus the digital design is easily migrated to different processes and upgraded or combined with other systems. Available DSP or micro- controllers, together with ADC (Analog- to-Digital Converter) and DAC (Digital-to- Analog Converter) can do the job of digital control. However, this approach has dis- advantages such as significant cost, area, and power overhead. Therefore, a customized low power digital controller DC-DC controller is

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becoming more popular and realistic solution for SoC.

The basic concept of digital controlled DC-DC converter is illustrated in Fig. 1, taking a Buck converter as an example [1]. First, the voltage difference between V_{fb} (output feedback voltage) and V_{ref} (bandgap reference voltage) is quantized by a high resolution ADC, and a digital error signal e[n] is generated. Then the error signal e[n] is processed by a digital computing unit, which may include digital compensator, protection function and other control algorism, and a duty ratio d[n] outputs to the DPWM. DPWM is actually a high resolution digital to time converter (DTC), which generates a pulse signal with its width modulated by the d[n] at fixed frequency. Finally, the pulsed is used to control the on/off state of the power switches in order to regulate the output to a targeted value.

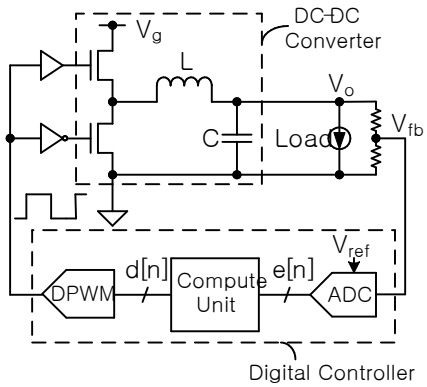

Fig. 1 Conventional digital DC-DC converter architecture

With the detailed structure analysis of digital controlled DC-DC converter, one can tell that its major disadvantage is that the performance is limited by the realistic resolution of ADC and DPWM. Meanwhile, the resolution of DPWM should always be higher than that of the ADC to prevent an unstable state called limit-cycle [2]. Therefore, a high resolution DPWM is always demanded in such systems. Reference [3] runs simulation on the output precision versus the resolution of ADC and the resolution of DPWM. The result shows that the optimum precision is reached when the DPWM is 12-bits, and the ADC is approximately 11-bits. Beyond this resolution, the output ripple becomes the limiting factor of the output accuracy.

This paper presents an effective design of a 12-bit hybrid DPWM that incorporates a low 6-bit differential tapped delay line ring-mux (DTC) with process and temperature calibra- tion and a high-resolution 6-bit counter- comparator DTC. Usually the delay line DTC excels in its low power but occupies more silicon area. On the other hand, the counter based DTC utilizes 2^n times faster clock to realize n-bit DTC, which imposes design stress on the high speed clock and excessive power consumption. The proposed hybrid structure combines the advantageous of the two methods and significantly counteracts their drawbacks, which makes it a promising choice.

For the proposed architecture, a voltage controlled differential inverter delay cell is proposed in this paper. The differential structure can save as much as 37.5% area [3]. The proposed voltage controlled inverter is economic in size and convenience in fine- tuning of the delay time for its additional voltage control node. Furthermore, process and temperature calibration circuit are proposed to address the delay time dependency on process and temperature variation. The overall design is completed on 0.18um technology node.

2. Hybrid Differential DPWM

The conventional hybrid DPWM is analyzed in Ref. [1] and [2]. A tapped delay line and a digital counter together with comparator are used to build the structure. This structure smartly combines the existing small size counter-comparator DPWM and low power tapped delay-line ring-mux DPWM.

Reference [3] improves the conventional structure by employing differential delay line cells to further reduce the area. Reference [3] utilizes the delay-line ring oscillator frequency as the clock of the counter so that a high frequency clock generation circuit is saved. However, the structure proposed in Ref. [3] suffers two major problems. One is that its delay cell is an analog differential amplifier with common feedback loop, which causes its delay cell to be much larger than the conventional digital delay cell. The other one is that the delay line is usually highly dependent on the process and temperature, which results that the switching frequency will vary as the process and temperature change. To overcome these problems, a novel 12-bit DPWM with process and temperature calibration is proposed in this paper as shown in Fig. 2. Eight 1X cells and three 4X cells are connected into a ring oscillator frame. The low 3-bit [L0-L7] and middle 3-bit [M0-M7] are tapped out as denoted in Fig. 2. The relationship of the low 6-bit signals is shown in Fig. 3 (a), where T_d is the oscillation period of the delay line. The rising edge sequence is from L7 to L0 and M0 to M7. For the final DPWM pulse, the Low 3-bit determines the starting edge of the pulse and the high six bits [H6-H11] determines how many T_d is following, and the middle three bits determine the falling edge of the pulse. The total period is $2^6 \times T_d$ as illustrated in Fig. 3 (b). The differential tapped delay line ring oscillator is composed of 8 1X delay cells and three 4X delay cells. A control voltage called V_c can adjust all the cells' delay time.

The control voltage is generated by the PT calibration circuit, which works as following. First, the PT monitor circuits keep monitoring the process and temperature variations and output an analog output. The output is converted to digital code by two 2-bits flash ADC. Combining the information of process and temperature variations, an appropriate voltage is selected through a loop-up table. The detailed circuits are given in the following section.

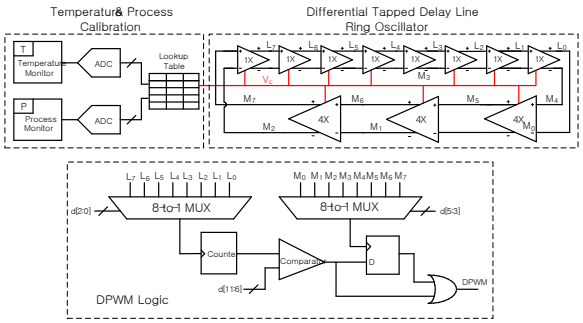

Fig. 2 Proposed 12-bit hybrid DPWM with process and temperature calibration.

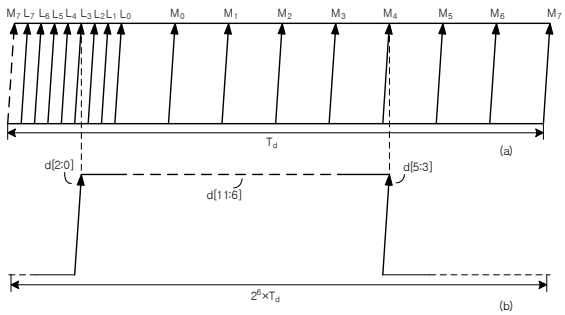

Fig. 3 Time chart of the proposed DPWM

3. Circuit Implementation

3.1 Differential Delay Cell

The detailed structure of 1X cell in Fig. 2 is revealed in Fig. 4 (a). It is composed of two voltage controlled inverter delay elements in parallel and two minimum sized inverters connected head to tail between the outputs of two delay element, which are to ensure the opposite phase of the differential output. The delay element, as shown in Fig. 4 (b), is constructed by a voltage controlled inverter and a gain boost inverter, which provides sharper transient edges, and a full digital output swing for the delay element. The voltage-controlled inverter has an additional NMOS transistor M_c in the pull-down of

the inverter controlled by a global control voltage V_c. Equation 1 gives the delay time. Besides the W/L ratio of the transistors, the delay time is also inversely proportional to the square of V_c, giving a flexible factor for fine tuning of the delay time.

$$t_p = \frac{1}{2}(t_{pLH} + t_{pHL}) = \frac{C_L}{2}\left(\frac{1}{k_p V_{DD}} + \frac{V_{DD}}{k_n V_c^2}\right) \quad (1)$$

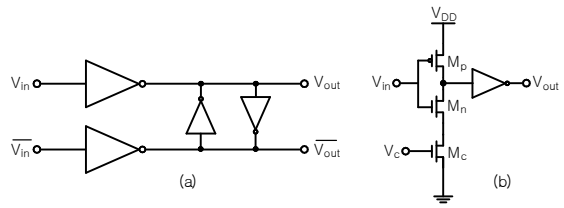

Fig. 4 (a) Differential delay cell (b) Voltage controlled delay element.

3.2 Differential Delay Cell

For temperature monitor, it is necessary to design an effective circuit is process insensitive and linear to temperature. Although Ref. [8] proposed a temperature monitor circuit, it works in sub-threshold region, which is not reliable in the real implementation. A traditional PTAT (proportional to absolute temperature) current generator [7] together with buffer output can meet the temperature monitoring requirements as illustrated in Fig. 5. The start-up circuit is used to prevent the PTAT circuit from the zero current state.

Once the circuit is activated, transistor Ms is off and isolates the start-up circuit from the PTAT current generation circuit. For the PTAT current generation part, Mp1-Mp2 and Mn1-Mn2 are identical pairs and formed in the current mirror frame, thus the current in two branches is equal. I1=I2. Thus the source voltages of Mn1 and Mn2 are approximately the same. The voltage across R1 is calculated as

$$V_{R_2} = V_{BE1} - V_{BE2} = V_T \ln n \quad (2)$$

where n is the size ratio of Q2 to Q1, and VT is the thermal voltage, given by

$$V_T = \frac{K \times T}{q} \quad (3)$$

where k is the Boltzmann's constant, T is the absolute temperature, and q is the electron charge. Io is the mirrored current and has the same value as I1 and I2. Therefore, the output voltage can be expressed as Equation 4

$$V_{out} = V_{ref} - \frac{R_2}{R_1} V_T \ln n \quad (4)$$

where Vref is a 1V bias voltage. R1 and R2 cancel each other's temperature effect. Vout is inversely proportional to the absolute temperature. The simulation results are summarized in Table 1. The output voltage differs a lot as temperature changing but only with little process variation. The 2-bit flash ADC described in next sub-section will encode three cases of temperature output.

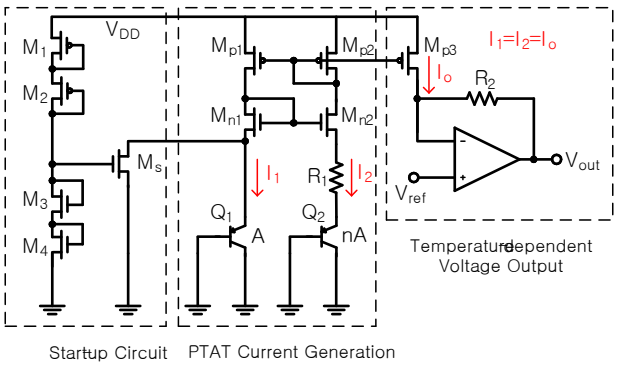

Fig. 5 Temperature monitor circuit.

Table 1 Temperature monitor circuit simulation results

Temp.	Vout (ff)	Vout (tt)	Vout(ss)	T_1T_0
-40°C	769 mV	775 mV	780 mV	11
25°C	693 mV	700 mV	706 mV	10
125°C	575 mV	585 mV	593 mV	01

3.3 Process Monitor

Reference [8] also proposed a process monitor circuit. However, it's still designed for sub-threshold operation, which is not reliable in the real implementation. The proposed process monitor circuit is illustrated in Fig. 6. It is composed of start-up circuit, PTAT current generation circuit, and a process dependent output. The start-up circuit and PTAT current generator are the same as the ones shown in Fig. 5. The output voltage equals the gate source voltage of M5 plus the voltage drop between R2 as written in Eqn. 5. M5 has the same dimension as the ones used in the differential delay line. The VGS has a negative temperature coefficient and the voltage across R2 provides a positive temperature coefficient. Choosing suitable R2/R1, it is possible to make the overall temperature coefficient zero at room temperature. Vout will be affected by the large threshold-voltage variation in different process corner since V_{GS} is highly related to the threshold voltage V_{th}. The simulation results are summarized in Table 2. The Vout changes about

$$V_{out} = V_{GS(M5)} + \frac{R_2}{R_1} V_T \ln n \quad (5)$$

$$\frac{\partial V_{out}}{\partial T} = \frac{\partial V_{GS}}{\partial T} + \frac{R_2}{R_1} \times \frac{K}{q} \times \ln n = 0 @ 25^{\circ}\mathrm{C} \quad (6)$$

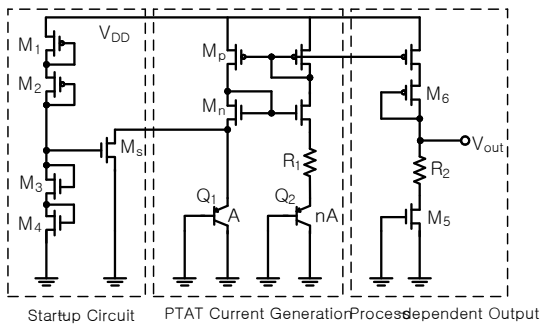

Fig. 6 Process monitor circuit.

100mV at different process corner, but only varies less than 15mV across the whole temperature range.

Table 2 Process monitor circuit simulation results

Corner	Vout (-40°C)	Vout (25°C)	Vout (125°C)	P_1P_0
ss	800 mV	802 mV	815 mV	11
tt	704 mV	700 mV	705 mV	10
ff	625 mV	619 mV	621 mV	01

3.4 Look-up Table

Both the process and the temperature will affect the delay time at the same time. Table 3 lists all possible combination of PT variations. A look-up table circuit is designed to select different output

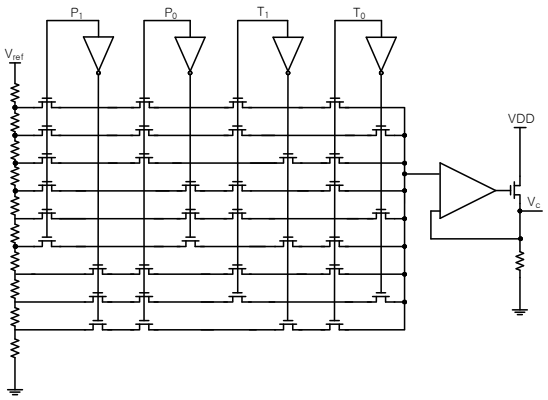

Fig. 7 Look-up Table for the PT calibration voltage output.

Table 3 All the possible combinatin of PT variations

Process Corner			Temperature			Control Voltage
ss	tt	ff	-40°C	25°C	125°C	
11			11			620 mV
11				10		610 mV
11					01	602 mV
	10		11			510 mV
	10			10		500 mV
	10				01	480 mV
		01	11			400 mV
		01		10		385 mV
		01			01	370 mV

according to the PT output code as shown in Fig. 8. A driving stage is added to drive the large delay line output load.

4. Conclusion

This paper proposed a power and area efficient architecture of 12-bit hybrid DPWM with process and temperature calibration. It is constructed by 6-bit differential tapped delay line ring-mux DTC and 6-bit counter- comparator DTC. Although the basic delay element for the delay line is investigated presented as an effective design in Ref. [6], a voltage-controlled inverter is adopted as our choice considering its controllable delay time plus small in size. Furthermore, it can be easily configured into differential mode. With the additional phase provided by differential mode, the area of the 6-bit delay-line cell is significantly reduced, which in turn power reduction as well. To overcome the common problems of process and temperature variation of most delay cells, a process and temperature monitoring and self-calibration circuits are proposed and analyzed in the paper along with he simulation results. The process monitor output is insensitive to temperature variation and temperature monitor is insensitive to process variation. The output of each monitor is combined and encoded to determine the appropriate control voltage to the voltage controlled inverter delay cell. Using this proposed approach, it became possible to control the delay time of each cell or the frequency of the ring-oscillator delay line accurately. All the circuits are implemented on 0.18um process node, and simulation results have verified all the design successfully.

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