Maximum Efficiency Operation of Three-Level T-type Inverter for Low-Voltage and Low-Power Home Appliances

Seung-Min Shin*, Jung-Hoon Ahn* and Byoung-Kuk Lee[†]

Abstract – This paper proposes a maximum efficiency operation strategy for three-level T-type inverter in entire operation areas. The three-level T-type inverter has higher and lower efficiency areas compared with two-level inverter. The proposed strategy aims to operate in the maximum efficiency point for the low-voltage and low-power home appliances. The three-level T-type inverter is analyzed in detail, and the two operation mode selection strategy is developed. The proposed algorithm is verified by theoretical analysis and experimental results.

Keywords: Three-level inverter, T-type inverter, Maximum efficiency operation, Low-voltage home appliance

1. Introduction

Voltage source inverters are widely used in many applications, such as industrial systems and home appliances, to achieve energy conservation and to improve high motion control quality. Especially, the two-level inverter to drive a multi-pole permanent magnet synchronous motor is a general choice for modern home appliances and industrial systems [1, 2]. In recent years, the low-voltage applications with 270V~600V DC link voltage for home appliances is continually increased and for higher efficient energy conversion and low cost, the micro-control unit and the power electronics technology are advanced [3].

A two-level voltage source inverter is commonly used for home appliances and industrial systems since its configuration is simple and the reliability is sufficiently ensured. However, there is a limit to improve the two-level inverter efficiency and performance because two-level inverter output voltage is decided by $\pm V_{DC}/2$. Furthermore, the inverter efficiency and performance are varied according to the switching method. In the case of the six-step modulation, the switching loss can be reduced, but the copper loss and torque ripple are increased because of the low frequency harmonics. The pulse width modulation method (PWM) is commonly used to solve the harmonic problem of this six-step method in many applications. PWM methods can be reduced the copper loss and the torque ripple compared with six-step method since PWM method switching frequency is higher than six-step method, but the switching loss becomes increased. The switching loss is more prominent when the switching frequency is increased and the DC link voltage becomes higher [4]. Therefore, in order to overcome these limitations of the

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two-level inverter efficiency and performance, a three-level inverter is being researched in various applications for further improvement of energy efficiency, reliability, power and density [5].

The multi-level topology such as the three-level inverter has been developed to drive medium-voltage level (DC link voltage: 600V~2500V) and high-voltage level (DC link voltage: 2500V~) since a semiconductor voltage blocking capability in conjunction is limited. Furthermore, it is verified that the multi-level topology offered a superior harmonic spectrum, lower overvoltage stress at cable and end windings of motors, lower common-mode voltage and lower switching loss [6]. Among various well-established multi-level topologies, the neutral-point clamped inverter (NPCI), flying capacitor inverter (FCI), and cascaded Hbridge inverter (CHBI) have been widely used and investigated as shown in Fig. 1 [7-14]. For these topologies, the switching loss in each switch is half and the conduction losses become double of the counterpart of the two-level inverter due to the two switch series connection. Therefore, these three-level inverter topologies are not suitable for low-voltage and low-power applications. To overcome these characteristics in the multi-level topology, the three-level T-type inverter (3LTI) has been proposed for

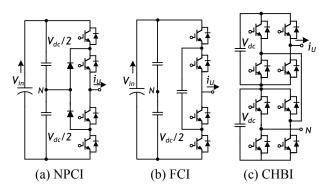


Fig. 1. Conventional multi-level inverter topologies

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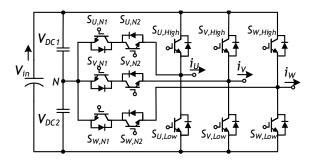


Fig. 2. Circuit configuration of three-level T-type inverter

the high efficiency and performance in low-voltage applications [15].

Even though the 3LTI is generally evaluated and investigated to apply in low-voltage industrial systems [16, 17], it has difficulties to apply in low-voltage and low-power home appliances such as refrigerators and air conditioners because the increased efficiency is not sufficient due to its complexity and cost problem. More accurately, since the utilization rate of switches is varied according to the modulation index (MI), the 3LTI has together higher and lower efficiency points. Therefore, in this paper, the maximum efficiency operation strategy for the 3LTI in entire operation areas is proposed. With the proposed strategy, the 3LTI is always operated in the maximum efficiency point in low-voltage and low-power applications. The proposed strategy is theoretically explained in detail and its validity is verified by experiment results.

2. General Characteristics of Three-Level **T-type Inverters**

2.1 Operational principle

Basically, the output bridge can be connected one of three states:

- 1) $S_{X, High}$ is turn-on
 - It is connected to positive DC link voltage level
 - The output voltage is $V_{DC}/2$
- 2) $S_{X, N1}$ or $S_{X, N2}$ is turn-on
 - It is connected to neutral voltage level
 - The output voltage is 0
- 3) $S_{X, Low}$ is turn-on
 - It is connected to negative DC link voltage level
 - The output voltage is $-V_{DC}/2$

The 3LTI is implemented by comparing the reference voltage with two triangular waves which are corresponding to the high-side capacitor voltage (V_{DC1}) and low-side capacitor voltage (V_{DC2}). During the period of the positive reference, S_{X, High} and S_{X, N1} are operated complementary through the relationship between the reference voltage and the triangular wave corresponding to V_{DC1} , and $S_{X N2}$ is kept on-state in order to guarantee the current path

through the anti-parallel diode of S_{X, N1}. Therefore, it is possible to control the phase voltage in the period of the positive reference. On the contrary, during the period of the negative reference, $S_{X, Low}$ and $S_{X, N2}$ are operated complementary through the relationship between the reference voltage and the triangular wave corresponding to V_{DC2} , and $S_{X, N1}$ is kept on-state. Then, since improper voltage sharing on DC link capacitors leads to an overvoltage on switches and, a failure of the 3LTI, the capacitor voltage change should be reflected in the triangular wave to maintain the DC link voltage balancing.

2.2 Analysis of operating modes

One phase of the T-type inverter has six operating modes according to the direction of the output current (i_x) and reference voltage (V_{X, RER}) as shown in Fig. 3. Modes 1, 3, 4, and 6 are same as two-level inverter operation modes. Mode 2 and 5 construct bidirectional current path between

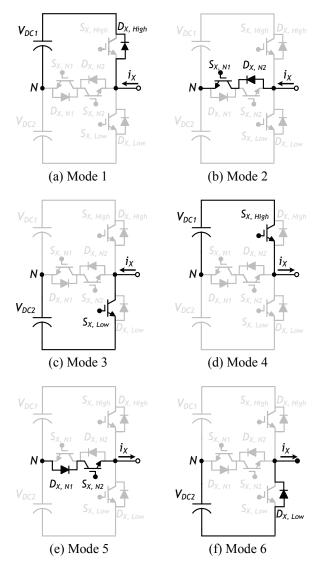


Fig. 3. Operation mode for one phase of T-type inverter

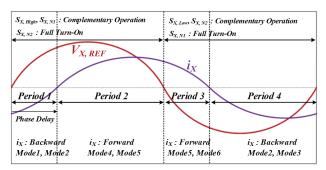


Fig. 4. Operating mode classification according to the relationship between the reference voltage and the load current

the neutral point and the output bridge. Therefore, the operating mode is selected one of two-level inverter operation modes (Mode 1, Mode 3, Mode 4, Mode 6) and one of bidirectional current path modes (Mode 2, Mode 5) as shown in Fig. 4. For instance, in period 1, since the output bridge is connected to the positive voltage level for the negative output current, mode 1 and mode 2 are selected. Therefore, mode 4 and mode 5 are selected in period 2, mode 5 and mode 6 are selected in period 3, and mode 2 and mode 3 are selected in period 4.

The proportion of each period is changed according to the phase delay. If the phase delay is increased, the proportion of period 1 and period 3 is increased, but the proportion of period 2 and period 4 is decreased. Furthermore, the utilization rate of $S_{X,\; High}$ and $S_{X,\; Low}$ is changed according to the magnitude of $V_{X,\; REF}$. If the size of $V_{X,\; REF}$ is bigger than the present value, $S_{X,\; High}$ and $S_{X,\; Low}$ are more frequently used. As a result, in the high MI areas, the 3LFI and the two-level inverter are similar in the utilization rate of switches. Therefore, the 3LFI efficiency is influenced by the phase delay and the MI.

3. Proposed Maximum Efficiency Operation Algorithm

3.1 Utilization rate of switch for 3LTI

The utilization rate of switches for the 3LTI is influenced by the MI, switching method and reference voltage angle. Especially, the utilization rate of switches is instantaneously varied according to the angle of the reference voltage in each cycle. For example, when the angle of the reference voltage is 30°, the utilization rate of the V-phase switch is always two regardless of the MI and switching method since the V-phase reference voltage is zero voltage. However, in this case, the utilization rate of the U-phase switch and W-phase switch is varied according to the MI and switching method. Fig. 5 shows the variation of the reference voltage in space vector pulse width modulation (SVPWM) and classification of areas according to the

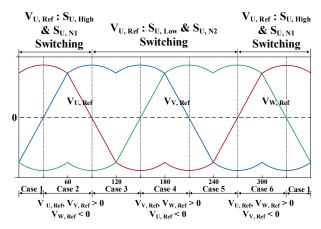


Fig. 5. Classification of areas according to reference voltage

reference voltage. As a result, controllable switches are changed according to the reference voltage. In case 1, case 2 and case 6, $V_{U, Ref}$ is the positive value. Therefore, in these cases, $V_{U, Ref}$ determines $S_{U, High}$ and $S_{U, N1}$ switching patterns and the utilization rate of $S_{U, High}$ and $S_{U, N1}$. However, in case 3, case 4 and case 5, $V_{U, Ref}$ is the negative value. Therefore, in contrast with case 1, case 2 and case 6, $V_{U, Ref}$ determines $S_{U, Low}$ and $S_{U, N2}$ switching patterns and the utilization rate of $S_{U, Low}$ and $S_{U, N2}$. Therefore, the instantaneous utilization rate of the switch (S_{θ}) for the SVPWM 3LTI can be calculated as

Case 1 (
$$\theta = 330^{\circ} \sim 30^{\circ}$$
)

$$S_{\theta} = 6 + \frac{2}{V_{DC}} V_{SN} - 2MI \cos \theta$$
 (1)

Case 2 (
$$\theta = 30^{\circ} \sim 90^{\circ}$$
)

$$S_{\theta} = 6 - \frac{2}{V_{DC}} V_{SN} - MI \cos \theta - \sqrt{3}MI \sin \theta$$
 (2)

Case 3 (
$$\theta = 90^{\circ} \sim 150^{\circ}$$
)

$$S_{\theta} = 6 + \frac{2}{V_{DS}} V_{SN} + MI \cos \theta - \sqrt{3} MI \sin \theta$$
(3)

Case 4 (
$$\theta = 150^{\circ} \sim 210^{\circ}$$
)
$$S_{\theta} = 6 - \frac{2}{V_{DC}} V_{SN} + 2MI \cos \theta$$
(4)

Case 5 (
$$\theta = 210^{\circ} \sim 270^{\circ}$$
)

$$S_{\theta} = 6 + \frac{2}{V_{DC}} V_{SN} + MI \cos \theta + \sqrt{3} MI \sin \theta$$
 (5)

Case 6 (
$$\theta = 270^{\circ} \sim 330^{\circ}$$
)

$$S_{\theta} = 6 - \frac{2}{V_{NS}} V_{SN} - MI \cos \theta - \sqrt{3}MI \sin \theta$$
 (6)

where V_{SN} is the offset voltage according to the switching method and θ is the angle of the reference voltage.

Basically, regardless of the MI and switching method, the average utilization rate of switches for the two-level

Table 1. Average utilization rate of switches according to the MI and the inverter topology

MI	Two-Level Inverter	Three-Level NPCI&FCI	3LTI (SVPWM)	
0.1	3	6	5.79	
0.2	3	6	5.59	
0.3	3	6	5.38	
0.4	3	6	5.18	
0.5	3	6	4.98	
0.6	3	6	4.77	
0.7	3	6	4.57	
0.8	3	6	4.36	
0.9	3	6	4.16	
1	3	6	3.96	

inverter is always three. The average utilization rate of switches for the three-level NPCI and FCI is always six. However, the average utilization rate of switches for the 3LTI is changed based on the MI and switching method as shown in Table 1. Neutral point switches are more used compared with high-side and low-side switches in the low MI. Since if the MI is increased, the utilization rate of high-side and low-side switches is also increased, the average utilization rate of switches is decreased. Therefore, if the MI is low, conduction losses of the 3LTI are similar to the three-level NPCI and FCI. However, if the MI is sufficiently high, conduction losses of the 3LTI are similar to the two-level inverter. Furthermore, in the case of using a discrete pulse width modulation, the average utilization rate of switches is much more decreased.

3.2 Efficiency calculation method and proposed maximum efficiency operation algorithm

Commonly, switching losses can be calculated by using the switching energy and switching frequency. However, since all switching actions during a fundamental period have to be considered, two assumptions are required. First, the switching frequency (f_{sw}) is higher than the fundamental frequency. Second, the switching actions evenly distributed over the fundamental period. Therefore, the average switching energy losses (E_{SWITCH}) and the switching losses (P_{SWITCH}) can be expressed as

$$E_{SWITCH} = \frac{V_{SWITCH}}{V_{PASE}} \frac{1}{2\pi} \int_{\alpha_1}^{\alpha_2} (AI_{PEAK} \sin \theta + B) d\theta$$
 (7)

$$P_{SWITCH} = E_{SWITCH} f_{SW}$$
 (8)

where V_{SWITCH} is the switching voltage, and V_{BASE} is the reference switching voltage, used in the datasheet. Using these two value, the switching energy is linearly scaled. θ represents the current angle, $I_{\mbox{\scriptsize PEAK}}$ is the maximum current value, and α_1 and α_2 represent the switching intervals within one fundamental period. A and B are the curvefitting constants for IGBTs $(A_S,\,B_S)$ and diodes $(A_D,\,B_D)$ switching energy.

In order to calculate the 3LTI switching losses, operation

Table 2. Operation switches and operation modes according to the switching intervals for the 3LTI

Switching Interval	Operation Switch	Operation Mode	Switching Voltage	
$0 \sim (\pi - \emptyset)$	$S_{X, High}$	Mode 4	V_{DC}	
$0 \sim (n - \emptyset)$	$D_{X, N1}$ & $S_{X, N2}$	Mode 5	$V_{DC}/2$	
(7. 0) 7.	$D_{X, Low}$	Mode 6	V_{DC}	
$(\pi - \emptyset) \sim \pi$	$D_{X, N1}$ & $S_{X, N2}$	Mode 5	$V_{DC}/2$	
$\pi \sim (2\pi - \emptyset)$	$S_{X, Low}$	Mode 3	V_{DC}	
$n \sim (2n - \emptyset)$	S _{X, N1} & D _{X, N2}	Mode 2	$V_{DC}/2$	
$(2\pi - \emptyset) \sim 2\pi$	$D_{X, High}$	Mode 1	V_{DC}	
(∠n - Ø) ~ 2n	S _{X, N1} & D _{X, N2}	Mode 2	$V_{DC}/2$	

switches are classified depending on the switching intervals as shown in Table 2. V_{SWITCH} is determined according to the connection position of the operation switch. The highside and low-side switches (S_{X, High}, S_{X, Low}) have to block the full DC link voltage. However, since the full DC link voltage is blocked by using two IGBTs in the neutral point switches $(S_{X, N1}, S_{X, N2})$, V_{SWITCH} of the neutral point switches is half of the full DC link voltage. Therefore, based on Table 2, the average switching losses for each switch can be calculated as

$$P_{SWITCH}(S_{X,High}) = P_{SWITCH}(S_{X,Low})$$

$$= \frac{V_{DC}}{V_{RASE}} \frac{f_{SW}}{2\pi} \int_{0}^{\pi-\phi} (A_{S}I_{PEAK} \sin \theta + B_{S}) d\theta \qquad (9)$$

$$P_{SWITCH}(S_{X,N1}) = P_{SWITCH}(S_{X,N2})$$

$$= \frac{V_{DC}}{V_{RASE}} \frac{f_{SW}}{4\pi} \int_{0}^{\pi} (A_{S} I_{PEAK} \sin \theta + B_{S}) d\theta \qquad (10)$$

$$\begin{split} P_{SWTTCH}(D_{X,High}) &= P_{SWTTCH}(D_{X,Low}) \\ &= \frac{V_{DC}}{V_{BASE}} \int_{2\pi}^{f_{SW}} \int_{\pi-\phi}^{\pi} (A_D I_{PEAK} \sin \theta + B_D) d\theta \ \ (11) \end{split}$$

$$P_{SWITCH}(D_{X,N1}) = P_{SWITCH}(D_{X,N2})$$

$$= \frac{V_{DC}}{V_{RASE}} \frac{f_{SW}}{4\pi} \int_{0}^{\pi} (A_D I_{PEAK} \sin \theta + B_D) d\theta \qquad (12)$$

where ø represents the phase delay angle.

Conduction losses can be calculated using the conduction I-V characteristics of the IGBT and anti-parallel diode. These characteristics can be approximated by using two curve-fitting constants with instantaneous current (i), on-state zero-current saturation voltage (V_0) and on-state resistance (R)

$$V(i) = V_0 + iR \tag{13}$$

Then, the average conduction losses (P_{CON}) can be expressed as

$$P_{CON} = \frac{1}{2\pi} \int_{\beta_1}^{\beta_2} DI_{PEAK} \sin \theta (V_0 + RI_{PEAK} \sin \theta) d\theta \qquad (14)$$

	T	ī		
Conduction switch	Conduction interval	Duty cycle	Output bridge state	
$S_{X, High}$	$0 \sim (\pi - \emptyset)$	$MIsin(\theta + \emptyset)$	$0 \rightarrow P$	
$S_{X, Low}$	$\pi \sim (2\pi - \emptyset)$	- $MIsin(\theta + \emptyset)$	$0 \rightarrow N$	
	$\pi \sim (2\pi - \emptyset)$	$1 + MIsin(\theta + \emptyset)$	$N \rightarrow 0$	
$S_{X, N1}$	$(2\pi - \emptyset) \sim 2\pi$	$1 - MIsin(\theta + \emptyset)$	$P \rightarrow 0$	
C	$0 \sim (\pi - \emptyset)$	$1 - MIsin(\theta + \emptyset)$	$P \rightarrow 0$	
$S_{X, N2}$	$(\pi - \emptyset) \sim \pi$	$1 + MIsin(\theta + \emptyset)$	$N \rightarrow 0$	
D _{X, High}	$(2\pi - \varnothing) \sim 2\pi$	$MIsin(\theta + \emptyset)$	0 → P	
$D_{X, Low}$	$(\pi - \emptyset) \sim \pi$	- $MIsin(\theta + \emptyset)$	0 → N	
	$0 \sim (\pi - \emptyset)$	$1 - MIsin(\theta + \emptyset)$	$P \rightarrow 0$	
$D_{X, Nl}$	$(\pi - \emptyset) \sim \pi$	$1 + MIsin(\theta + \emptyset)$	$N \rightarrow 0$	
D	$\pi \sim (2\pi - \emptyset)$	$1 + MIsin(\theta + \emptyset)$	$N \rightarrow 0$	
$D_{X, N2}$	$(2\pi - \varnothing) \sim 2\pi$	$1 - MIsin(\theta + \emptyset)$	$P \rightarrow 0$	

Table 3. Conduction switches and duty cycle according to the conduction intervals for the 3LTI

where D is a duty cycle, and β_1 and β_2 represent conduction angle intervals within one fundamental period.

The conduction interval and conduction switch can be classified as shown in Table 3. For example, in period 2, mode 4 and mode 5 are operated complementary by using $S_{X, High}$, $D_{X, N1}$ and $S_{X, N2}$. Therefore, the conduction interval can be determined as $0\sim(\pi-\varnothing)$. The duty cycle is assumed according to the output bridge state change. Based on Table 3, average conduction losses for each switch can be calculated as

$$\begin{split} P_{CON}(S_{X,High}) &= P_{CON}(S_{X,Low}) \\ &= \frac{1}{2\pi} \int_{0}^{\pi-\phi} MI \sin(\theta + \phi) I_{PEAK} \sin\theta (V_{0,S} + R_S I_{PEAK} \sin\theta) d\theta \\ &\qquad \qquad (15) \\ P_{CON}(S_{X,N1}) &= P_{CON}(S_{X,N2}) \\ &= \frac{1}{2\pi} \int_{0}^{\pi-\phi} \{1 - MI \sin(\theta + \phi)\} I_{PEAK} \sin\theta (V_{0,S} + R_S I_{PEAK} \sin\theta) d\theta \\ &+ \frac{1}{2\pi} \int_{\pi-\phi}^{\pi} \{1 + MI \sin(\theta + \phi)\} I_{PEAK} \sin\theta (V_{0,D} + R_D I_{PEAK} \sin\theta) d\theta \end{split}$$

$$\begin{split} P_{CON}(D_{X,High}) &= P_{CON}(D_{X,Low}) \\ &= \frac{1}{2\pi} \int_{\pi-\phi}^{\pi} -MI \sin(\theta + \phi) I_{PEAK} \sin \theta (V_{0,D} + R_D I_{PEAK} \sin \theta) d\theta \\ &\qquad (17) \\ P_{CON}(D_{X,N1}) &= P_{CON}(D_{X,N2}) \\ &= \frac{1}{2\pi} \int_{0}^{\pi-\phi} \{1 - MI \sin(\theta + \phi)\} I_{PEAK} \sin \theta (V_{0,D} + R_D I_{PEAK} \sin \theta) d\theta \\ &+ \frac{1}{2\pi} \int_{\pi-\phi}^{\pi} \{1 + MI \sin(\theta + \phi)\} I_{PEAK} \sin \theta (V_{0,D} + R_D I_{PEAK} \sin \theta) d\theta \end{split}$$

where $V_{0,S}$ and R_S is the IGBT on-state zero-current saturation voltage and on-state resistance, $V_{0,D}$ and R_D is the diode on-state zero-current saturation voltage and on-state resistance, respectively. Therefore, total conduction losses for the 3LTI can be calculated as

$$3[2P_{CON}(S_{X,High}) + 2P_{CON}(S_{X,N2}) + 2P_{CON}(D_{X,Low}) + 2P_{CON}(D_{X,N2})]$$

$$= \left[\frac{3}{2}(R_S + R_D) - \frac{1}{\pi}MI(R_S + R_D)\cos^2\phi - \frac{2}{\pi}MI(R_S + R_D)\right]I_{PEAK}^2$$

$$+ \left[\frac{6}{\pi}(V_{0,S} + V_{0,D}) - \frac{3}{2}V_{0,D}MI\cos\phi \right]$$

$$+ \frac{3}{2\pi}MI(V_{0,S} + V_{0,D})(\phi\cos\phi - \sin\phi)]I_{PEAK}$$
(19)

Table 4 shows calculation results of switching and conduction losses according to the MI in the half and full load condition. Conduction and switching losses are calculated based on the IKP10B60T (600V, 10A, Infineon), which was selected to implement the low-voltage and low-power 3LTI prototype. The percent value represents the ratio of the 3LTI calculation result according to the MI compared with the two-level inverter. 3LTI switching losses are smaller than two-level inverter, and conduction losses are varied from 193% to 133% according to the MI. Consequentially, the 3LTI has together higher and lower

Table 4. Calculation results of switching and conduction losses according to the MI

	Half Load Condition			Full Load Condition				
	$(I_{RMS} = 0.465A, f_{SW} = 10kHz, cos\emptyset = 0.8, V_{DC} = 311V)$			$(I_{RMS} = 0.75A, f_{SW} = 10kHz, cos\emptyset = 0.8, V_{DC} = 311V)$				
	2-Level Inverter Switching Losses = 3.353 [W]			2-Level Inverter Switching Losses = 3.753 [W]				
MI	3LFI Switching Losses = 2.606 (77.7%) [W]			3LFI Switching Losses = 2.926 (78%) [W]				
	Conduction Losses [W]		Total Losses [W]		Conduction Losses [W]		Total Losses [W]	
	2-Level	3LTI	2-Level	vel 3LTI	2-Level	3LFI	2-Level	3LTI
	Inverter		Inverter	Inverter	JLIT	Inverter	JLII	
0.1	1.406	2.723 (193%)	4.759	5.329 (111%)	2.299	4.451 (193%)	6.053	7.377 (121%)
0.2	1.394	2.619 (187%)	4.747	5.225 (110%)	2.287	4.279 (187%)	6.041	7.206 (119%)
0.3	1.39	2.514 (180%)	4.744	5.12 (107%)	2.275	4.108 (180%)	6.028	7.034 (116%)
0.4	1.383	2.41 (174%)	4.736	5.016 (105%)	2.263	3.936 (173%)	6.016	6.863 (114%)
0.5	1.375	2.306 (167%)	4.728	4.912 (103%)	2.251	3.765 (167%)	6.004	6.691 (111%)
0.6	1.368	2.202 (161%)	4.721	4.808 (101%)	2.239	3.593 (160%)	5.992	6.519 (108%)
0.7	1.36	2.098 (154%)	4.713	4.704 (99%)	2.227	3.422 (153%)	5.98	6.348 (106%)
0.8	1.352	1.994 (147%)	4.705	4.599 (97%)	2.215	3.25 (146%)	5.968	6.177 (103%)
0.9	1.345	1.889 (140%)	4.698	4.495 (95%)	2.203	3.079 (139%)	5.956	6.005 (101%)
1	1.337	1.785 (133%)	4.69	4.391 (93%)	2.191	2.907 (132%)	5.944	5.834 (98%)

efficiency areas compared with the two-level inverter. Especially, in the high MI, the 3LTI efficiency is higher than the two-level inverter. The magnitude and ratio of the calculated loss might be changed according to the electrical characteristics of the switching device, the overall trend of loss analysis could be similar to the evaluated results in Table 4.

If the 3LTI is applied in the low-voltage and low-power home appliance such as refrigerators and air conditioners, compared with the two-level inverter, it has low efficiency in the low speed region, but it has high efficiency in the high speed region. Especially, due to the low power factor, the efficiency is much lower in the low-load and low-speed region since the proportion of conduction losses is further increased.

The 3LTI consists of the general two-level inverter and six IGBTs. Six IGBTs are connected between the DC link midpoint and each output bridge in order to generate the zero voltage in the two-level inverter. Therefore, unlike the other well-known three-level inverter such as NPCI, FCI and CHBI, the 3LTI is possible the selective operation as shown in Fig. 6, such as the two-level operation mode and the three-level operation mode. If the operation mode is selected to drive maximum efficiency according to the load current, MI and power factor as shown in Fig. 7, the 3LTI is possible to always obtain the maximum efficiency. Based on each mode efficiency, the 3LTI is operated two-level operation mode in low-speed region, and it is operated three-level operation mode in high-speed region.

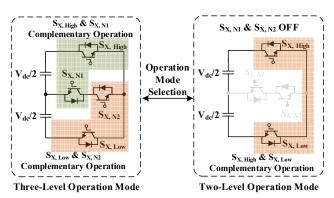


Fig. 6. Three-level and two-level operation mode

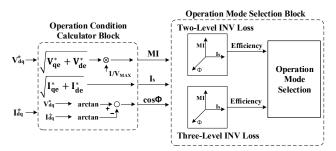
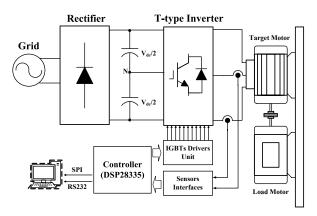


Fig. 7. Operation mode selection according to each mode efficiency

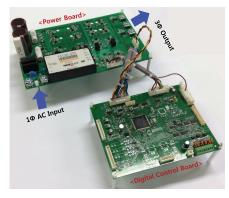
4. Experimental Results

A prototype of the 3LTI system was built to verify the validity of the proposed maximum efficiency operation strategy. Fig. 8 shows the entire block diagram of the 3LTI test-bed, along with the prototype. The strategy was implemented base on a digital signal process 28335, and 600-V 10-A Infineon IKP10B60T single IGBT is used for the 3LTI. Also, an interior permanent magnet synchronous motor (IPMSM) for a refrigerator driver system is applied to the experiment test-bed and the proposed strategy is verified under the operation condition of refrigerator. The conditions and parameters of the experiments are shown in Table 5. The output waveform of the three-level operation mode and two-level operation mode are shown in Fig. 9.

Fig. 10 shows the 3LTI efficiency without and with the proposed strategy under half and full loads. In the low



(a) Block diagram of the experiment test-bed

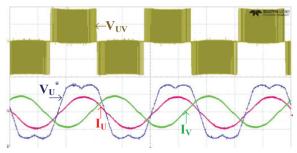


(b) Prototype of 3LTI and controller

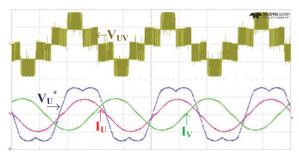
Fig. 8. Experimental test-bed

Table 5. Experimental conditions and motor parameter

Parameter	Value		
DC link voltage	311V		
Switching frequency	10kHz		
Target motor type	IPMSM		
R_s	3.95Ω		
L_d / L_q	81.62 / 114.6mH		

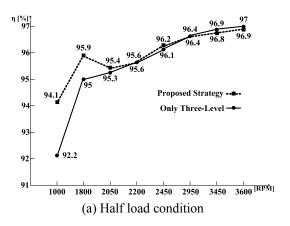


(a) Case of two-level operation



(b) Case of three-level operation

Fig. 9. Output voltage and current waveforms according to operation modes (V_{UV}: 50V/div., I_U: 1A/div., I_V: 1A/div., V_U*: 1V/div.)



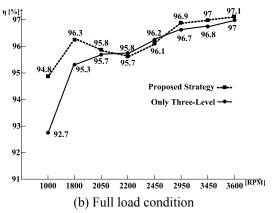
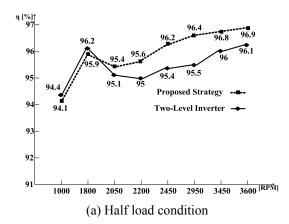


Fig. 10. 3LTI efficiency comparison between the threelevel mode operation and the proposed strategy operation



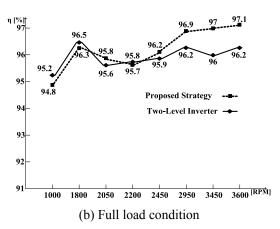


Fig. 11. Efficiency comparison between the two-level inverter and the proposed strategy operation

MI region such as 1000RPM and 1800RPM, the 3LTI efficiency is improved about 2% compared with the twolevel mode by using the proposed strategy. Similarly, in the half load condition, the 3LTI efficiency with the proposed strategy is improved about 2%. In the motor speed higher than 2000RPM, since the efficiency of the three-level operation mode is higher than the efficiency of the twolevel operation mode, the 3LTI with the proposed strategy is operated as the three-level operation mode.

Fig. 11 shows 3LTI efficiency with the proposed strategy and the two-level inverter efficiency. In the low MI region, since the 3LTI is operated the two-level operation mode, the two-level inverter and the 3LTI efficiency are similar. However, in the middle and high MI region, the 3LTI efficiency is higher than the two-level inverter since the 3LTI is operated as the three-level operation mode. As a result, the 3LTI with the proposed strategy can be always obtained the maximum efficiency in all operation areas.

5. Conclusion

This paper has analyzed the maximum efficiency operation strategy for the 3LTI in low-voltage and lowpower home appliance. Unlike the other well-known threelevel inverter such as the three-level NPCI and FCI, the efficiency of the 3LTI is effected by the utilization rate of switches. In the low MI region, the efficiency of the 3LTI is similar to the general three-level inverters since the utilization rate of switches is increased. However, in the high MI region, the efficiency of the 3LTI is similar to the two-level inverter since the utilization rate of switches is decreased. Therefore, compared with the twolevel inverter, the 3LTI has together higher and lower efficiency areas according to the MI. To overcome this characteristic, two operation mode selection strategy is proposed for maximum efficiency operation. Based on each mode efficiency, the 3LTI is operated two-level operation mode in low MI, and it is operated three-level operation mode in high MI. As a result, the 3LTI can always obtain the maximum efficiency in all operation areas. The validity of the proposed strategy has been verified by experimental results.

References

- Emre ün and Ahmet M. Hava, "A Near-State PWM Method with Reduced Switching Losses and Reduced Common-Mode Voltage for Three-Phase Voltage Source Inverters," IEEE Trans. Industry Applications, vol.45, no.2, pp.782-793, Mar. 2009.
- Abhijit Choudhury, Pragasen Pillay, M. Amar and Sheldon S. Williamson, "Performance Comparison study of Two and Three-Level Inverter for Electric Vehicle Application," Transportation Electrification Conference and Expo (ITEC), 2014 IEEE, Dearborn, USA, June. 2014.
- Hojoon Shin and Jung-Ik Ha, "Phase Current Reconstructions from DC-Link Currents in Three-Phase Three-Level PWM Inverters," IEEE Trans. Power Electronics, vol. 29, no. 2, pp. 582-593, Feb. 2014.
- Jun-ichi Itoh, Takumi Ogura, "Evaluation of Total Loss for An Inverter and Motor by Applying Modulation Strategies," in Proceedings of IEEE EPE, 2010, pp. S12-21-S12-28, Ohrid, Macedonia, Sept 2010.
- M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the chip area usage of 2-level and 3level voltage source converter Topologies," in Proc. 36th Annu. Conf. IEEE Ind. Electron., pp. 391-396, Nov. 2012.
- R. Teichmann and S. Bernet, "A comparison of threelevel converters versus two-level converters for lowvoltage drives, tractions, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, no. 3, pp. 855-865, May/Jun. 2005. 391-396, Nov. 2012.
- Dordevic. O, Jones. M, and Levi E, "A Comparison of Carrier-Based and Space Vector PWM Technique for the Three-Level Five-Phase Voltage Source Inverter," IEEE Trans. Industrial Informatics, vol. 9, no. 2, pp. 609-619, May. 2009.

- Schweiser. M, Feiedli, and Kolar. W, "Comparative Evaluation of Advanced Three-Level Inverter / Converter Topologies against Two-Level Systems," IEEE Trans. Industrial Electronics, vol. 60, no. 12, pp. 5515-5527, Nov. 2013.
- Felipe J. C. Padilha, Walter Issamu Suemitsu, Maria Dias Bellar, and Plutarcho Maravilha Lourenco, "Low-Cost Gate Drive Circuit for Three-level Neutral-Point-Clamped Voltage-Source Inverter," IEEE Trans. Ind. Electron, vol. 56, no. 4, pp. 1196-1204, Apr. 2009.
- [10] Felipe J. C. Padilha, Walter Issamu Suemitsu, Maria Dias Bellar, and Plutarcho Maravilha Lourenco, "A Hybrid Cascade Converter Topology with Series-Connected Symmetrical and Asymmetrical Diode-Clamped H-Bridge Cells," IEEE Trans. Power Electron., vol. 26, no. 1, pp. 51-65, Jan. 2011.
- [11] Felipe J. C. Padilha, Walter Issamu Suemitsu, Maria Dias Bellar, and Plutarcho Maravilha Lourenco, "Modified DC-Link Voltage Balancing Algorithm for a 3-Level Neutral Point Clamped (NPC) Traction Inverter Based Electric Vehicle PMSM Drive," in Proc. Annual Conf. of the IEEE Industrial Electronics *Society,* Vienna, Austria, pp. 4660-4665, Nov. 2013.
- [12] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium Voltage Multilevel Converters: State of the art, Challenges and Requirements in Industrial Applications," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581-2596, Aug. 2010.
- [13] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A Survey on Neutral-Point-Clamped Inverters," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2219-2230, Jul. 2009.
- [14] Suleiman M. Sharkh, Mohammad A. Abusara, Georgios I. Orfanoudakis, and Babar Hussain, 'Loss Comparison of Two- and Three-Level Inverter Topologies: Power Electronic Converter for Microgrids, John Wiley & Sons, 2014.
- [15] Mario Schweizer, Johann W. Kolar, "Design and Implementation of a Highly Efficiency Three-Level T-Type Converter for Low-Voltage Applications," IEEE Trans. Ind. Electron., vol. 28, no. 2, pp. 889-907, Feb. 2013.
- [16] Ui-Min Choi, Kyo-Beum Lee, Frede Blaabjerg, "Diagnosis and Tolerant Strategy of an Open-Switch Fault for T-Type Three-Level Inverter Systems," IEEE Trans. Ind. Appl., vol. 50, no. 1, pp. 495-508, Jan / Feb. 2014.
- [17] K. Komatsu, M. Yatsu, S. Miyashita, S. Okita, H. Nakazawa, S. Igarashi, Y. Takahashi, Y. Okuma, Y. Seki, and T. Fujihira, "New IGBT Modules for Advanced Neutral-Point-Clamped 3-Level Power Converters," in Conf. Rec. IPEC, pp. 523-527, June. 2010.



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